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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN
Supplier Device Package	28-UFQFPN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l031g4u6

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2 Description

The access line ultra-low-power STM32L031x4/6 family incorporates the high-performance ARM® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, high-speed embedded memories (up to 32 Kbytes of Flash program memory, 1 Kbytes of data EEPROM and 8 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L031x4/6 devices provide high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L031x4/6 devices offer several analog features, one 12-bit ADC with hardware oversampling, two ultra-low-power comparators, several timers, one low-power timer (LPTIM), three general-purpose 16-bit timers, one RTC and one SysTick which can be used as timebases. They also feature two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L031x4/6 devices embed standard and advanced communication interfaces: one I2C, one SPI, one USART, and a low-power UART (LPUART).

The STM32L031x4/6 also include a real-time clock and a set of backup registers that remain powered in Standby mode.

The ultra-low-power STM32L031x4/6 devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +125 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.



Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the V_{PVD} threshold and/or when $V_{DD/VDDA}$ is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wake-up logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC_CSR).

3.4.4 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1 (PA4, PA5, PA6, PA7), USART2 (PA2, PA3) or USART2 (PA9, PA10). See STM32™ microcontroller system memory boot mode AN2606 for details.

3.5 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**
To get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**
Clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management**
To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source**
Three different clock sources can be used to drive the master clock SYSCLK:
 - 1-25 MHz high-speed external (HSE), that can supply a PLL
 - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
 - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a $\pm 0.5\%$ accuracy.
- **Auxiliary clock source**
Two ultra-low-power clock sources that can be used to drive the real-time clock:
 - 32.768 kHz low-speed external crystal (LSE)
 - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC clock sources**
The LSI, LSE or HSE sources can be chosen to clock the RTC, whatever the system clock.
- **Startup clock**
After reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS)**
This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled. Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output)**
It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See [Figure 2](#) for details on the clock tree.

Table 11. STM32L031x4/6 I²C implementation

I2C features ⁽¹⁾	I2C1
7-bit addressing mode	X
10-bit addressing mode	X
Standard mode (up to 100 kbit/s)	X
Fast mode (up to 400 kbit/s)	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X ⁽²⁾
Independent clock	X
SMBus	X
Wakeup from STOP	X

1. X = supported.

2. See [Table 15: Pin definitions on page 38](#) for the list of I/Os that feature Fast Mode Plus capability

3.15.2 Universal synchronous/asynchronous receiver transmitter (USART)

The USART interface (USART2) is able to communicate at speeds of up to 4 Mbit/s.

it provides hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART2 also supports Smartcard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock that allows to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

USART2 interface can be served by the DMA controller.

[Table 12](#) for the supported modes and features of USART interface.

Table 12. USART implementation

USART modes/features ⁽¹⁾	USART2
Hardware flow control for modem	X
Continuous communication using DMA	X
Multiprocessor communication	X
Synchronous mode ⁽²⁾	X
Smartcard mode	X
Single-wire half-duplex communication	X
IrDA SIR ENDEC block	X
LIN mode	X
Dual clock domain and wakeup from Stop mode	X
Receiver timeout interrupt	X
Modbus communication	X
Auto baud rate detection (4 modes)	X
Driver Enable	X

1. X = supported.

2. This mode allows using the USART as an SPI master.

3.15.3 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed one Low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wake up the system from Stop mode using baudrates up to 46 Kbaud. The Wakeup events from Stop mode are programmable and can be:

- Start bit detection
- Or any received data frame
- Or a specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

3.15.4 Serial peripheral interface (SPI)

The SPI is able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The USARTs with synchronous capability can also be used as SPI master.

The SPI can be served by the DMA controller.

Refer to [Table 13](#) for the supported modes and features of SPI interface.

Table 13. SPI implementation

SPI features ⁽¹⁾	SPI1
Hardware CRC calculation	X
I2S mode	-
TI mode	X

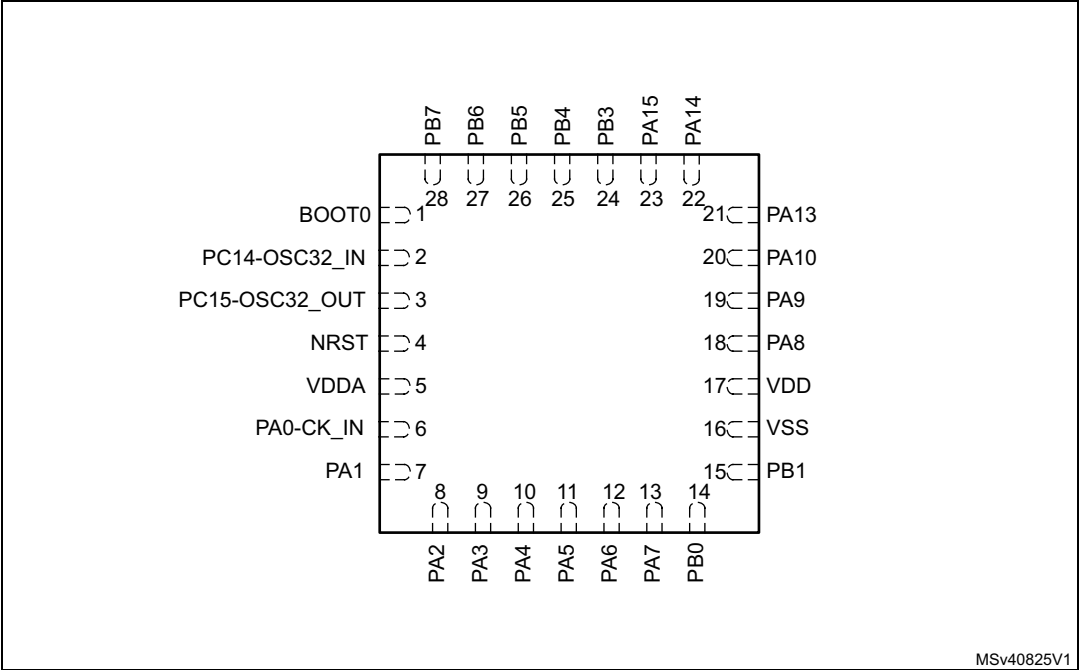
1. X = supported.

3.16 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

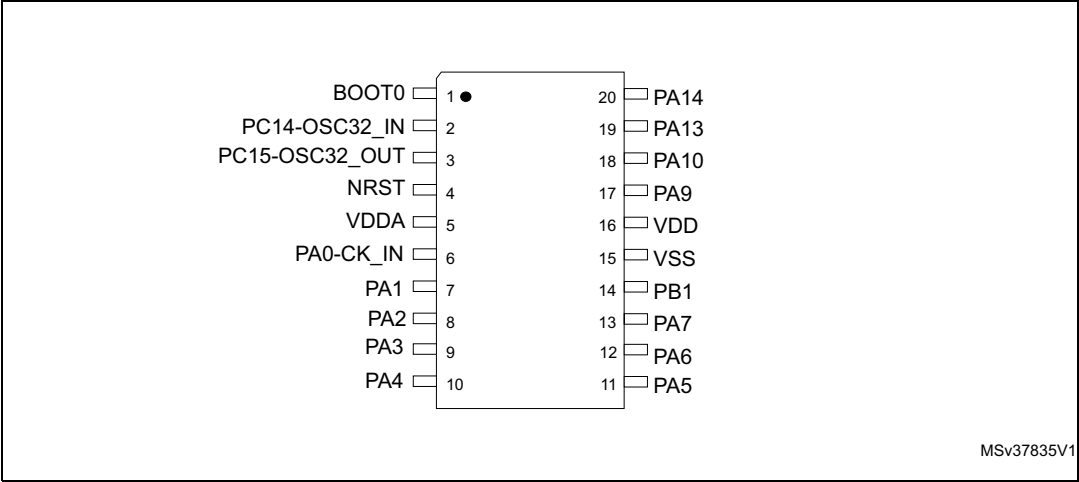
Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of

Figure 7. STM32L031GxUxS UFQFPN28 pinout



1. The above figure shows the package top view.
2. This pinout applies only to STM32L031GxUxS part number.

Figure 8. STM32L031x4/6 TSSOP20 pinout



1. The above figure shows the package top view.

Table 28. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f _{HCLK}	Typ	Max ⁽¹⁾	Unit
I _{DD} (Sleep)	Supply current in Sleep mode, Flash memory OFF	f _{HSE} = f _{HCLK} up to 16 MHz included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL ON) ⁽²⁾	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	1 MHz	36.5	87	µA
				2 MHz	58	100	
				4 MHz	100	170	
			Range 2, V _{CORE} =1.5 V, VOS[1:0]=10	4 MHz	125	190	
				8 MHz	230	310	
				16 MHz	450	540	
			Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	8 MHz	275	360	
				16 MHz	555	650	
				32 MHz	1350	1600	
		HSI16 clock source (16 MHz)	Range 2, V _{CORE} =1.5 V, VOS[1:0]=10	16 MHz	585	690	
			Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	32 MHz	1500	1700	
		MSI clock	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	65 kHz	17	43	
				524 kHz	28	55	
				4.2 MHz	115	190	
	Supply current in Sleep mode, Flash memory ON	f _{HSE} = f _{HCLK} up to 16 MHz included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL ON) ⁽²⁾	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	1 MHz	49	160	
				2 MHz	69	190	
				4 MHz	115	230	
			Range 2, V _{CORE} =1.5 V, VOS[1:0]=10	4 MHz	135	200	
				8 MHz	240	320	
				16 MHz	460	550	
			Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	8 MHz	290	370	
				16 MHz	565	670	
				32 MHz	1350	1600	
		HSI16 clock source (16 MHz)	Range 2, V _{CORE} =1.5 V, VOS[1:0]=10	16 MHz	600	700	
			Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	32 MHz	1500	1700	
		MSI clock	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	65 kHz	28	55	
				524 kHz	39.5	67	
				4.2 MHz	125	200	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Low-speed external user clock generated from an external source

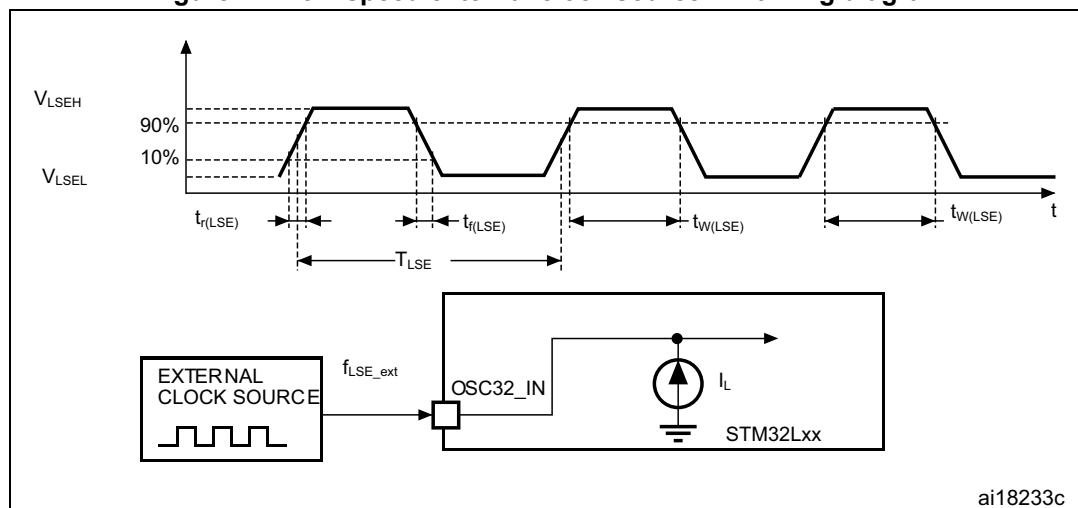
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 20](#).

Table 38. Low-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

1. Guaranteed by design.

Figure 21. Low-speed external clock source AC timing diagram



ai18233c

Table 43. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	μs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	
$t_{STAB(MSI)}^{(2)}$	MSI oscillator stabilization time	MSI range 0	-	40	μs
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
		MSI range 4	-	2.5	
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage range 3	-	3	
$f_{OVER(MSI)}$	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
		Any range to range 6	-	6	

1. This is a deviation for an individual part, once the initial frequency has been measured.

2. Guaranteed by characterization results.

6.3.8 PLL characteristics

The parameters given in [Table 44](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 20](#).

Table 44. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max ⁽¹⁾	
f_{PLL_IN}	PLL input clock ⁽²⁾	2	-	24	MHz
	PLL input clock duty cycle	45	-	55	%

Table 44. PLL characteristics (continued)

Symbol	Parameter	Value			Unit
		Min	Typ	Max ⁽¹⁾	
$f_{\text{PLL_OUT}}$	PLL output clock	2	-	32	MHz
t_{LOCK}	PLL input = 16 MHz PLL VCO = 96 MHz	-	115	160	μs
Jitter	Cycle-to-cycle jitter	-		± 600	ps
$I_{\text{DDA}}(\text{PLL})$	Current consumption on V_{DDA}	-	220	450	μA
$I_{\text{DD}}(\text{PLL})$	Current consumption on V_{DD}	-	120	150	

1. Guaranteed by characterization results.

2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by $f_{\text{PLL_OUT}}$.

6.3.9 Memory characteristics

RAM memory

Table 45. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode ⁽¹⁾	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory and data EEPROM

Table 46. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max ⁽¹⁾	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t_{prog}	Programming time for word or half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I_{DD}	Average current during the whole programming / erase operation	$T_{\text{A}} = 25\text{ }^{\circ}\text{C}$, $V_{\text{DD}} = 3.6\text{ V}$	-	500	700	μA
	Maximum current (peak) during the whole programming / erase operation		-	1.5	2.5	mA

1. Guaranteed by design.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 49. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. f_{osc}/f_{CPU}	Unit
				8 MHz/32 MHz	
S _{EMI}	Peak level	V _{DD} = 3.6 V, T _A = 25 °C, LQFP48 package conforming to IEC61967-2	0.1 to 30 MHz	-10	dBμV
			30 to 130 MHz	5	
			130 MHz to 1GHz	-5	
			EMI Level	1.5	-

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 50. ESD absolute maximum ratings

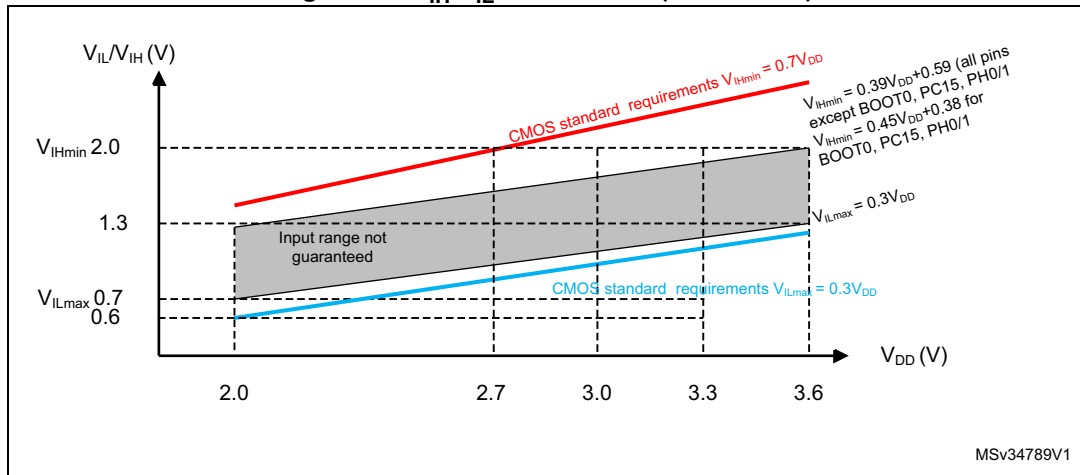
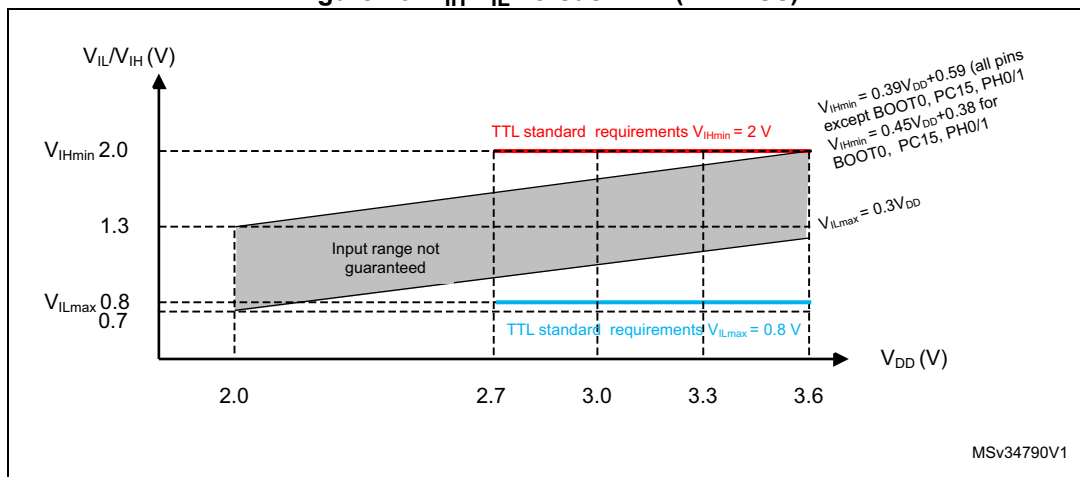
Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T _A = +25 °C, conforming to ANSI/JEDEC JS-001	2	2000	V
V _{ESD(CDM)}	Electrostatic discharge voltage (charge device model)	T _A = +25 °C, conforming to ANSI/ESD STM5.3.1.	C4	500	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

Figure 25. V_{IH}/V_{IL} versus V_{DD} (CMOS I/Os)Figure 26. V_{IH}/V_{IL} versus V_{DD} (TTL I/Os)

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 15 mA with the non-standard V_{OL}/V_{OH} specifications given in [Table 54](#).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating $I_{VDD(\Sigma)}$ (see [Table 18](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $I_{VSS(\Sigma)}$ (see [Table 18](#)).

Figure 29. ADC accuracy characteristics

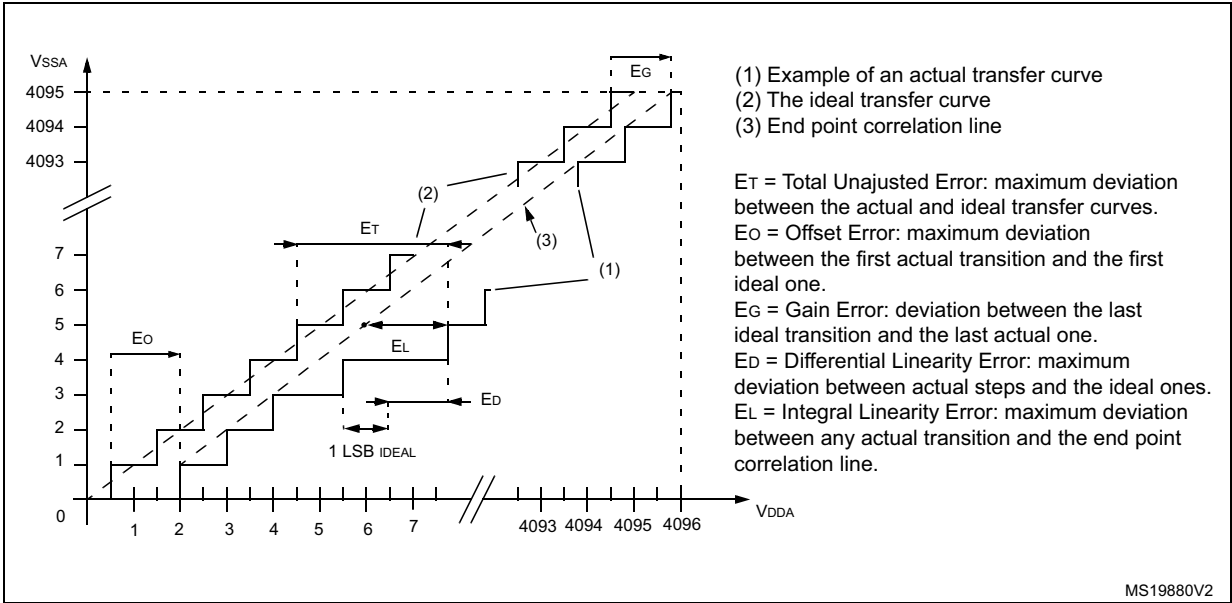
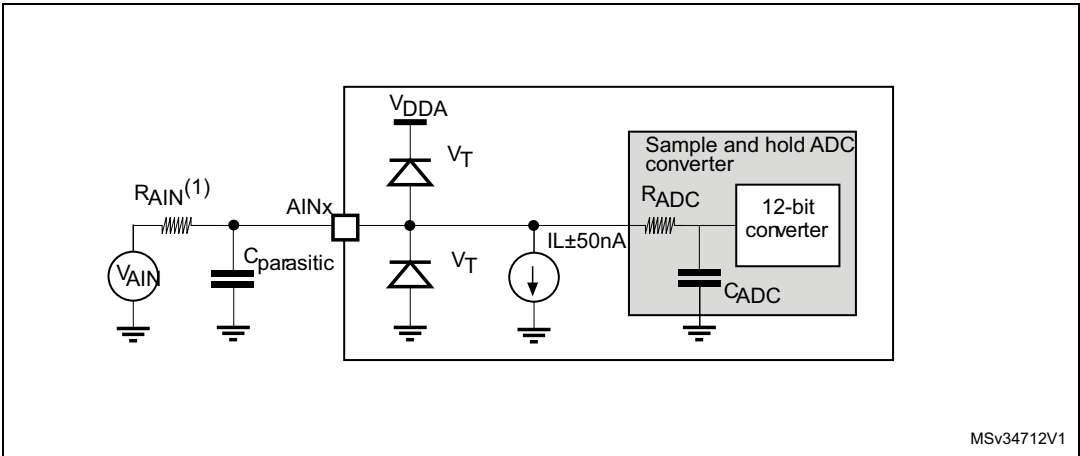


Figure 30. Typical connection diagram using the ADC



1. Refer to [Table 57: ADC characteristics](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

6.3.16 Temperature sensor characteristics

Table 60. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, $V_{DDA} = 3$ V	0x1FF8 007A - 0x1FF8 007B
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C $V_{DDA} = 3$ V	0x1FF8 007E - 0x1FF8 007F

Table 63. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max ⁽¹⁾	Unit
V _{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V _{IN}	Comparator 2 input voltage range	-	0	-	V _{DDA}	V
t _{START}	Comparator startup time	Fast mode	-	15	20	μs
		Slow mode	-	20	25	
t _{d slow}	Propagation delay ⁽²⁾ in slow mode	1.65 V ≤ V _{DDA} ≤ 2.7 V	-	1.8	3.5	
		2.7 V ≤ V _{DDA} ≤ 3.6 V	-	2.5	6	
t _{d fast}	Propagation delay ⁽²⁾ in fast mode	1.65 V ≤ V _{DDA} ≤ 2.7 V	-	0.8	2	
		2.7 V ≤ V _{DDA} ≤ 3.6 V	-	1.2	4	
V _{offset}	Comparator offset error		-	±4	±20	mV
dThreshold/ dt	Threshold voltage temperature coefficient	V _{DDA} = 3.3V T _A = 0 to 50 °C V ₋ = V _{REFINT} , 3/4 V _{REFINT} , 1/2 V _{REFINT} , 1/4 V _{REFINT}	-	15	30	ppm / °C
I _{COMP2}	Current consumption ⁽³⁾	Fast mode	-	3.5	5	μA
		Slow mode	-	0.5	2	

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

6.3.18 Timer characteristics

TIM timer characteristics

The parameters given in the [Table 64](#) are guaranteed by design.

Refer to [Section 6.3.13: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 64. TIMx⁽¹⁾ characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t _{res(TIM)}	Timer resolution time		1	-	t _{TIMxCLK}
		f _{TIMxCLK} = 32 MHz	31.25	-	ns
f _{EXT}	Timer external clock frequency on CH1 to CH4		0	f _{TIMxCLK} /2	MHz
		f _{TIMxCLK} = 32 MHz	0	16	MHz
Res _{TIM}	Timer resolution	-		16	bit

Table 64. TIMx⁽¹⁾ characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
t _{COUNTER}	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	t _{TIMxCLK}
		f _{TIMxCLK} = 32 MHz	0.0312	2048	μs
t _{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	t _{TIMxCLK}
		f _{TIMxCLK} = 32 MHz	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM21, and TIM22 timers.

6.3.19 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I²C timing requirements are guaranteed by design when the I²C peripheral is properly configured (refer to the reference manual for details). The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to [Section 6.3.13: I/O port characteristics](#) for the I2C I/Os characteristics).

All I²C SDA and SCL I/Os embed an analog filter (see [Table 65](#) for the analog filter characteristics).

Table 65. I2C analog filter characteristics⁽¹⁾

Symbol	Parameter	Min	Max	Unit
t _{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50 ⁽²⁾	260 ⁽³⁾	ns

1. Guaranteed by design.
2. Spikes with widths below t_{AF(min)} are filtered.
3. Spikes with widths above t_{AF(max)} are not filtered

USART/LPUART characteristics

The parameters given in the following table are guaranteed by design.

Table 66. USART/LPUART characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wake up from Stop mode	Stop mode with main regulator in Run mode, Range 2 or 3	-	8.7	μs
		Stop mode with main regulator in Run mode, Range 1	-	8.1	
		Stop mode with main regulator in low-power mode, Range 2 or 3	-	12	
		Stop mode with main regulator in low-power mode, Range 1	-	11.4	

Table 69. SPI characteristics in voltage Range 3 ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_c(SCK)$	SPI clock frequency	Master mode	-	-	2	MHz
		Slave mode			$2^{(2)}$	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su}(NSS)$	NSS setup time	Slave mode, SPI presc = 2	$4 \cdot T_{pclk}$	-	-	ns
$t_h(NSS)$	NSS hold time	Slave mode, SPI presc = 2	$2 \cdot T_{pclk}$	-	-	
$t_w(SCKH)$ $t_w(SCKL)$	SCK high and low time	Master mode	$T_{pclk}-2$	T_{pclk}	$T_{pclk}+2$	
$t_{su}(MI)$	Data input setup time	Master mode	28.5	-	-	
$t_{su}(SI)$		Slave mode	22	-	-	
$t_h(MI)$	Data input hold time	Master mode	7	-	-	
$t_h(SI)$		Slave mode	5	-	-	
$t_a(SO)$	Data output access time	Slave mode	30	-	70	
$t_{dis}(SO)$	Data output disable time	Slave mode	40	-	80	
$t_v(SO)$	Data output valid time	Slave mode	-	53	86	
		Master mode	-	30	54	
$t_v(MO)$	Data output hold time	Slave mode	18	-	-	
$t_h(SO)$		Master mode	8	-	-	

1. Guaranteed by characterization results.

2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_v(SO)$ and $t_{su}(MI)$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su}(MI) = 0$ while $Duty_{(SCK)} = 50\%$.

Figure 31. SPI timing diagram - slave mode and CPHA = 0

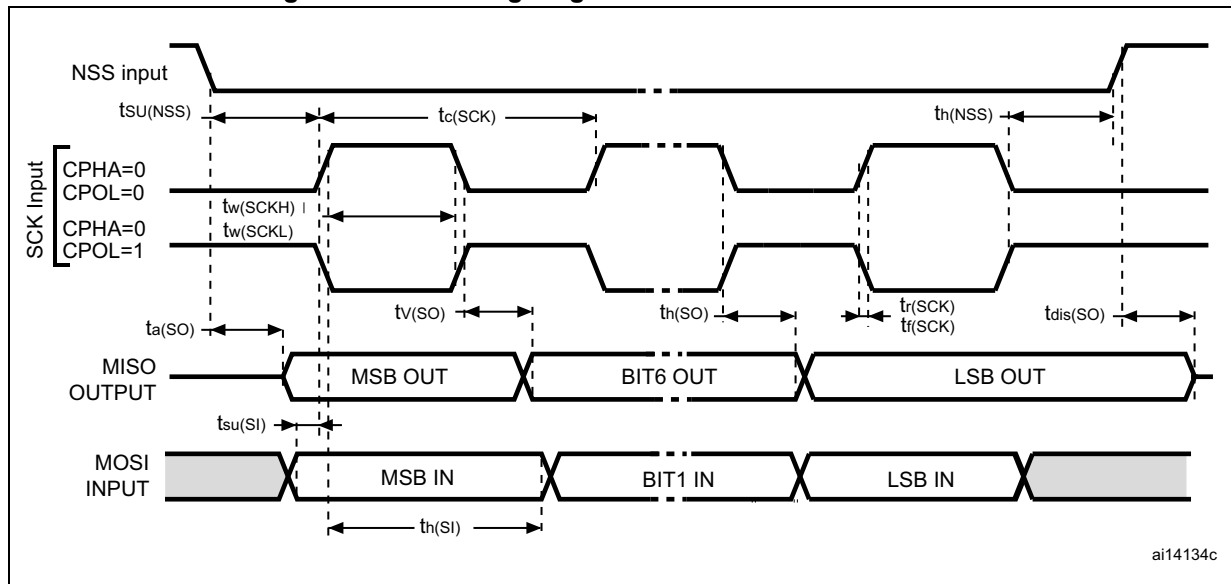
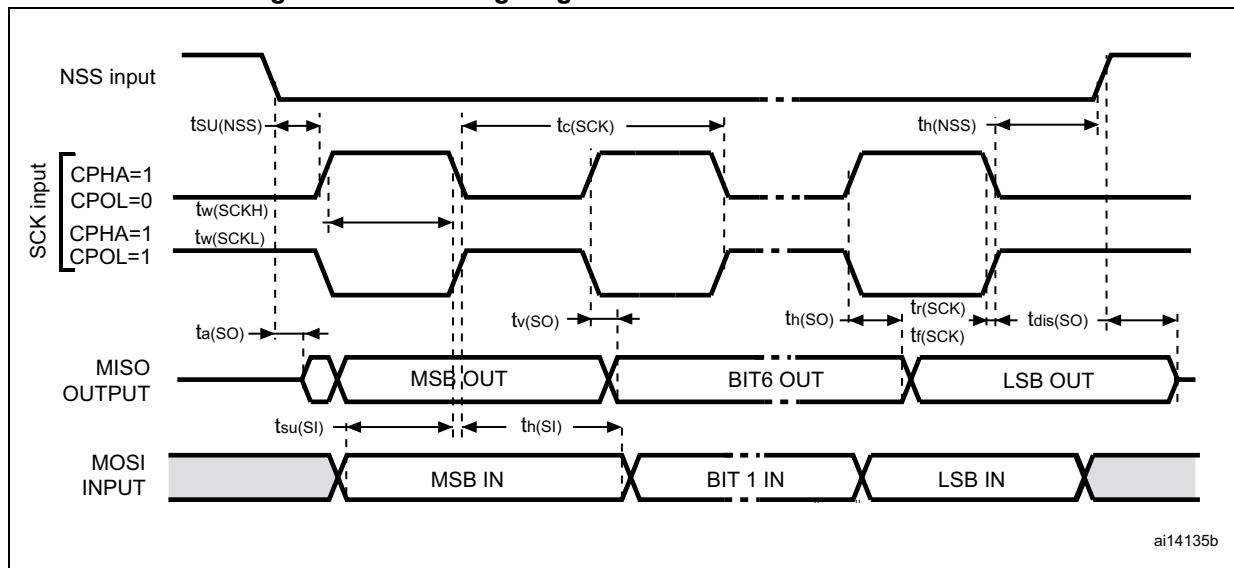
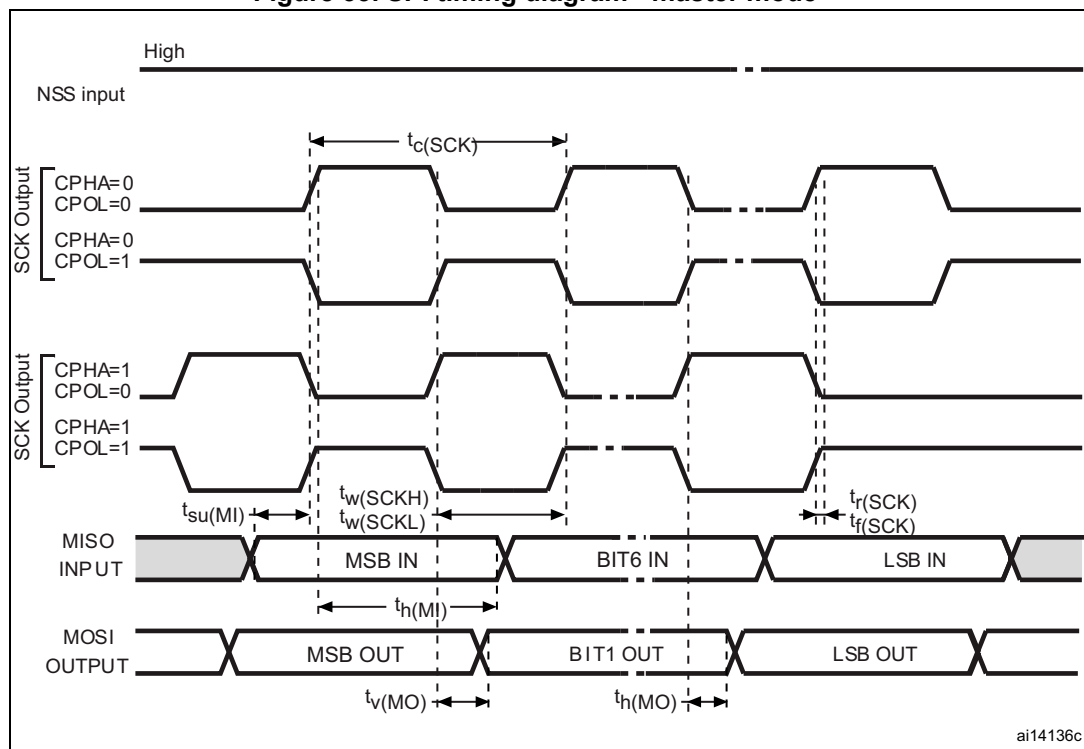


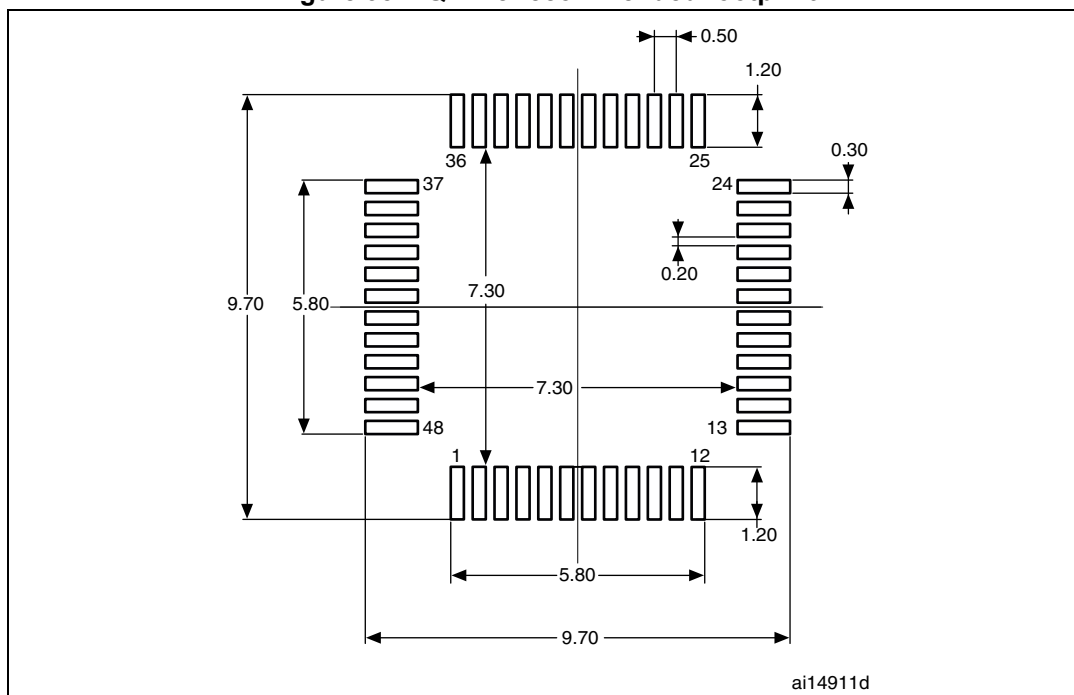
Figure 32. SPI timing diagram - slave mode and CPHA = 1⁽¹⁾

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 33. SPI timing diagram - master mode⁽¹⁾

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 35. LQFP48 recommended footprint

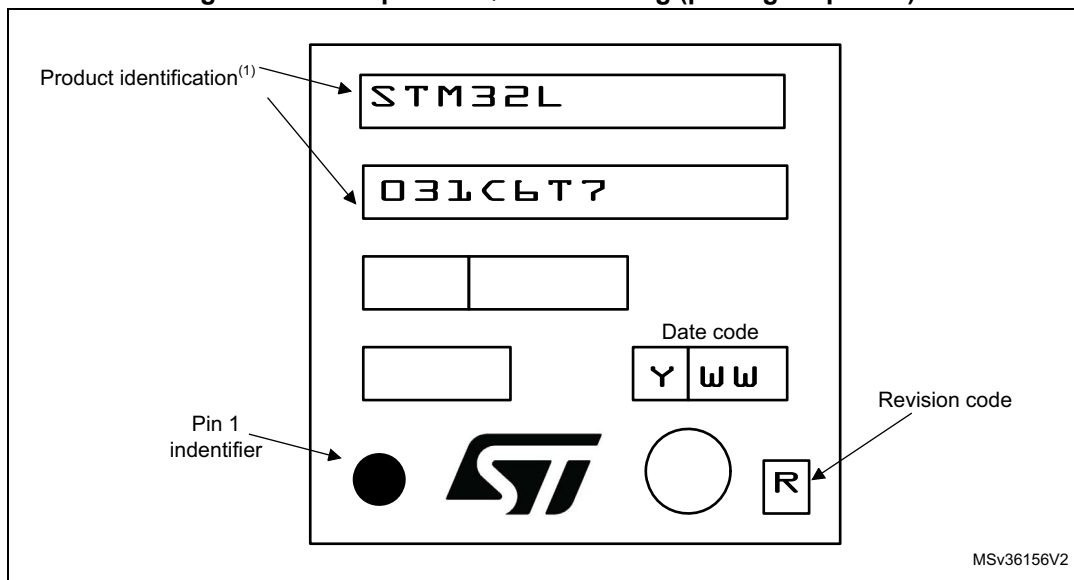


1. Dimensions are expressed in millimeters.

LQFP48 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 36. Example of LQFP48 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.