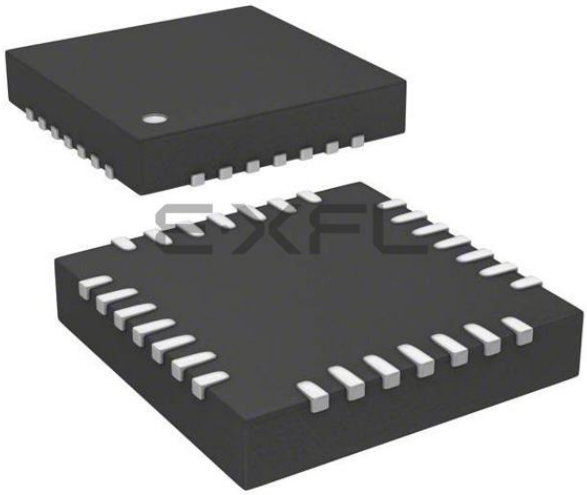


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 10x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-UFQFN |
| Supplier Device Package | 28-UFQFPN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l031g6u7 |

# Contents

## 2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM® Cortex®-M4, including ARM® Cortex®-M3 and ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 Ultra-low-power series are the best solution for applications such as gas/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

# 3 Functional overview

## 3.1 Low-power modes

The ultra-low-power STM32L031x4/6 supports dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 ($V_{DD}$ range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full $V_{DD}$ range), with a maximum CPU frequency of 16 MHz
- Range 3 (full $V_{DD}$ range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

  This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

  When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

- **Stop mode with RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the $V_{CORE}$ domain are stopped, the PLL, MSI RC, HSE and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event

## 3.6 Low-power real-time clock and backup registers

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms with wake up from Stop and Standby mode capability
- Periodic wakeup from Stop and Standby with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 37 kHz)
- The high-speed external clock

## 3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

### Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 26 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 38 GPIOs can be connected to the 16 configurable interrupt/event lines. The 10 other lines are connected to PVD, RTC, USART, I2C, LPUART, LPTIMER or comparator events.

The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers.

## 3.11 Temperature sensor

The temperature sensor ($T_{SENSE}$) generates a voltage $V_{SENSE}$ that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

**Table 7. Temperature sensor calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| TSENSE_CAL1 | TS ADC raw data acquired at temperature of 30 °C, $V_{DDA}$= 3 V | 0x1FF8 007A - 0x1FF8 007B |
| TSENSE_CAL2 | TS ADC raw data acquired at temperature of 130 °C, $V_{DDA}$= 3 V | 0x1FF8 007E - 0x1FF8 007F |

### 3.11.1 Internal voltage reference ($V_{REFINT}$)

The internal voltage reference ($V_{REFINT}$) provides a stable (bandgap) voltage output for the ADC and Comparators. $V_{REFINT}$ is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the $V_{DD}$ value (since no external voltage, $V_{REF+}$, is available for ADC). The precise voltage of $V_{REFINT}$ is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

**Table 8. Internal voltage reference measured values**

| Calibration value name | Description | Memory address |
|---|---|---|
| VREFINT_CAL | Raw data acquired at temperature of 25 °C $V_{DDA}$ = 3 V | 0x1FF8 0078 - 0x1FF8 0079 |

Table 15. Pin definitions (continued)

| Pin Number | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Note | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TSSOP20 | WLCSP25[1] | UFQFPN28 | UFQFPN28 (STM32L031GxUxS only) | LQFP32 | UFQFPN32[2] | LQFP48 | | | | | | |
| - | - | - | - | - | - | 35 | VSS | S | - | - | - | - |
| - | D1 | - | - | - | - | 36 | VDD | S | - | - | - | - |
| 20 | A2 | 22 | 22 | 24 | 24 | 37 | PA14 | I/O | FT | - | SWCLK, LPTIM1_OUT, I2C1_SMBA, USART2_TX, LPUART1_TX | - |
| - | - | 23 | 23 | 25 | 25 | 38 | PA15 | I/O | FT | - | SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1 | -- |
| - | B2 | 24 | 24 | 26 | 26 | 39 | PB3 | I/O | FT | - | SPI1_SCK, TIM2_CH2, EVENTOUT | COMP2_INN |
| - | - | - | 25 | 27 | 27 | 40 | PB4 | I/O | FT | - | SPI1_MISO, EVENTOUT, TIM22_CH1 | COMP2_INP |
| - | - | - | 26 | 28 | 28 | 41 | PB5 | I/O | FT | - | SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM22_CH2 | COMP2_INP |
| - | A3 | 25 | 27 | 29 | 29 | 42 | PB6 | I/O | FTf | - | USART2_TX, I2C1_SCL, LPTIM1_ETR, TIM21_CH1 | COMP2_INP |
| - | A4 | 26 | 28 | 30 | 30 | 43 | PB7 | I/O | FTf | - | USART2_RX, I2C1_SDA, LPTIM1_IN2 | COMP2_INP, VREF_PVD_IN |

## 6.3 Operating conditions

### 6.3.1 General operating conditions

**Table 20. General operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | - | 0 | 32 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | - | 0 | 32 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | - | 0 | 32 | |
| $V_{DD}$ | Standard operating voltage | BOR detector disabled | 1.65 | 3.6 | V |
| | | BOR detector enabled, at power on | 1.8 | 3.6 | |
| | | BOR detector disabled, after power on | 1.65 | 3.6 | |
| $V_{DDA}$ | Analog operating voltage (all features) | Must be the same voltage as $V_{DD}$(1) | 1.65 | 3.6 | V |
| $V_{IN}$ | Input voltage on FT, FTf and RST pins(2) | 2.0 V ≤ $V_{DD}$ ≤ 3.6 V | -0.3 | 5.5 | V |
| | | 1.65 V ≤ $V_{DD}$ ≤ 2.0 V | -0.3 | 5.2 | |
| | Input voltage on BOOT0 pin | - | 0 | 5.5 | |
| | Input voltage on TC pin | - | -0.3 | $V_{DD}$+0.3 | |
| $P_D$ | Power dissipation at $T_A$ = 85 °C (range 6) or $T_A$ =105 °C (rage 7) (3) | LQFP48 package | - | 351 | mW |
| | | LQFP32 package | - | 333 | |
| | | UFQFPN32 package | - | 513 | |
| | | UFQFPN28 package | - | 167 | |
| | | WLCSP25 package | - | 286 | |
| | | TSSOP20 package | - | 333 | |
| | Power dissipation at $T_A$ = 125 °C (range 3) (3) | LQFP48 package | - | 88 | |
| | | LQFP32 package | - | 83 | |
| | | UFQFPN32 package | - | 128 | |
| | | UFQFPN28 package | - | 42 | |
| | | WLCSP25 package | - | 71 | |
| | | TSSOP20 package | - | 83 | |

### 6.3.3 Embedded internal reference voltage

The parameters given in *Table 23* are based on characterization results, unless otherwise specified.

**Table 22. Embedded internal reference voltage calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| VREFINT_CAL | Raw data acquired at temperature of 25 °C, $V_{DDA}$= 3 V | 0x1FF8 0078 - 0x1FF8 0079 |

**Table 23. Embedded internal reference voltage(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT\ out}$(2) | Internal reference voltage | – 40 °C < $T_J$ < +125 °C | 1.202 | 1.224 | 1.242 | V |
| $T_{VREFINT}$ | Internal reference startup time | - | - | 2 | 3 | ms |
| $V_{VREF\_MEAS}$ | $V_{DDA}$ voltage during $V_{REFINT}$ factory measure | - | 2.99 | 3 | 3.01 | V |
| $A_{VREF\_MEAS}$ | Accuracy of factory-measured $V_{REFINT}$ value(3) | Including uncertainties due to ADC and $V_{DDA}$ values | - | - | ±5 | mV |
| $T_{Coeff}$(4) | Temperature coefficient | –40 °C < $T_J$ < +125 °C | - | 25 | 100 | ppm/°C |
| $A_{Coeff}$(4) | Long-term stability | 1000 hours, T= 25 °C | - | - | 1000 | ppm |
| $V_{DDCoeff}$(4) | Voltage coefficient | 3.0 V < $V_{DDA}$ < 3.6 V | - | - | 2000 | ppm/V |
| $T_{S\_vrefint}$(4)(5) | ADC sampling time when reading the internal reference voltage | - | 5 | 10 | - | µs |
| $T_{ADC\_BUF}$(4) | Startup time of reference voltage buffer for ADC | - | - | - | 10 | µs |
| $I_{BUF\_ADC}$(4) | Consumption of reference voltage buffer for ADC | - | - | 13.5 | 25 | µA |
| $I_{VREF\_OUT}$(4) | VREF_OUT output current(6) | - | - | - | 1 | µA |
| $C_{VREF\_OUT}$(4) | VREF_OUT output load | - | - | - | 50 | pF |
| $I_{LPBUF}$(4) | Consumption of reference voltage buffer for VREF_OUT and COMP | - | - | 730 | 1200 | nA |
| $V_{REFINT\_DIV1}$(4) | 1/4 reference voltage | - | 24 | 25 | 26 | % $V_{REFINT}$ |
| $V_{REFINT\_DIV2}$(4) | 1/2 reference voltage | - | 49 | 50 | 51 | |
| $V_{REFINT\_DIV3}$(4) | 3/4 reference voltage | - | 74 | 75 | 76 | |

1. Refer to *Table 35: Peripheral current consumption in Stop and Standby mode* for the value of the internal reference current consumption ($I_{REFINT}$).
2. Guaranteed by test in production.
3. The internal $V_{REF}$ value is individually measured in production and stored in dedicated EEPROM bytes.
4. Guaranteed by design.
5. Shortest sampling time can be determined in the application by multiple iterations.
6. To guarantee less than 1% VREF_OUT deviation.

**Table 24. Current consumption in Run mode, code with data processing running from Flash memory**

| Symbol | Parameter | Conditions | | $f_{HCLK}$ | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (Run from Flash) | Supply current in Run mode, code executed from Flash | $f_{HSE}$ = $f_{HCLK}$ up to 16 MHz included, $f_{HSE}$ = $f_{HCLK}$/2 above 16 MHz (PLL on)(2) | Range 3, $V_{CORE}$=1.2 V VOS[1:0]=11 | 1 MHz | 140 | 200 | µA |
| | | | | 2 MHz | 245 | 310 | |
| | | | | 4 MHz | 460 | 540 | |
| | | | Range 2, $V_{CORE}$=1.5 V, VOS[1:0]=10, | 4 MHz | 0.56 | 0.63 | mA |
| | | | | 8 MHz | 1.1 | 1.2 | |
| | | | | 16 MHz | 2.1 | 2.3 | |
| | | | Range 1, $V_{CORE}$=1.8 V, VOS[1:0]=01 | 8 MHz | 1.25 | 1.4 | |
| | | | | 16 MHz | 2.5 | 2.7 | |
| | | | | 32 MHz | 5 | 5.6 | |
| | | HSI clock | Range 2, $V_{CORE}$=1.5 V, VOS[1:0]=10, | 16 MHz | 2.1 | 2.4 | |
| | | | Range 1, $V_{CORE}$=1.8 V, VOS[1:0]=01 | 32 MHz | 5.1 | 5.7 | |
| | | MSI clock | Range 3, $V_{CORE}$=1.2 V, VOS[1:0]=11 | 65 kHz | 34.5 | 110 | µA |
| | | | | 524 kHz | 86 | 150 | |
| | | | | 4.2 MHz | 505 | 570 | |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

**Table 25. Current consumption in Run mode vs code type, code with data processing running from Flash memory**

| Symbol | Parameter | Conditions | | | $f_{HCLK}$ | Typ | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (Run from Flash) | Supply current in Run mode, code executed from Flash memory | $f_{HSE}$ = $f_{HCLK}$ up to 16 MHz included, $f_{HSE}$ = $f_{HCLK}$/2 above 16 MHz (PLL ON)(1) | Range 3, $V_{CORE}$=1.2 V, VOS[1:0]=11 | Dhrystone | 4 MHz | 460 | µA |
| | | | | CoreMark | | 455 | |
| | | | | Fibonacci | | 330 | |
| | | | | while(1) | | 305 | |
| | | | | while(1), prefetch OFF | | 320 | |
| | | | Range 1, VOS[1:0]=01, $V_{CORE}$=1.8 V | Dhrystone | 32 MHz | 5 | mA |
| | | | | CoreMark | | 5.15 | |
| | | | | Fibonacci | | 5 | |
| | | | | while(1) | | 4.35 | |
| | | | | while(1), prefetch OFF | | 3.85 | |

1. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

**Table 29. Current consumption in Low-power run mode**

| Symbol | Parameter | Conditions | | | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (LP Run) | Supply current in Low-power run mode | All peripherals off, code executed from RAM, Flash memory OFF, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz | $T_A$ = -40 °C to 25 °C | 6.3 | 8.4 | µA |
| | | | | $T_A$ = 85 °C | 9.15 | 13 | |
| | | | | $T_A$ = 105 °C | 12.5 | 19 | |
| | | | | $T_A$ = 125 °C | 20.5 | 36 | |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 65 kHz | $T_A$ =-40 °C to 25 °C | 9.45 | 12 | |
| | | | | $T_A$ = 85 °C | 12.5 | 15 | |
| | | | | $T_A$ = 105 °C | 16 | 22 | |
| | | | | $T_A$ = 125 °C | 24 | 38 | |
| | | | MSI clock, 131 kHz $f_{HCLK}$ = 131 kHz | $T_A$ = -40 °C to 25 °C | 17 | 20 | |
| | | | | $T_A$ = 55 °C | 19 | 21 | |
| | | | | $T_A$ = 85 °C | 20.5 | 24 | |
| | | | | $T_A$ = 105 °C | 23.5 | 28 | |
| | | | | $T_A$ = 125 °C | 31.5 | 46 | |
| | | All peripherals off, code executed from Flash memory, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz | $T_A$ = -40 °C to 25 °C | 18.5 | 23 | |
| | | | | $T_A$ = 85 °C | 23 | 27 | |
| | | | | $T_A$ = 105 °C | 27 | 33 | |
| | | | | $T_A$ = 125 °C | 36 | 52 | |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 65 kHz | $T_A$ = -40 °C to 25 °C | 22.5 | 26 | |
| | | | | $T_A$ = 85 °C | 27.5 | 31 | |
| | | | | $T_A$ = 105 °C | 31 | 38 | |
| | | | | $T_A$ = 125 °C | 40.5 | 56 | |
| | | | MSI clock, 131 kHz $f_{HCLK}$ = 131 kHz | $T_A$ = -40 °C to 25 °C | 32 | 36 | |
| | | | | $T_A$ = 55 °C | 35 | 37 | |
| | | | | $T_A$ = 85 °C | 37.5 | 42 | |
| | | | | $T_A$ = 105 °C | 41 | 47 | |
| | | | | $T_A$ = 125 °C | 50 | 65 | |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

### Low-speed external user clock generated from an external source

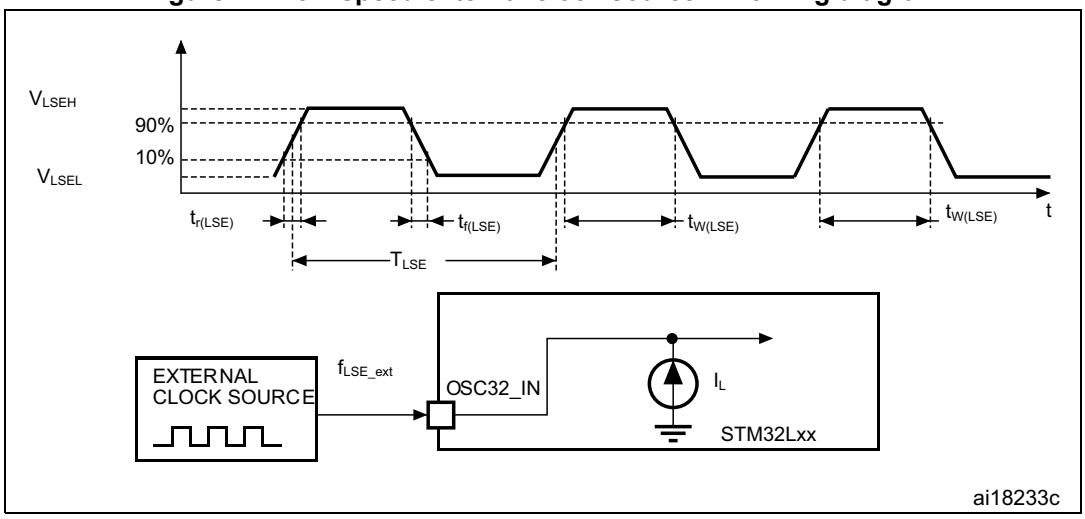
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 20*.

**Table 38. Low-speed external user clock characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE\_ext}$ | User external clock source frequency | - | 1 | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(LSE)}$ $t_{w(LSE)}$ | OSC32_IN high or low time | | 465 | - | - | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time | | - | - | 10 | |
| $C_{IN(LSE)}$ | OSC32_IN input capacitance | - | - | 0.6 | - | pF |
| $DuCy_{(LSE)}$ | Duty cycle | - | 45 | - | 55 | % |
| $I_L$ | OSC32_IN Input leakage current | $V_{SS} \le V_{IN} \le V_{DD}$ | - | - | ±1 | µA |

1. Guaranteed by design.

**Figure 21. Low-speed external clock source AC timing diagram**



### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

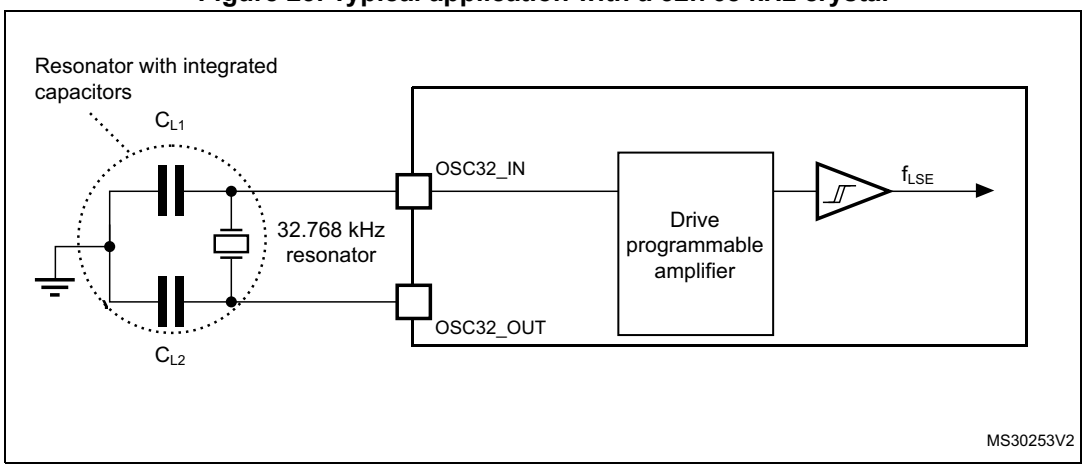
**Table 40. LSE oscillator characteristics(1)**

| Symbol | Parameter | Conditions(2) | Min(2) | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE}$ | LSE oscillator frequency | | - | 32.768 | - | kHz |
| $G_m$ | Maximum critical crystal transconductance | LSEDRV[1:0]=00 lower driving capability | - | - | 0.5 | µA/V |
| | | LSEDRV[1:0]= 01 medium low driving capability | - | - | 0.75 | |
| | | LSEDRV[1:0] = 10 medium high driving capability | - | - | 1.7 | |
| | | LSEDRV[1:0]=11 higher driving capability | - | - | 2.7 | |
| $t_{SU(LSE)}$(3) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | s |

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. Guaranteed by characterization results. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

*Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.*

**Figure 23. Typical application with a 32.768 kHz crystal**




*Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 49. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. $f_{OSC}/f_{CPU}$ | Unit |
|---|---|---|---|---|---|
| | | | | 8 MHz/32 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.6 V, $T_A$ = 25 °C, LQFP48 package conforming to IEC61967-2 | 0.1 to 30 MHz | -10 | dBµV |
| | | | 30 to 130 MHz | 5 | |
| | | | 130 MHz to 1GHz | -5 | |
| | | | EMI Level | 1.5 | - |

## 6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

**Table 50. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C, conforming to ANSI/JEDEC JS-001 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C, conforming to ANSI/ESD STM5.3.1. | C4 | 500 | |

1. Guaranteed by characterization results.

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

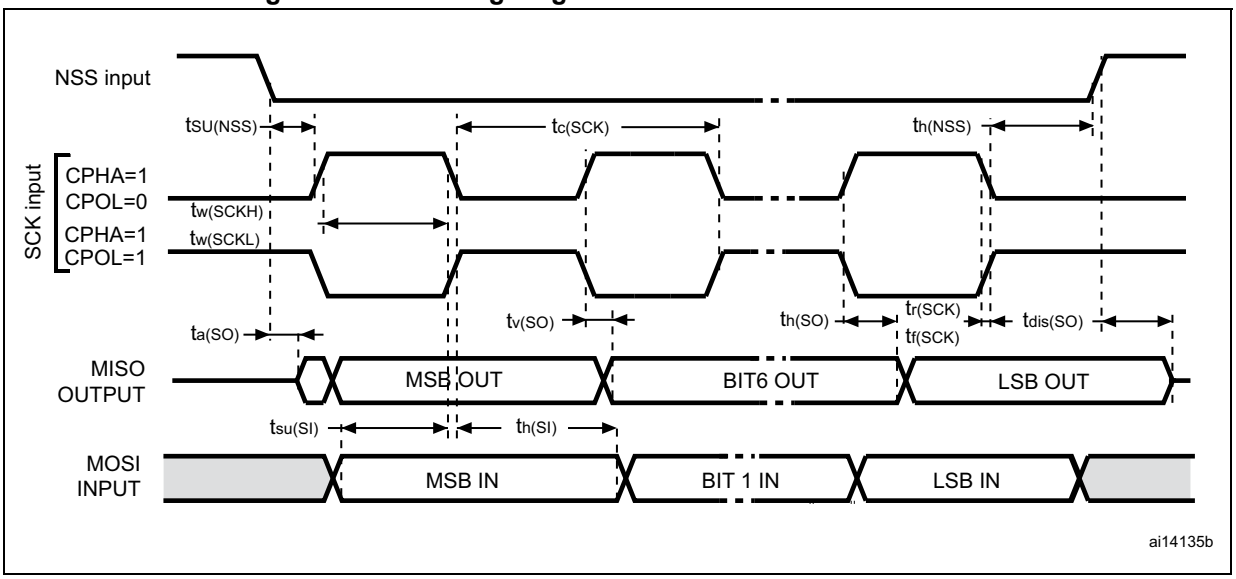
- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

**Table 68. SPI characteristics in voltage Range 2 (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$ $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | - | 8 | MHz |
| | | Slave mode Transmitter $1.65<V_{DD}<3.6V$ | | | 8 | |
| | | Slave mode Transmitter $2.7<V_{DD}<3.6V$ | | | 8(2) | |
| $Duty_{(SCK)}$ | Duty cycle of SPI clock frequency | Slave mode | 30 | 50 | 70 | % |
| $t_{su(NSS)}$ | NSS setup time | Slave mode, SPI presc = 2 | 4*Tpclk | - | - | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode, SPI presc = 2 | 2*Tpclk | - | - | |
| $t_{w(SCKH)}$ $t_{w(SCKL)}$ | SCK high and low time | Master mode | Tpclk-2 | Tpclk | Tpclk+2 | |
| $t_{su(MI)}$ | Data input setup time | Master mode | 12 | - | - | |
| $t_{su(SI)}$ | | Slave mode | 11 | - | - | |
| $t_{h(MI)}$ | Data input hold time | Master mode | 6.5 | - | - | |
| $t_{h(SI)}$ | | Slave mode | 2 | - | - | |
| $t_{a(SO}$ | Data output access time | Slave mode | 18 | - | 52 | |
| $t_{dis(SO)}$ | Data output disable time | Slave mode | 12 | - | 42 | |
| $t_{v(SO)}$ | Data output valid time | Slave mode | - | 40 | 55 | |
| | | Master mode | - | 16 | 26 | |
| $t_{v(MO)}$ | Data output hold time | Slave mode | 12 | - | - | |
| $t_{h(SO)}$ | | Master mode | 4 | - | - | |

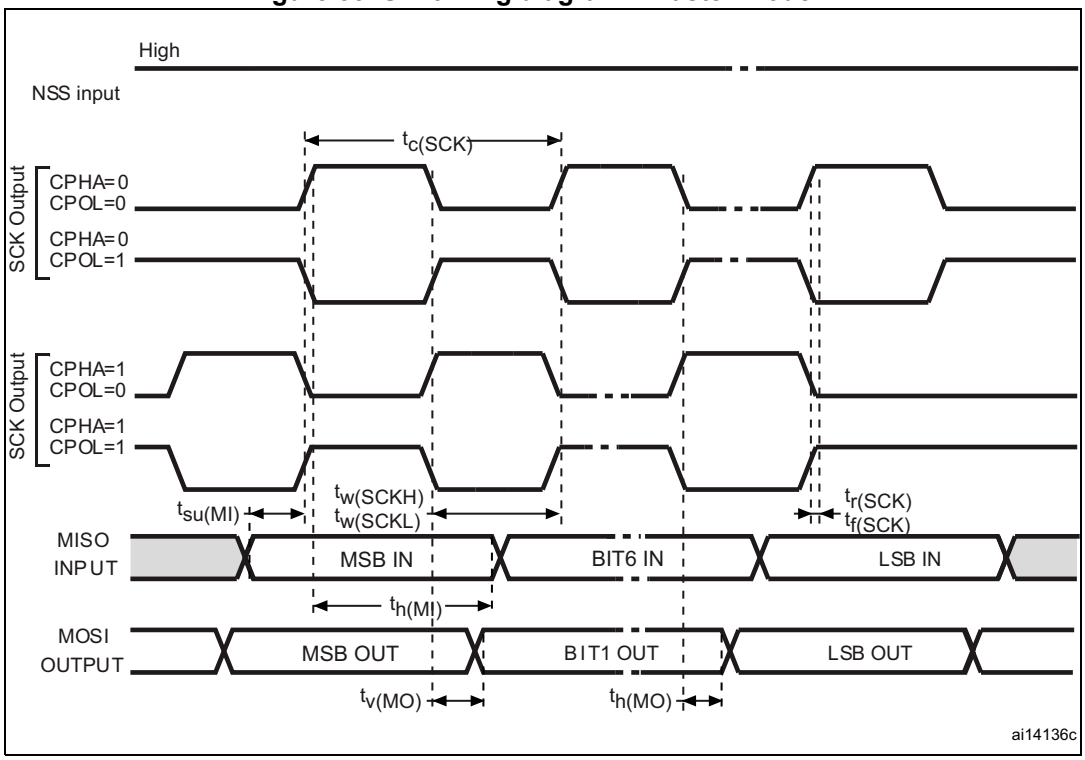
1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

**Figure 32. SPI timing diagram - slave mode and CPHA = 1(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Figure 33. SPI timing diagram - master mode(1)**



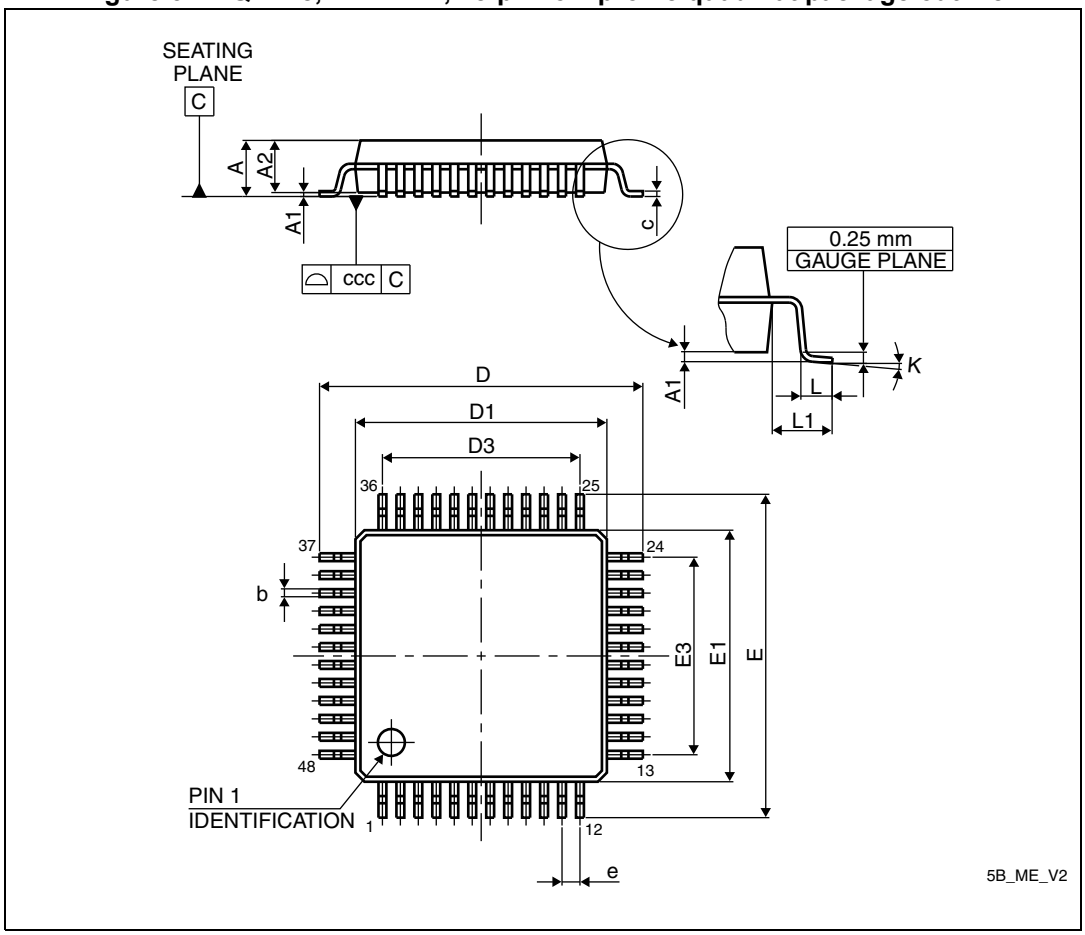

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status *are available at http://www.st.com.* ECOPACK® is an ST trademark.

## 7.1 LQFP48 package information

**Figure 34. LQFP48, 7 x 7 mm, 48-pin low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 70. LQFP48 - 48-pin low-profile quad flat package, 7 x 7 mm, package mechanical data**

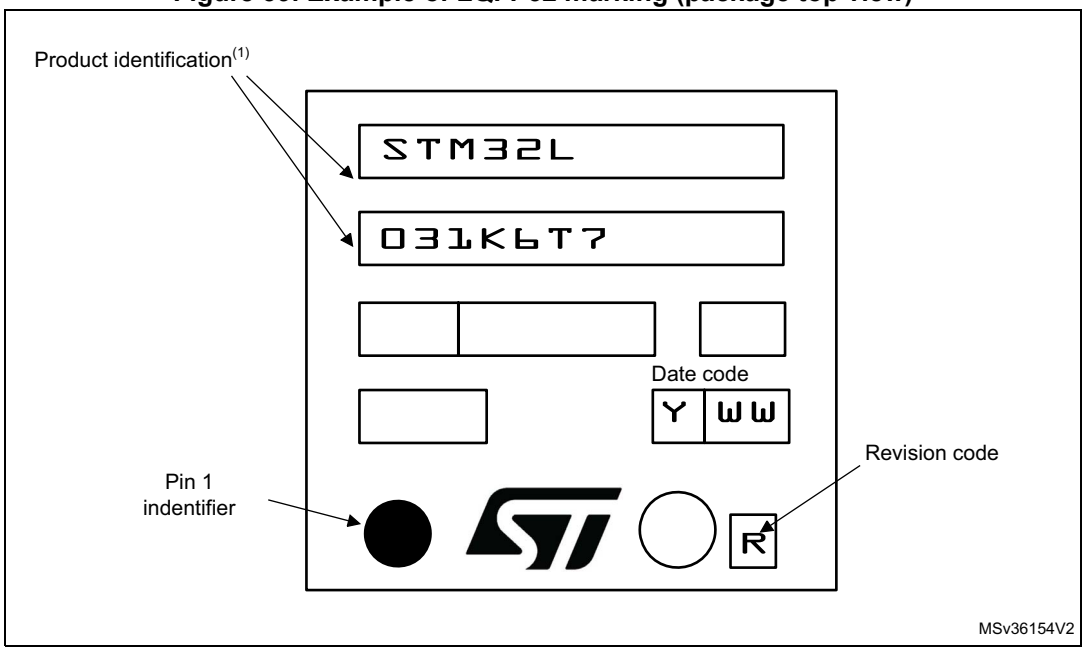
| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

### LQFP32 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

**Figure 39. Example of LQFP32 marking (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

# 8 Part numbering

**Table 78. STM32L031x4/6 ordering information scheme**

Example: STM32 L 031 K 6 T 6 D TR

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

L = Low power

Device subfamily

031 = Access line

Pin count

C = 48 pins
K = 32 pins
G = 28 pins
E = 25 pins
F = 20 pins

Flash memory size

4 = 16 Kbytes
6 = 32 Kbytes

Package

T = LQFP
U = UFQFPN
Y = WLCSP
P = TSSOP

Temperature range

6 = Industrial temperature range, –40 to 85 °C
7 = Industrial temperature range, –40 to 105 °C
3 = Industrial temperature range, –40 to 125 °C

Number of UFQFPN28 power pairs

S = one power pair(1)
No character = Two power pairs

Options

No character = $V_{DD}$ range: 1.8 to 3.6 V and BOR enabled
D = $V_{DD}$ range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel
No character = tray or tube

1. This option is available only on STM32L031GxUxS part number. Contact your nearest ST sales office for availability.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.