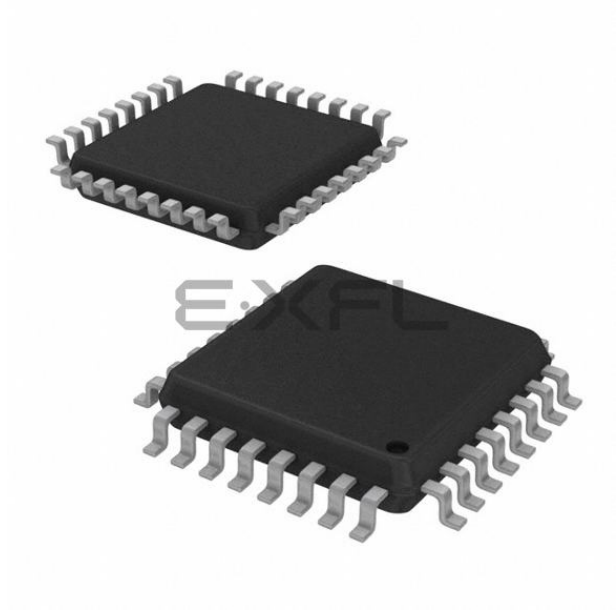

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l031k6t6

List of figures

2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM® Cortex®-M4, including ARM® Cortex®-M3 and ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 Ultra-low-power series are the best solution for applications such as gas/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

(if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USART/I2C/LPUART/LPTIMER wakeup events.

- **Stop mode without RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

  The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSE and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)(1)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
Consumption V_{DD}=1.8 to 3.6 V (Typ)	Down to 115 µA/MHz (from Flash)	Down to 25 µA/MHz (from Flash)	Down to 6.5 µA	Down to 3.2 µA	0.35 µA (No RTC) V_{DD}=1.8 V		0.23 µA (No RTC) V_{DD}=1.8 V	
					0.6 µA (with RTC) V_{DD}=1.8 V		0.39 µA (with RTC) V_{DD}=1.8 V	
					0.38 µA (No RTC) V_{DD}=3.0 V		0.26 µA (No RTC) V_{DD}=3.0 V	
					0.8 µA (with RTC) V_{DD}=3.0 V		0.57 µA (with RTC) V_{DD}=3.0 V	

1. Legend:
   "Y" = Yes (enable).
   "O" = Optional, can be enabled/disabled by software)
   "-" = Not available
2. Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.
3. UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start.To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.
4. I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

3.2 Interconnect matrix

Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

Table 6. STM32L0xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
COMPx	TIM2,TIM21, TIM22	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	-
	LPTIM	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	Y
TIMx	TIMx	Timer triggered by other timer	Y	Y	Y	Y	-

Table 6. STM32L0xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
RTC	TIM21	Timer triggered by Auto wake-up	Y	Y	Y	Y	-
	LPTIM	Timer triggered by RTC event	Y	Y	Y	Y	Y
All clock source	TIMx	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-
GPIO	TIMx	Timer input channel and trigger	Y	Y	Y	Y	-
	LPTIM	Timer input channel and trigger	Y	Y	Y	Y	Y
	ADC	Conversion trigger	Y	Y	Y	Y	-

3.3 ARM® Cortex®-M0+ core

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness.

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L031x4/6 are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L031x4/6 embed a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels and 4 priority levels.

3.5 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**

  To get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.

- **Safe clock switching**

  Clock sources can be changed safely on the fly in Run mode through a configuration register.

- **Clock management**

  To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.

- **System clock source**

  Three different clock sources can be used to drive the master clock SYSCLK:

  – 1-25 MHz high-speed external (HSE), that can supply a PLL
  – 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  – Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.

- **Auxiliary clock source**

  Two ultra-low-power clock sources that can be used to drive the real-time clock:

  – 32.768 kHz low-speed external crystal (LSE)
  – 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.

- **RTC clock sources**

  The LSI, LSE or HSE sources can be chosen to clock the RTC, whatever the system clock.

- **Startup clock**

  After reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.

- **Clock security system (CSS)**

  This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.

  Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.

- **Clock-out capability (MCO: microcontroller clock output)**

  It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

3.8 Memories

The STM32L031x4/6 devices have the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 16 or 32 Kbytes of embedded Flash program memory
  - 1 Kbytes of data EEPROM
  - Information block containing 32 user and factory options bytes plus 4 Kbytes of system memory

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0**: no protection
- **Level 1**: memory readout protected.

  The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2**: chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.9 Direct memory access (DMA)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, LPUART, general-purpose timers, and ADC.

3.10 Analog-to-digital converter (ADC)

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L031x4/6 devices. It has up to 10 external channels and 3 internal channels (temperature sensor, voltage reference). Three channel are fast channel, PA0, PA4 and PA5, while the others are standard channels.

It performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 MSPS even with a low CPU speed. The ADC consumption is low at all frequencies (~25 µA at 10 kSPS, ~200 µA at 1MSPS). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers.

3.11 Temperature sensor

The temperature sensor (T_{SENSE}) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 7. Temperature sensor calibration values

Calibration value name	Description	Memory address
TSENSE_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3 V	0x1FF8 007A - 0x1FF8 007B
TSENSE_CAL2	TS ADC raw data acquired at temperature of 130 °C, V_{DDA}= 3 V	0x1FF8 007E - 0x1FF8 007F

3.11.1 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (since no external voltage, V_{REF+}, is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 8. Internal voltage reference measured values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C V_{DDA} = 3 V	0x1FF8 0078 - 0x1FF8 0079

3.14.1 General-purpose timers (TIM2, TIM21 and TIM22)

There are three synchronizable general-purpose timers embedded in the STM32L031x4/6 devices (see *Table 9* for differences).

TIM2

TIM2 is based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM2 general-purpose timers can work together or with the TIM21 and TIM22 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2 has independent DMA request generation.

This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM21 and TIM22

TIM21 and TIM22 are based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. They have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together and be synchronized with the TIM2, full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

3.14.2 Low-power Timer (LPTIM)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one shot mode
- Selectable software / hardware input trigger
- Selectable clock source
  - Internal clock source: LSE, LSI, HSI or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

3.14.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches ‘0’.

Table 15. Pin definitions (continued)

Pin Number							Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP25[1]	UFQFPN28	UFQFPN28 (STM32L031GxUxS only)	LQFP32	UFQFPN32[2]	LQFP48						
13	C3	13	13	13	13	17	PA7	I/O	FT	-	SPI1_MOSI, LPTIM1_OUT, USART2_CTS, TIM22_CH2, EVENTOUT, COMP2_OUT	ADC_IN7
-	E2	14	14	14	14	18	PB0	I/O	FT	-	EVENTOUT, SPI1_MISO, USART2_RTS, TIM2_CH3	ADC_IN8, VREF_OUT
14	D2	15	15	15	15	19	PB1	I/O	FT	-	USART2_CK, SPI1_MOSI, LPUART1_RTS, TIM2_CH4	ADC_IN9, VREF_OUT
-	-	-	-	-	16	20	PB2	I/O	FT	-	LPTIM1_OUT	-
-	-	-	-	-	-	21	PB10	I/O	FT	-	TIM2_CH3, LPUART1_TX	-
-	-	-	-	-	-	22	PB11	I/O	FT	-	EVENTOUT, TIM2_CH4, LPUART1_RX	-
15	-	16	16	16	-	23	VSS	S	-	-	-	-
16	-	17	17	17	17	24	VDD	S	-	-	-	-
-	-	-	-	-	-	25	PB12	I/O	FT	-	SPI1_NSS, EVENTOUT	-
-	-	-	-	-	-	26	PB13	I/O	FT	-	SPI1_SCK, MCO, TIM21_CH1, LPUART1_CTS	-

Table 16. Alternate functions

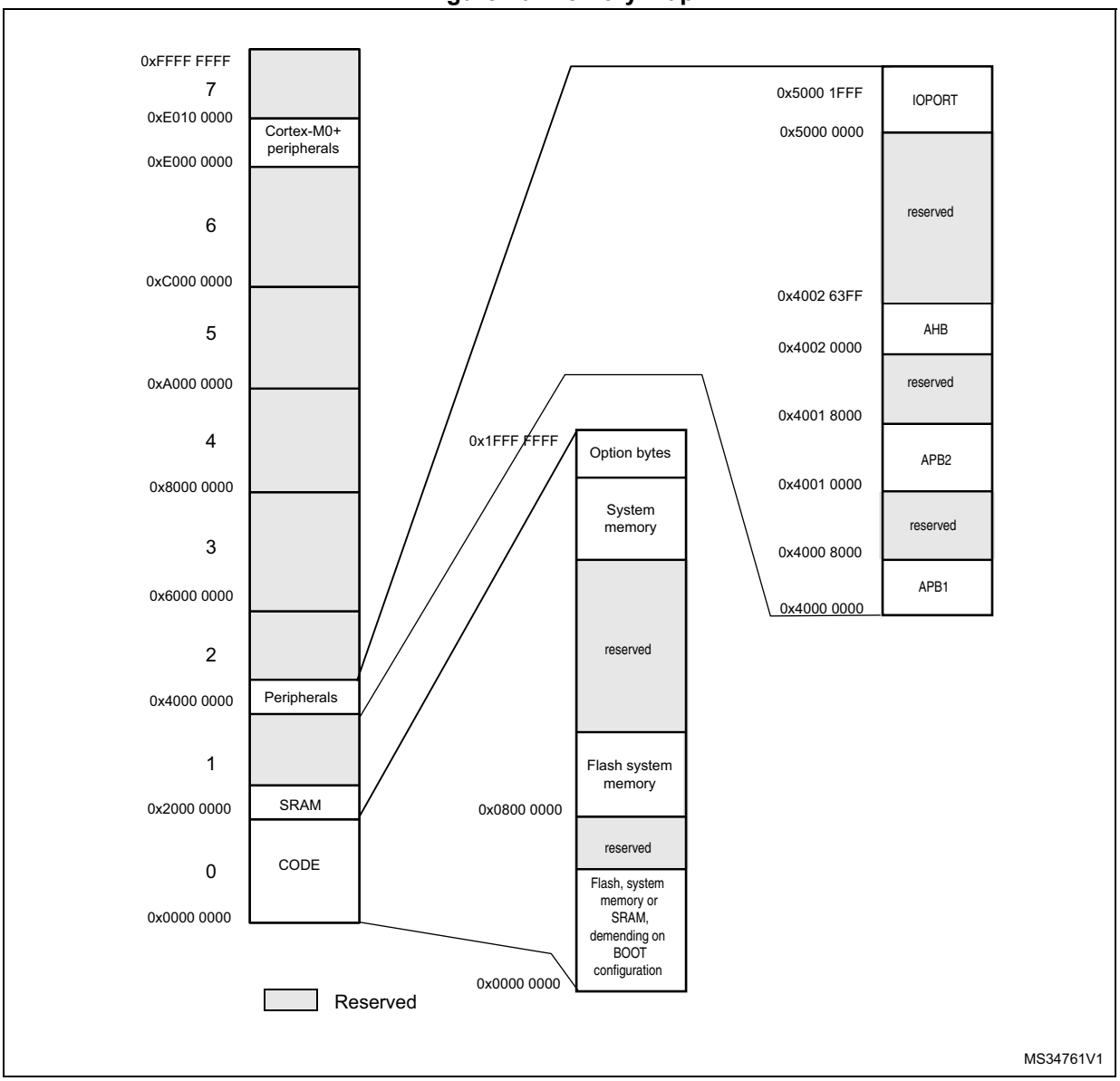
Ports		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/USART2 /LPTIM/TIM21 /EVENTOUT/ SYS_AF	SPI1/I2C1/ LPTIM	LPTIM/TIM2/ EVENTOUT/ SYS_AF	I2C1/ EVENTOUT	I2C1/USART2/ LPUART1/ TIM22/ EVENTOUT	TIM2/21/22	LPUART1/ EVENTOUT	COMP1/2
Port A	PA0	-	LPTIM1_IN1	TIM2_CH1	-	USART2_CTS	TIM2_ETR	-	COMP1_OUT
	PA1	EVENTOUT	LPTIM1_IN2	TIM2_CH2	I2C1_SMBA	USART2_RTS	TIM21_ETR	-	-
	PA2	TIM21_CH1	-	TIM2_CH3	-	USART2_TX	-	LPUART1_TX	COMP2_OUT
	PA3	TIM21_CH2	-	TIM2_CH4	-	USART2_RX	-	LPUART1_RX	
	PA4	SPI1_NSS	LPTIM1_IN1	-	-	USART2_CK	TIM22_ETR	-	-
	PA5	SPI1_SCK	LPTIM1_IN2	TIM2_ETR	-	-	TIM2_CH1	-	-
	PA6	SPI1_MISO	LPTIM1_ETR	-	-	LPUART1_CTS	TIM22_CH1	EVENTOUT	COMP1_OUT
	PA7	SPI1_MOSI	LPTIM1_OUT	-	-	USART2_CTS	TIM22_CH2	EVENTOUT	COMP2_OUT
	PA8	MCO	-	LPTIM1_IN1	EVENTOUT	USART2_CK	TIM2_CH1	-	-
	PA9	MCO	I2C1_SCL	-	-	USART2_TX	TIM22_CH1	-	-
	PA10	-	I2C1_SDA	-	-	USART2_RX	TIM22_CH2	-	-
	PA11	SPI1_MISO	-	EVENTOUT	-	USART2_CTS	TIM21_CH2	-	COMP1_OUT
	PA12	SPI1_MOSI	-	EVENTOUT	-	USART2_RTS	-	-	COMP2_OUT
	PA13	SWDIO	LPTIM1_ETR	-	-	-	-	LPUART1_RX	-
	PA14	SWCLK	LPTIM1_OUT	-	I2C1_SMBA	USART2_TX	-	LPUART1_TX	-
	PA15	SPI1_NSS	-	TIM2_ETR	EVENTOUT	USART2_RX	TIM2_CH1	-	-

Table 16. Alternate functions (continued)

Ports		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/USART2 /LPTIM/TIM21 /EVENTOUT/ SYS_AF	SPI1/I2C1/ LPTIM	LPTIM/TIM2/ EVENTOUT/ SYS_AF	I2C1/ EVENTOUT	I2C1/USART2/ LPUART1/ TIM22/ EVENTOUT	TIM2/21/22	LPUART1/ EVENTOUT	COMP1/2
Port B	PB0	EVENTOUT	SPI1_MISO	-	-	USART2_RTS	TIM2_CH3	-	-
	PB1	USART2_CK	SPI1_MOSI	-	-	LPUART1_RTS	TIM2_CH4	-	-
	PB2	-	-	LPTIM1_OUT	-	-	-	-	-
	PB3	SPI1_SCK	-	TIM2_CH2	-	EVENTOUT	-	-	-
	PB4	SPI1_MISO	-	EVENTOUT	-	TIM22_CH1	-	-	-
	PB5	SPI1_MOSI	-	LPTIM1_IN1	I2C1_SMBA	TIM22_CH2	-	-	-
	PB6	USART2_TX	I2C1_SCL	LPTIM1_ETR	-	-	TIM21_CH1	-	-
	PB7	USART2_RX	I2C1_SDA	LPTIM1_IN2	-	-	-	-	-
	PB8	-	-	-	-	I2C1_SCL	-	-	-
	PB9	-	-	EVENTOUT	-	I2C1_SDA	-	-	-
	PB10	-	-	TIM2_CH3	-	-	-	LPUART1_TX	-
	PB11	EVENTOUT	-	TIM2_CH4	-	-	-	LPUART1_RX	-
	PB12	SPI1_NSS	-	-	-	-	-	EVENTOUT	-
	PB13	SPI1_SCK	-	MCO	-	-	TIM21_CH1	LPUART1_CTS	-
	PB14	SPI1_MISO	-	RTC_OUT	-	-	TIM21_CH2	LPUART1_RTS	-
	PB15	SPI1_MOSI	-	RTC_REFIN	-	-	-	-	-
Port C	PC0	LPTIM1_IN1	-	EVENTOUT	-	-	-	LPUART1_RX	-
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-

5 Memory mapping

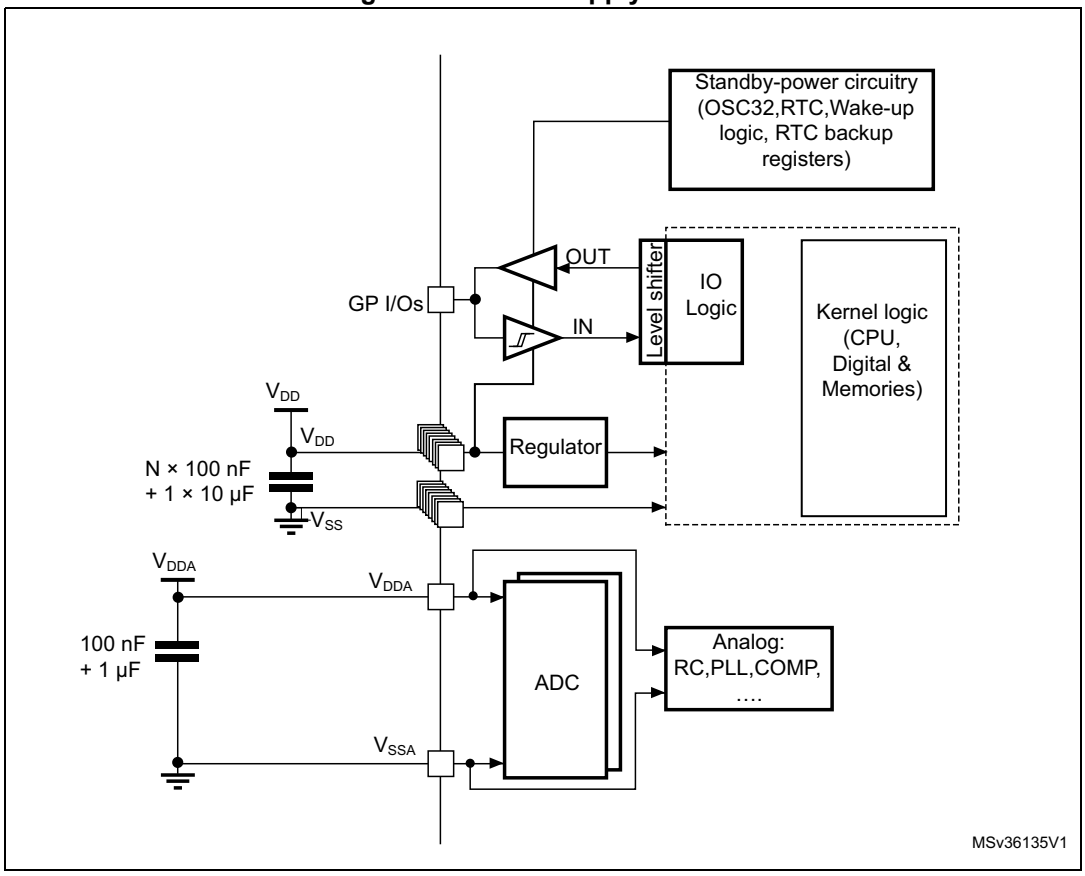
Figure 10. Memory map



1. Refer to the STM32L031x4/6 reference manual for details on the Flash memory organization for each memory size.

6.1.6 Power supply scheme

Figure 13. Power supply scheme



6.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme

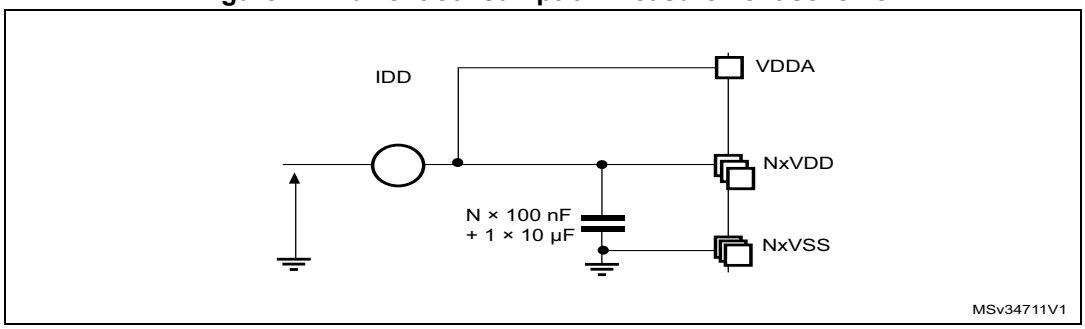


Table 18. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD} (2)	Total current into sum of all V_{DD} power lines (source)(1)	105	mA
ΣI_{VSS} (2)	Total current out of sum of all V_{SS} ground lines (sink)(1)	105	
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin except FTf pins	16	
	Output current sunk by FTf pins	22	
	Output current sourced by any I/O and control pin	-16	
$\Sigma I_{IO(PIN)}$ (3)	Total output current sunk by sum of all IOs and control pins(4)	45	
	Total output current sourced by sum of all IOs and control pins(4)	-45	
$\Sigma I_{IO(PIN)}$ (5)	Total output current sunk by sum of all IOs and control pins(2)	90	
	Total output current sourced by sum of all IOs and control pins(2)	-90	
$I_{INJ(PIN)}$	Injected current on FT, FFf, RST and B pins	-5/+0(6)	
	Injected current on TC pin	± 5(7)	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(8)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. These values apply only to STM32L031GxUxS part number.
4. This current consumption must be correctly distributed over all I/Os and control pins. In particular, it must be located the closest possible to the couple of supply and ground, and distributed on both sides.
5. These values apply to all part numbers except for STM32L031GxUxS.
6. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 17* for maximum allowed input voltage values.
7. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 17: Voltage characteristics* for the maximum allowed input voltage values.
8. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 19. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

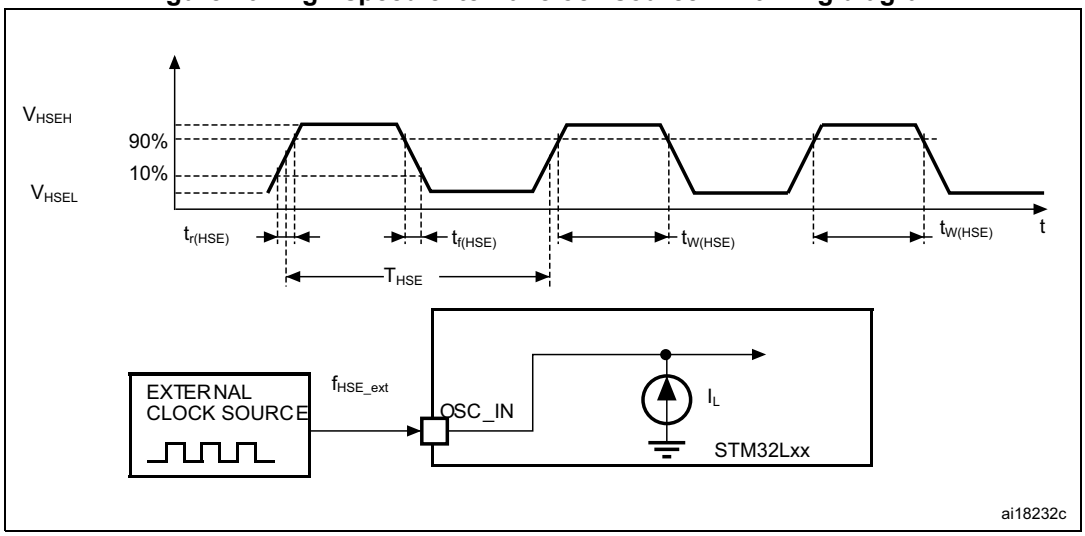
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.The external clock signal has to respect the I/O characteristics in *Section 6.3.12*. However, the recommended clock input waveform is shown in *Figure 20*.

Table 37. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0	8	32	MHz
V_{HSEH}	OSC_IN/CK_IN(2) input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN/CK_IN(2) input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN/CK_IN(2) high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN/CK_IN(2) rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN/CK_IN(2) input capacitance		-	2.6	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN/CK_IN(2) Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design.
2. HSE external user clock is applied to OSC_IN on LQFP48 package and to CK_IN on other packages.

Figure 20. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 20*.

Table 38. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 21. Low-speed external clock source AC timing diagram

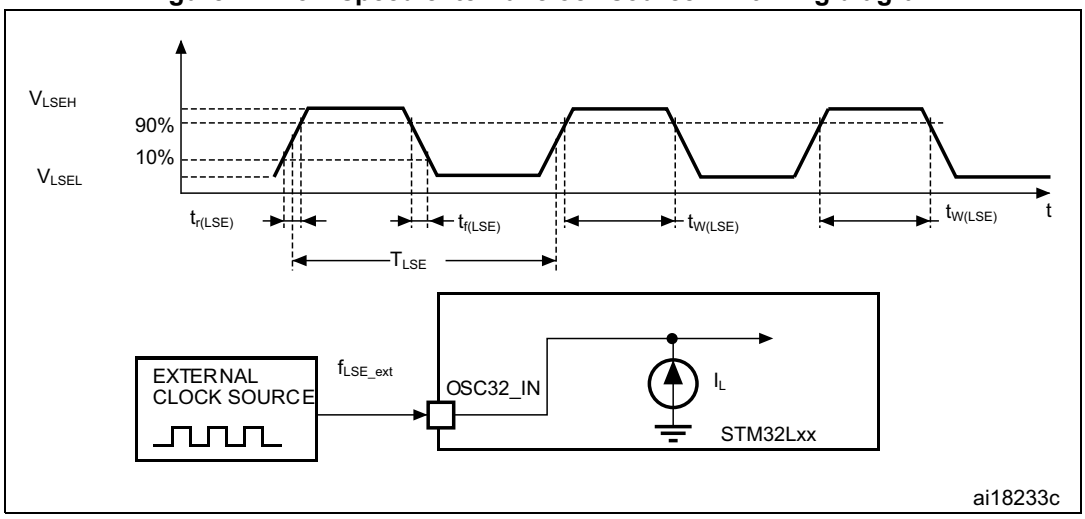


Table 70. LQFP48 - 48-pin low-profile quad flat package, 7 x 7 mm, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

8 Part numbering

Table 78. STM32L031x4/6 ordering information scheme

Example: STM32 L 031 K 6 T 6 D TR

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

L = Low power

Device subfamily

031 = Access line

Pin count

C = 48 pins
K = 32 pins
G = 28 pins
E = 25 pins
F = 20 pins

Flash memory size

4 = 16 Kbytes
6 = 32 Kbytes

Package

T = LQFP
U = UFQFPN
Y = WLCSP
P = TSSOP

Temperature range

6 = Industrial temperature range, –40 to 85 °C
7 = Industrial temperature range, –40 to 105 °C
3 = Industrial temperature range, –40 to 125 °C

Number of UFQFPN28 power pairs

S = one power pair(1)
No character = Two power pairs

Options

No character = V_{DD} range: 1.8 to 3.6 V and BOR enabled
D = V_{DD} range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel
No character = tray or tube

1. This option is available only on STM32L031GxUxS part number. Contact your nearest ST sales office for availability.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 79. Document revision history

Date	Revision	Changes
01-Feb-2016	3	Updated number of SPI interfaces on cover page and in *Table 2: Ultra-low-power STM32L031x4/x6 device features and peripheral counts*. Updated number of GPIOs for devices in UFQFPN28 in *Table 2: Ultra-low-power STM32L031x4/x6 device features and peripheral counts*. Updated *Section 3.4.4: Boot modes*. Updated *Section 3.15.2: Universal synchronous/asynchronous receiver transmitter (USART)* and *Section 3.15.4: Serial peripheral interface (SPI)* to mention the fact that USARTs with synchronous mode feature can be used as SPI master interfaces. Modified pin 2 in *Figure 5: STM32L031x4/6 UFQFPN32 pinout*. Added *Figure 7: STM32L031GxUxS UFQFPN28 pinout*. *Table 15: Pin definitions*: – Added UFQFPN28 for STM32L031GxUxS part number. – Renamed PA0-WKUP-CK_IN into PA0-CK_IN – Renamed PA0-WKUP into PA0 Updated *Table 18: Current characteristics* to add the total output current for STM32L031GxUxS. Added one power pair option in *Table 78: STM32L031x4/6 ordering information scheme*.