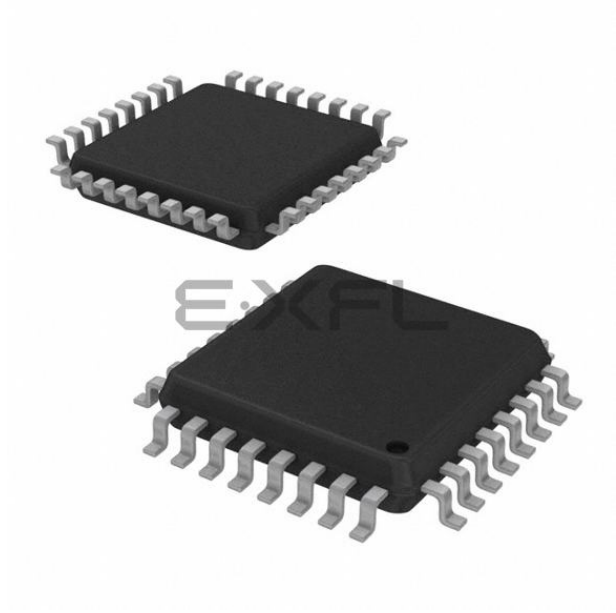

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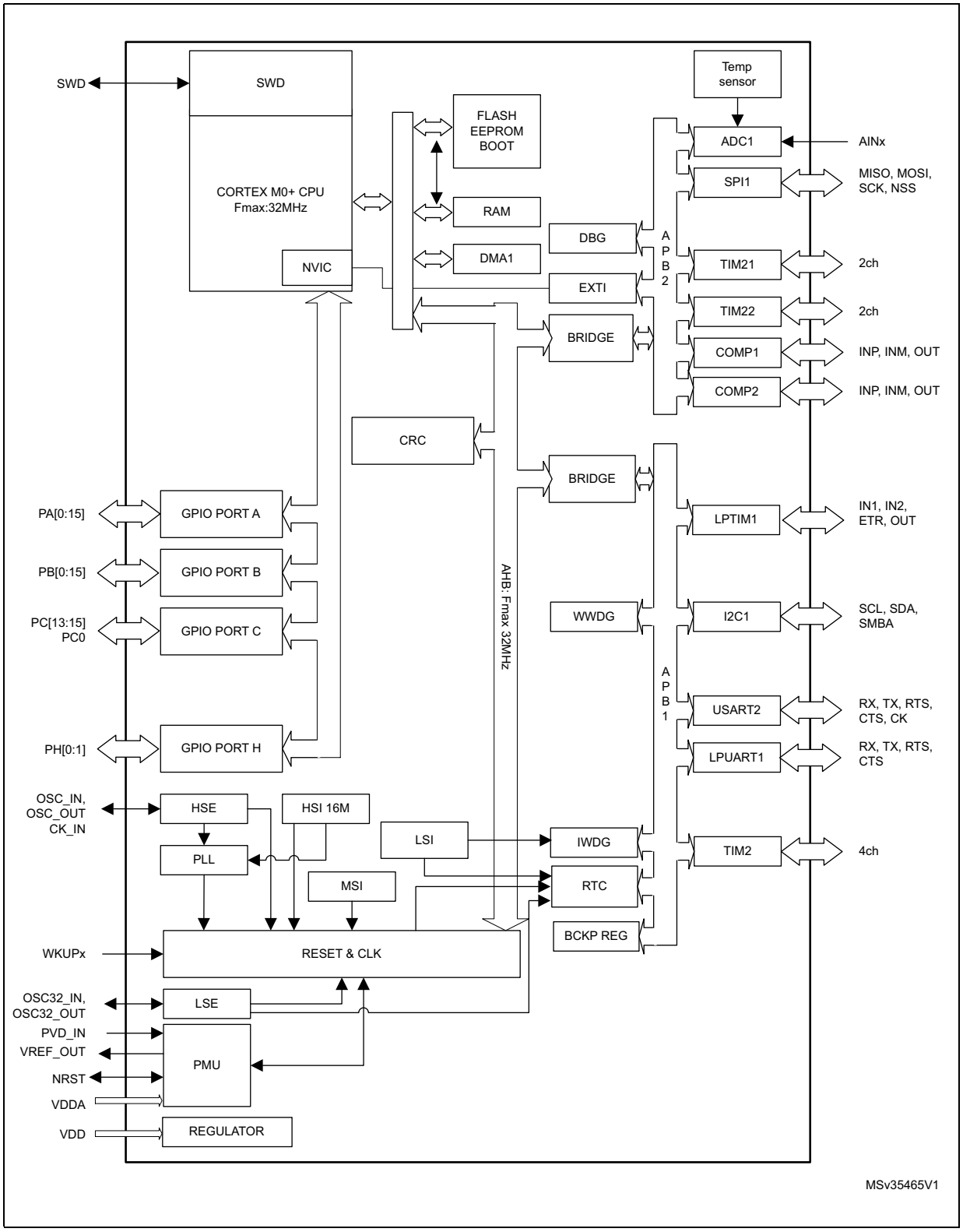
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l031k6t7

Figure 1. STM32L031x4/6 block diagram



3.12 Ultra-low-power comparators and reference voltage

The STM32L031x4/6 embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with ultra low consumption
- One comparator with rail-to-rail inputs, fast or slow mode.
- The threshold can be one of the following:
  - External I/O pins
  - Internal reference voltage (V_{REFINT})
  - submultiple of Internal reference voltage(1/4, 1/2, 3/4) for the rail to rail comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

3.13 System configuration controller

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM21, TIM22 and LPTIM timer input captures. It also controls the routing of internal analog signals to the ADC, COMP1 and COMP2 and the internal reference voltage V_{REFINT}.

3.14 Timers and watchdogs

The ultra-low-power STM32L031x4/6 devices include three general-purpose timers, one low- power timer (LPTM), two watchdog timers and the SysTick timer.

Table 9 compares the features of the general-purpose and basic timers.

Table 9. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No

the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.17 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Table 15. Pin definitions (continued)

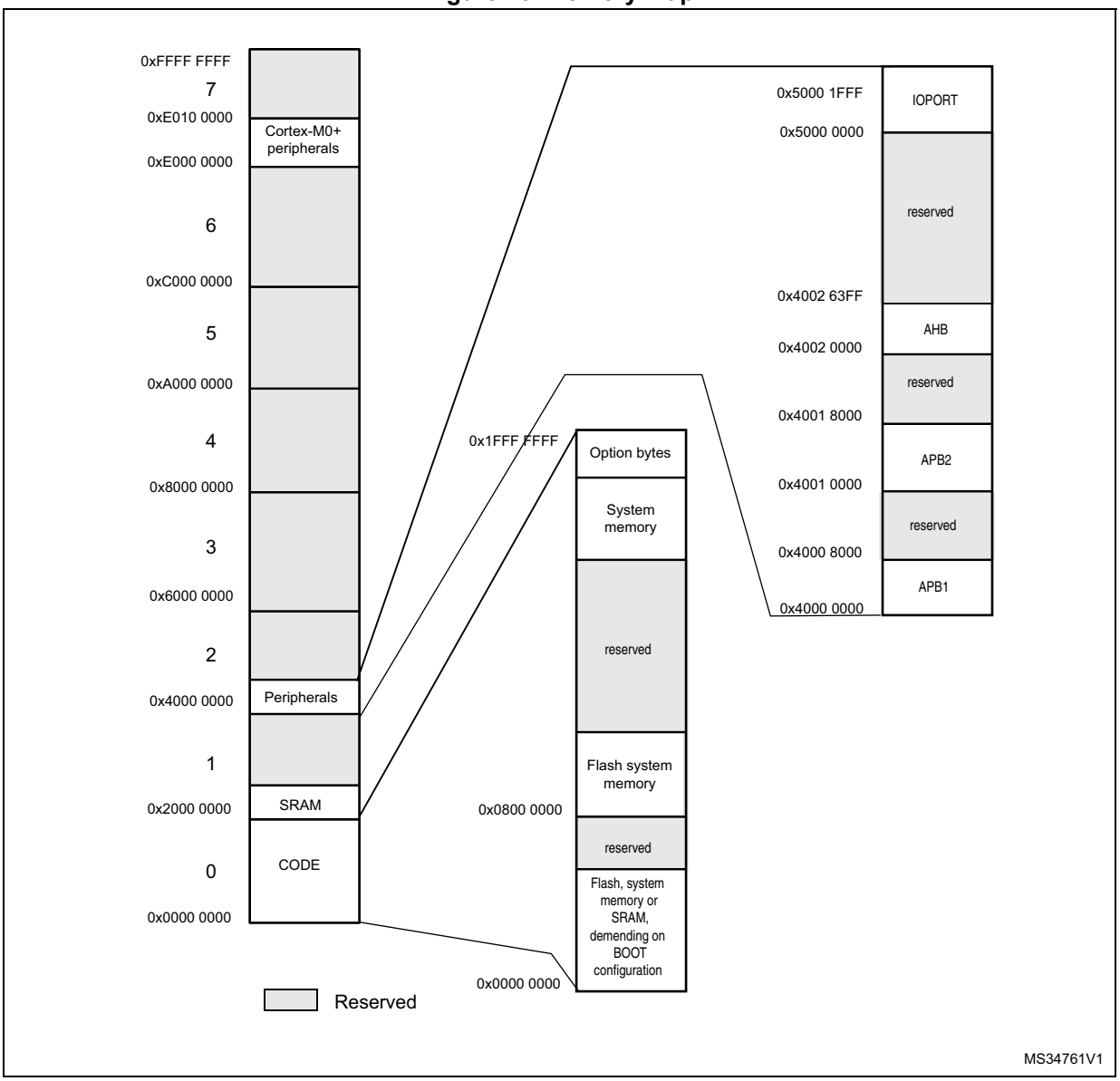
Pin Number							Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
TSSOP20	WLCSP25[1]	UFQFPN28	UFQFPN28 (STM32L031GxUxS only)	LQFP32	UFQFPN32[2]	LQFP48						
13	C3	13	13	13	13	17	PA7	I/O	FT	-	SPI1_MOSI, LPTIM1_OUT, USART2_CTS, TIM22_CH2, EVENTOUT, COMP2_OUT	ADC_IN7
-	E2	14	14	14	14	18	PB0	I/O	FT	-	EVENTOUT, SPI1_MISO, USART2_RTS, TIM2_CH3	ADC_IN8, VREF_OUT
14	D2	15	15	15	15	19	PB1	I/O	FT	-	USART2_CK, SPI1_MOSI, LPUART1_RTS, TIM2_CH4	ADC_IN9, VREF_OUT
-	-	-	-	-	16	20	PB2	I/O	FT	-	LPTIM1_OUT	-
-	-	-	-	-	-	21	PB10	I/O	FT	-	TIM2_CH3, LPUART1_TX	-
-	-	-	-	-	-	22	PB11	I/O	FT	-	EVENTOUT, TIM2_CH4, LPUART1_RX	-
15	-	16	16	16	-	23	VSS	S	-	-	-	-
16	-	17	17	17	17	24	VDD	S	-	-	-	-
-	-	-	-	-	-	25	PB12	I/O	FT	-	SPI1_NSS, EVENTOUT	-
-	-	-	-	-	-	26	PB13	I/O	FT	-	SPI1_SCK, MCO, TIM21_CH1, LPUART1_CTS	-

Table 16. Alternate functions (continued)

Ports		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/USART2 /LPTIM/TIM21 /EVENTOUT/ SYS_AF	SPI1/I2C1/ LPTIM	LPTIM/TIM2/ EVENTOUT/ SYS_AF	I2C1/ EVENTOUT	I2C1/USART2/ LPUART1/ TIM22/ EVENTOUT	TIM2/21/22	LPUART1/ EVENTOUT	COMP1/2
Port B	PB0	EVENTOUT	SPI1_MISO	-	-	USART2_RTS	TIM2_CH3	-	-
	PB1	USART2_CK	SPI1_MOSI	-	-	LPUART1_RTS	TIM2_CH4	-	-
	PB2	-	-	LPTIM1_OUT	-	-	-	-	-
	PB3	SPI1_SCK	-	TIM2_CH2	-	EVENTOUT	-	-	-
	PB4	SPI1_MISO	-	EVENTOUT	-	TIM22_CH1	-	-	-
	PB5	SPI1_MOSI	-	LPTIM1_IN1	I2C1_SMBA	TIM22_CH2	-	-	-
	PB6	USART2_TX	I2C1_SCL	LPTIM1_ETR	-	-	TIM21_CH1	-	-
	PB7	USART2_RX	I2C1_SDA	LPTIM1_IN2	-	-	-	-	-
	PB8	-	-	-	-	I2C1_SCL	-	-	-
	PB9	-	-	EVENTOUT	-	I2C1_SDA	-	-	-
	PB10	-	-	TIM2_CH3	-	-	-	LPUART1_TX	-
	PB11	EVENTOUT	-	TIM2_CH4	-	-	-	LPUART1_RX	-
	PB12	SPI1_NSS	-	-	-	-	-	EVENTOUT	-
	PB13	SPI1_SCK	-	MCO	-	-	TIM21_CH1	LPUART1_CTS	-
	PB14	SPI1_MISO	-	RTC_OUT	-	-	TIM21_CH2	LPUART1_RTS	-
	PB15	SPI1_MOSI	-	RTC_REFIN	-	-	-	-	-
Port C	PC0	LPTIM1_IN1	-	EVENTOUT	-	-	-	LPUART1_RX	-
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-

5 Memory mapping

Figure 10. Memory map



1. Refer to the STM32L031x4/6 reference manual for details on the Flash memory organization for each memory size.

6.3.3 Embedded internal reference voltage

The parameters given in *Table 23* are based on characterization results, unless otherwise specified.

Table 22. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C, V_{DDA}= 3 V	0x1FF8 0078 - 0x1FF8 0079

Table 23. Embedded internal reference voltage(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$(2)	Internal reference voltage	– 40 °C < T_J < +125 °C	1.202	1.224	1.242	V
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REFINT} value(3)	Including uncertainties due to ADC and V_{DDA} values	-	-	±5	mV
T_{Coeff}(4)	Temperature coefficient	–40 °C < T_J < +125 °C	-	25	100	ppm/°C
A_{Coeff}(4)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(4)	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$(4)(5)	ADC sampling time when reading the internal reference voltage	-	5	10	-	µs
T_{ADC_BUF}(4)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(4)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(4)	VREF_OUT output current(6)	-	-	-	1	µA
C_{VREF_OUT}(4)	VREF_OUT output load	-	-	-	50	pF
I_{LPBUF}(4)	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}(4)	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}(4)	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}(4)	3/4 reference voltage	-	74	75	76	

1. Refer to *Table 35: Peripheral current consumption in Stop and Standby mode* for the value of the internal reference current consumption (I_{REFINT}).
2. Guaranteed by test in production.
3. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.
4. Guaranteed by design.
5. Shortest sampling time can be determined in the application by multiple iterations.
6. To guarantee less than 1% VREF_OUT deviation.

Table 24. Current consumption in Run mode, code with data processing running from Flash memory

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL on)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0]=11	1 MHz	140	200	µA
				2 MHz	245	310	
				4 MHz	460	540	
			Range 2, V_{CORE}=1.5 V, VOS[1:0]=10,	4 MHz	0.56	0.63	mA
				8 MHz	1.1	1.2	
				16 MHz	2.1	2.3	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	8 MHz	1.25	1.4	
				16 MHz	2.5	2.7	
				32 MHz	5	5.6	
		HSI clock	Range 2, V_{CORE}=1.5 V, VOS[1:0]=10,	16 MHz	2.1	2.4	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	32 MHz	5.1	5.7	
		MSI clock	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	65 kHz	34.5	110	µA
				524 kHz	86	150	
				4.2 MHz	505	570	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 25. Current consumption in Run mode vs code type, code with data processing running from Flash memory

Symbol	Parameter	Conditions			f_{HCLK}	Typ	Unit
I_{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash memory	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(1)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	460	µA
				CoreMark		455	
				Fibonacci		330	
				while(1)		305	
				while(1), prefetch OFF		320	
			Range 1, VOS[1:0]=01, V_{CORE}=1.8 V	Dhrystone	32 MHz	5	mA
				CoreMark		5.15	
				Fibonacci		5	
				while(1)		4.35	
				while(1), prefetch OFF		3.85	

1. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 35. Peripheral current consumption in Stop and Standby mode(1)

Symbol	Peripheral	Typical consumption, T_A = 25 °C		Unit
		V_{DD}=1.8 V	V_{DD}=3.0 V	
$I_{DD(PVD / BOR)}$	-	0.7	1.2	µA
I_{REFINT}	-	1.3	1.4	
-	LSE Low drive(2)	0.1	0.1	
-	LSI	0.27	0.31	
-	IWDG	0.2	0.3	
-	LPTIM1, Input 100 Hz	0.01	0.01	
-	LPTIM1, Input 1 MHz	6	6	
-	LPUART1	0.2	0.2	
-	RTC (LSE in Bypass mode)	0.2	0.2	

1. LPTIM, LPUART peripherals can operate in Stop mode but not in Standby mode
2. LSE Low drive consumption is the difference between an external clock on OSC32_IN and a quartz between OSC32_IN and OSC32_OUT.-

6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI or HSI16 RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is either the MSI oscillator in the range configured before entering Stop mode, the HSI16 or HSI16/4.
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

Low-speed external user clock generated from an external source

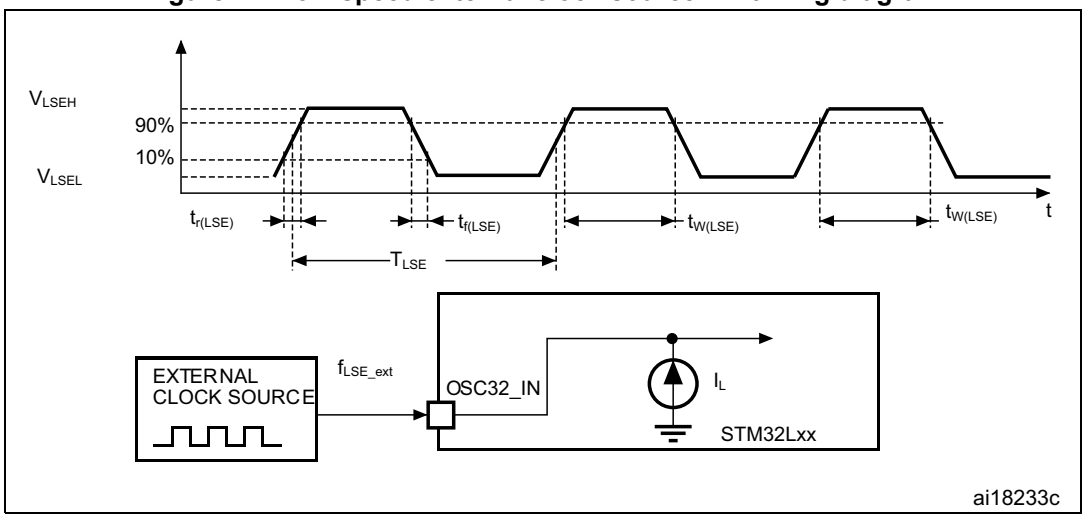
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 20*.

Table 38. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 21. Low-speed external clock source AC timing diagram



6.3.7 Internal clock source characteristics

The parameters given in *Table 41* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 20*.

High-speed internal 16 MHz (HSI16) RC oscillator

Table 41. 16 MHz HSI16 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
$TRIM^{(1)(2)}$	HSI16 user-trimmed resolution	Trimming code is not a multiple of 16	-	± 0.4	0.7	%
		Trimming code is a multiple of 16	-	-	± 1.5	%
$ACC_{HSI16}^{(2)}$	Accuracy of the factory-calibrated HSI16 oscillator	V_{DDA} = 3.0 V, T_A = 25 °C	-1(3)	-	1(3)	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V_{DDA} = 1.65 V to 3.6 V T_A = -40 to 125 °C	-5.45	-	3.25	%
$t_{SU(HSI16)}^{(2)}$	HSI16 oscillator startup time	-	-	3.7	6	µs
$I_{DD(HSI16)}^{(2)}$	HSI16 oscillator power consumption	-	-	100	140	µA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

Figure 24. HSI16 minimum and maximum value versus temperature

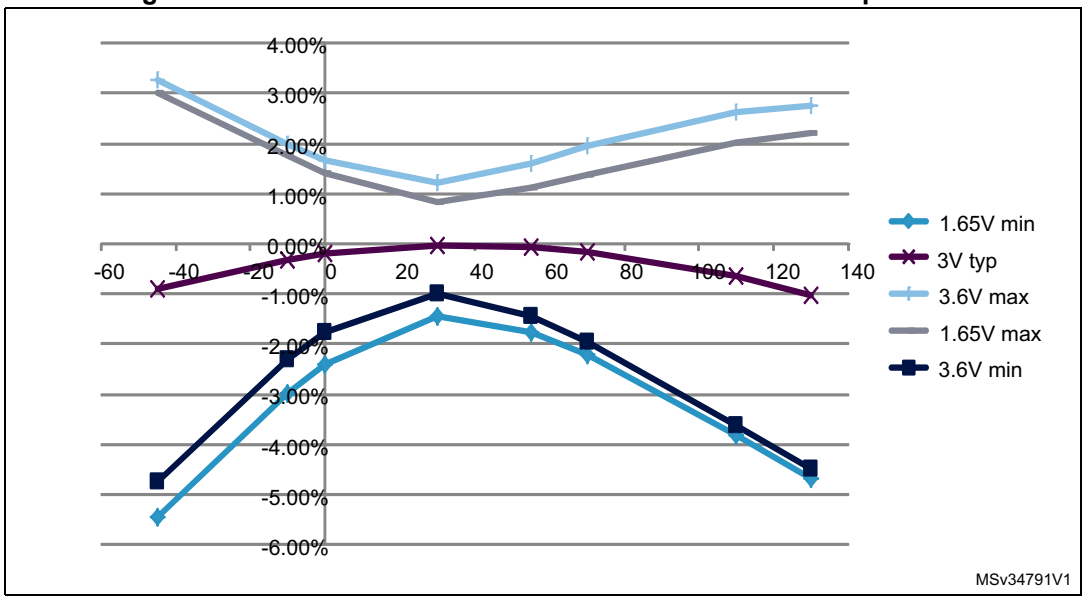


Table 44. PLL characteristics (continued)

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
f_{PLL_OUT}	PLL output clock	2	-	32	MHz
t_{LOCK}	PLL input = 16 MHz PLL VCO = 96 MHz	-	115	160	µs
Jitter	Cycle-to-cycle jitter	-		± 600	ps
I_{DDA}(PLL)	Current consumption on V_{DDA}	-	220	450	µA
I_{DD}(PLL)	Current consumption on V_{DD}	-	120	150	

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

6.3.9 Memory characteristics

RAM memory

Table 45. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode(1)	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory and data EEPROM

Table 46. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t_{prog}	Programming time for word or half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I_{DD}	Average current during the whole programming / erase operation	T_A = 25 °C, V_{DD} = 3.6 V	-	500	700	µA
	Maximum current (peak) during the whole programming / erase operation		-	1.5	2.5	mA

1. Guaranteed by design.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 48*. They are based on the EMS levels and classes defined in application note AN1709.

Table 48. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP48, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP48, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under the conditions summarized in *Table 20*. All I/Os are CMOS and TTL compliant.

Table 53. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TC, FT, FTf, RST I/Os	-	-	$0.3V_{DD}$	V
		BOOT0 pin	-	-	$0.14V_{DD}$ (1)	
V_{IH}	Input high level voltage	All I/Os	$0.7\ V_{DD}$	-	-	
V_{hys}	I/O Schmitt trigger voltage hysteresis (2)	Standard I/Os	-	$10\%\ V_{DD}$ (3)	-	
		BOOT0 pin	-	0.01	-	
I_{lkg}	Input leakage current (4)	$V_{SS} \le V_{IN} \le V_{DD}$ All I/Os except PA11, PA12, BOOT0 and FTf I/Os	-	-	±50	nA
		$V_{SS} \le V_{IN} \le V_{DD}$ PA11 and P12 I/Os	-	-	-50/+250	
		$V_{SS} \le V_{IN} \le V_{DD}$ FTf I/Os	-	-	±100	
		$V_{DD} \le V_{IN} \le 5$ V All I/Os except for PA11, PA12, BOOT0 and FTf I/Os	-	-	200	
		$V_{DD} \le V_{IN} \le 5$ V FTf I/Os	-	-	500	
		$V_{DD} \le V_{IN} \le 5$ V PA11, PA12 and BOOT0	-	-	10	µA
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	30	45	60	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by characterization.
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
3. With a minimum of 200 mV. Guaranteed by characterization results.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Table 58. R_{AIN} max for f_{ADC} = 16 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max for fast channels (kΩ)	R_{AIN} max for standard channels (kΩ)						
			V_{DD} > 2.7 V	V_{DD} > 2.4 V	V_{DD} > 2.0 V	V_{DD} > 1.8 V	V_{DD} > 1.75 V	V_{DD} > 1.65 V and T_A > –10 °C	V_{DD} > 1.65 V and T_A > 25 °C
1.5	0.09	0.5	< 0.1	NA	NA	NA	NA	NA	NA
3.5	0.22	1	0.2	< 0.1	NA	NA	NA	NA	NA
7.5	0.47	2.5	1.7	1.5	< 0.1	NA	NA	NA	NA
12.5	0.78	4	3.2	3	1	NA	NA	NA	NA
19.5	1.22	6.5	5.7	5.5	3.5	NA	NA	NA	< 0.1
39.5	2.47	13	12.2	12	10	NA	NA	NA	5
79.5	4.97	27	26.2	26	24	< 0.1	NA	NA	19
160.5	10.03	50	49.2	49	47	32	< 0.1	< 0.1	42

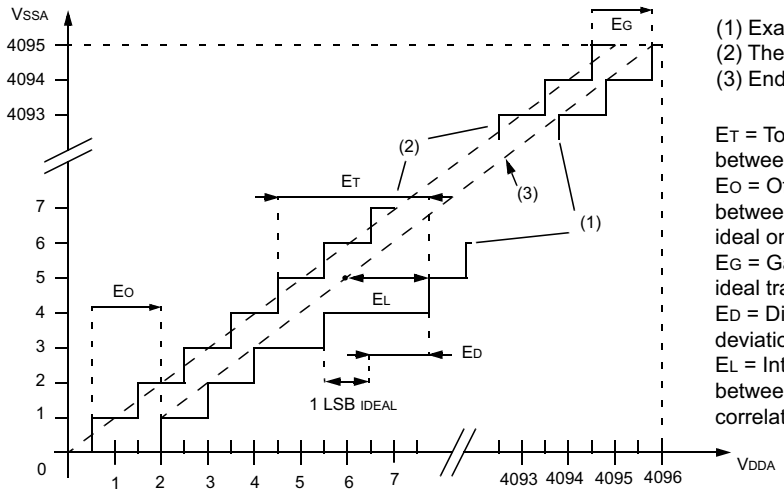
1. Guaranteed by design.

Table 59. ADC accuracy(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	1.65 V < V_{DDA} < 3.6 V, range 1/2/3	-	2	4	LSB
EO	Offset error		-	1	2.5	
EG	Gain error		-	1	2	
EL	Integral linearity error		-	1.5	2.5	
ED	Differential linearity error		-	1	1.5	
ENOB	Effective number of bits		10.2	11		bits
	Effective number of bits (16-bit mode oversampling with ratio =256)(4)		11.3	12.1	-	
SINAD	Signal-to-noise distortion		63	69	-	dB
SNR	Signal-to-noise ratio		63	69	-	
	Signal-to-noise ratio (16-bit mode oversampling with ratio =256)(4)		70	76	-	
THD	Total harmonic distortion		-	-85	-73	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.12* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. This number is obtained by the test board without additional noise, resulting in non-optimized value for oversampling mode.

Figure 29. ADC accuracy characteristics

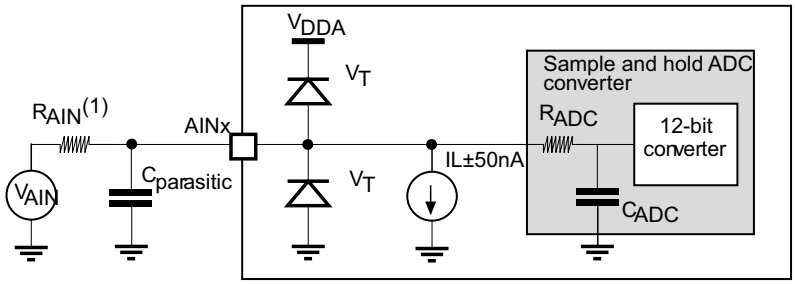


(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

E_T = Total Unajusted Error: maximum deviation between the actual and ideal transfer curves.
E_O = Offset Error: maximum deviation between the first actual transition and the first ideal one.
E_G = Gain Error: deviation between the last ideal transition and the last actual one.
E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal ones.
E_L = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

MS19880V2

Figure 30. Typical connection diagram using the ADC



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1. Refer to *Table 57: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

6.3.16 Temperature sensor characteristics

Table 60. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3 V	0x1FF8 007A - 0x1FF8 007B
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C V_{DDA}= 3 V	0x1FF8 007E - 0x1FF8 007F

Table 64. TIMx(1) characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	0.0312	2048	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM21, and TIM22 timers.

6.3.19 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I²C timing requirements are guaranteed by design when the I²C peripheral is properly configured (refer to the reference manual for details). The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics).

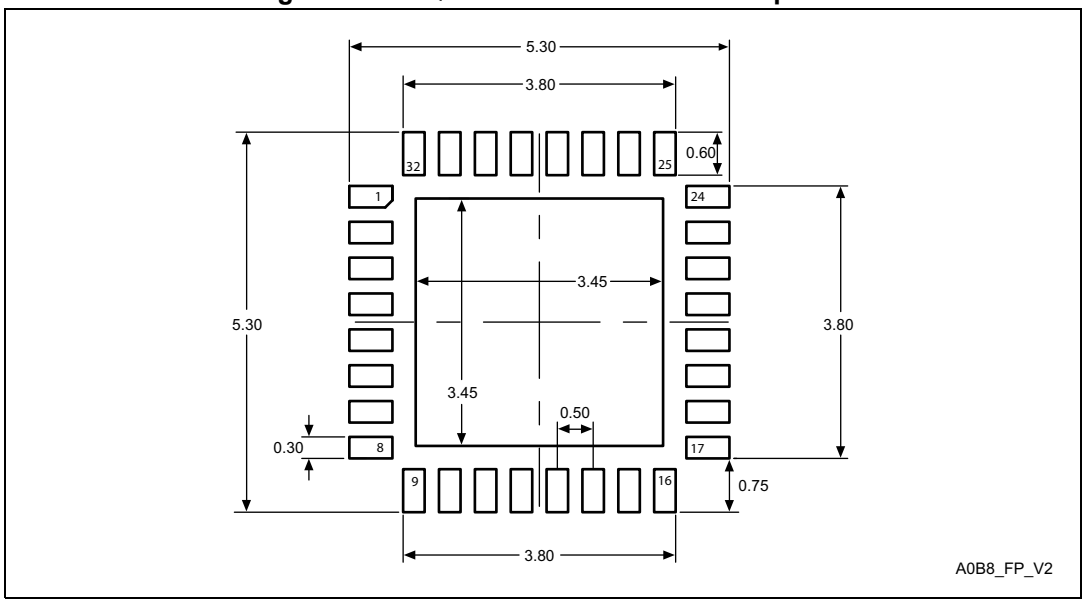
All I²C SDA and SCL I/Os embed an analog filter (see *Table 65* for the analog filter characteristics).

Table 65. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

Figure 41. UFQFPN32 recommended footprint

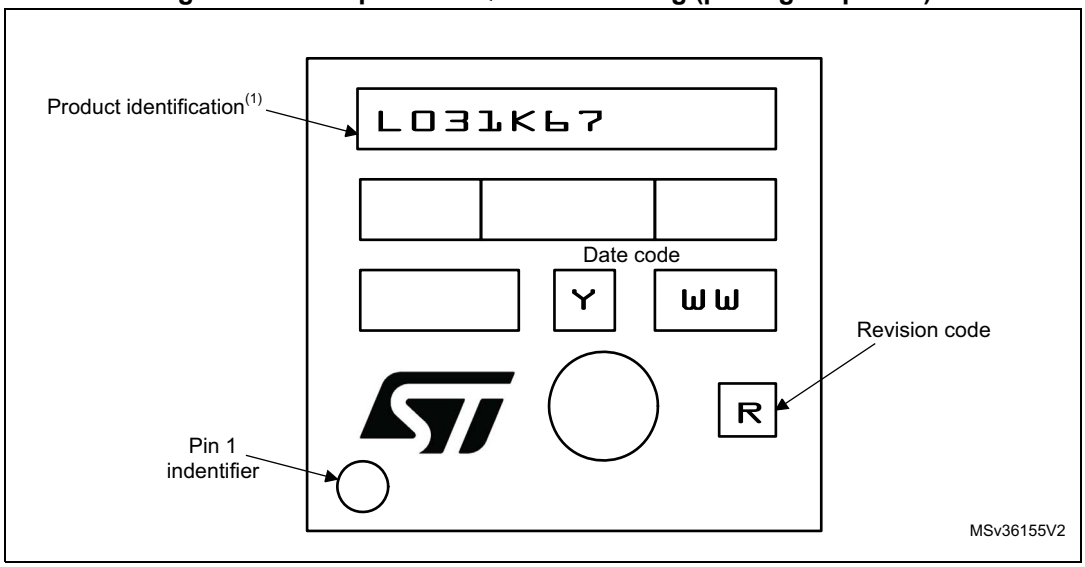


1. Dimensions are expressed in millimeters.

UFQFPN32 device marking

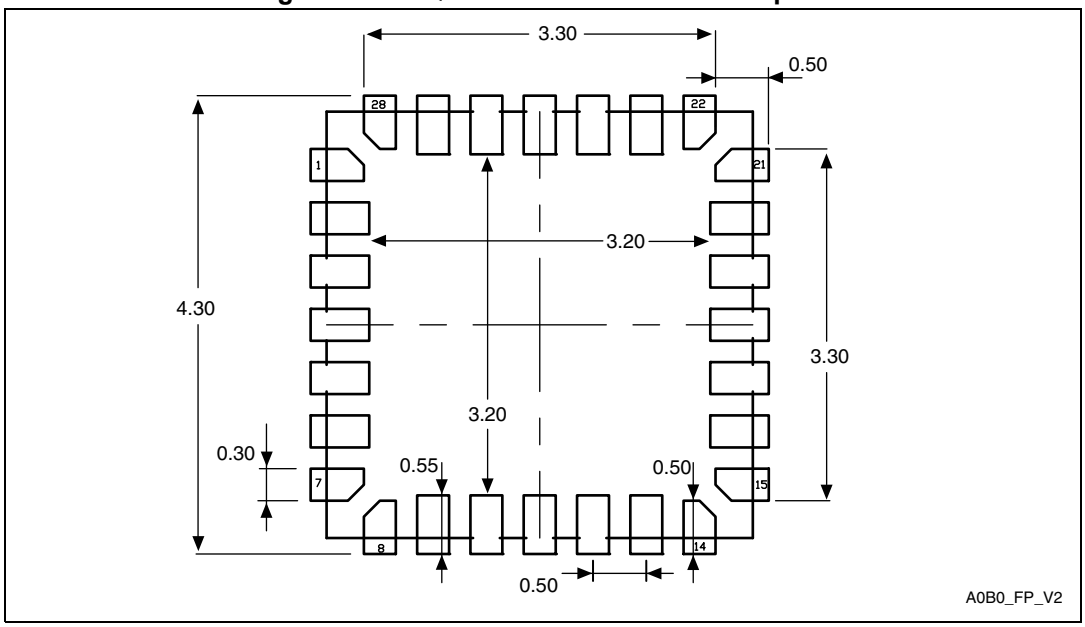
The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 42. Example of UFQFPN32 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 44. UFQFPN28 recommended footprint

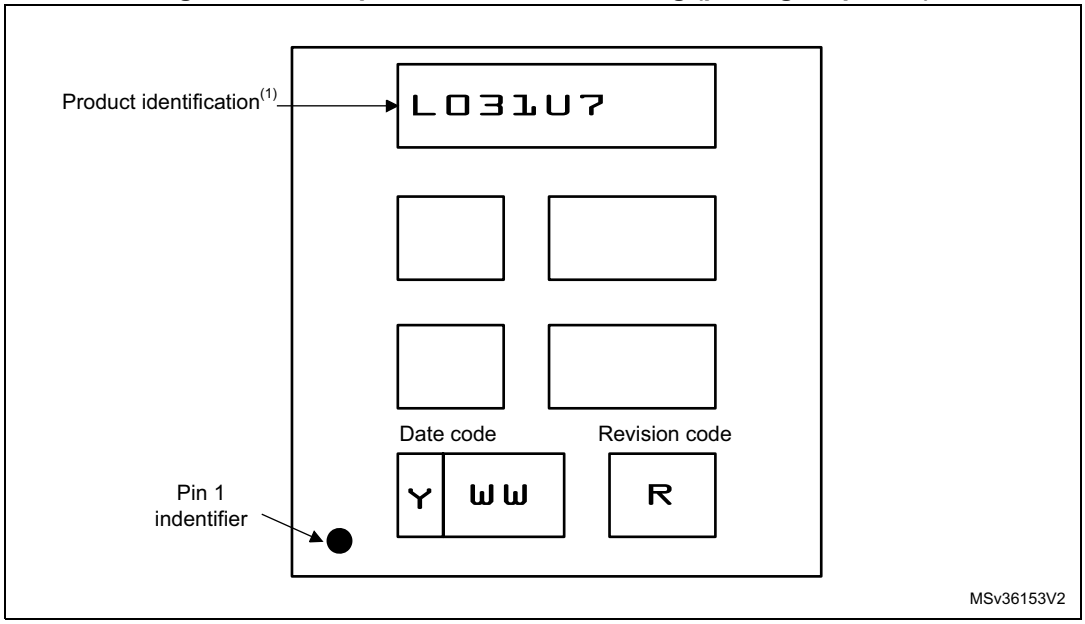


1. Dimensions are expressed in millimeters.

UFQFPN28 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 45. Example of UFQFPN28 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 79. Document revision history

Date	Revision	Changes
05-Apr-2016	4	*Features*: – Change minimum comparator supply voltage to 1.65 V. – Updated current consumptions in Standby, Stop and Stop with RTC ON modes. Updated number of GPIOs for STM32L031GxUxS in *Table 2: Ultra-low-power STM32L031x4/x6 device features and peripheral counts*. Removed note related to preliminary consumption values in *Table 5: Functionalities depending on the working mode (from Run/active down to standby)*. Added number of fast and standard channels in *Section 3.10: Analog-to-digital converter (ADC)*. Added baudrate allowing to wake up the MCU from Stop mode in *Section 3.15.2: Universal synchronous/asynchronous receiver transmitter (USART)* and *Section 3.15.3: Low-power universal asynchronous receiver transmitter (LPUART)*. Changed V_{DDA} minimum value to 1.65 V in *Table 20: General operating conditions*. Added I_{REFINT} value for V_{DD}=1.8 V in *Table 35: Peripheral current consumption in Stop and Standby mode*. *Section 6.3.15: 12-bit ADC characteristics*: – *Table 57: ADC characteristics*: Distinction made between V_{DDA} for fast and standard channels; added note *1.* Added note *4.* related to R_{ADC}. Updated t_S and t_{CONV}. – Updated *Table 58: RAIN max for fADC = 16 MHz* for f_{ADC} = 16 MHz and distinction made between fast and standard channels. Added *Table 66: USART/LPUART characteristics*.