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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details		
Product Status	Active	
Core Processor	ARM® Cortex®-M0+	
Core Size	32-Bit Single-Core	
Speed	32MHz	
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART	
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT	
Number of I/O	27	
Program Memory Size	32KB (32K x 8)	
Program Memory Type	FLASH	
EEPROM Size	1K x 8	
RAM Size	8K x 8	
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V	
Data Converters	A/D 10x12b	
Oscillator Type	Internal	
Operating Temperature	-40°C ~ 105°C (TA)	
Mounting Type	Surface Mount	
Package / Case	32-UFQFN Exposed Pad	
Supplier Device Package	32-UFQFPN (5x5)	
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l031k6u7	

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STM32L031x4/6 Functional overview

### 3 Functional overview

### 3.1 Low-power modes

The ultra-low-power STM32L031x4/6 supports dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V<sub>DD</sub> range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V<sub>DD</sub> range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V<sub>DD</sub> range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

#### Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

#### Low-power run mode

This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

#### Low-power sleep mode

This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

#### Stop mode with RTC

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the  $V_{CORE}$  domain are stopped, the PLL, MSI RC, HSE and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The device can be woken up from Stop mode by any of the EXTI line, in  $3.5 \mu s$ , the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event

Functional overview STM32L031x4/6

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)<sup>(1)</sup>

			Low-	Low-		Stop		Standby
IPs	Run/Active	Sleep	power run	power sleep		Wakeup capability		Wakeup capability
Power-on/down reset (POR/PDR)	Y	Y	Υ	Y	Υ	Y	Υ	Y
High Speed Internal (HSI)	0	0			(2)			
High Speed External (HSE)	0	0	0	0				
Low Speed Internal (LSI)	0	0	0	0	0		0	
Low Speed External (LSE)	0	0	0	0	0		0	
Multi-Speed Internal (MSI)	0	0	Υ	Y				
Inter-Connect Controller	Y	Y	Υ	Y	Υ			
RTC	0	0	0	0	0	0	0	
RTC Tamper	0	0	0	0	0	0	0	0
Auto WakeUp (AWU)	0	0	0	0	0	0	0	0
USART	0	0	0	0	O <sup>(3)</sup>	0		
LPUART	0	0	0	0	O <sup>(3)</sup>	0		
SPI	0	0	0	0				
I2C	0	0	0	0	O <sup>(4)</sup>	0		
ADC	0	0						
Temperature sensor	0	0	0	0	0			
Comparators	0	0	0	0	0	0		
16-bit timers	0	0	0	0				
LPTIMER	0	0	0	0	0	0		
IWDG	0	0	0	0	0	0	0	0
WWDG	0	0	0	0				
SysTick Timer	0	0	0	0				
GPIOs	0	0	0	0	0	0		2 pins
Wakeup time to Run mode	0 µs	0.36 µs	3 µs	32 µs				65 µs

Functional overview STM32L031x4/6

### 3.12 Ultra-low-power comparators and reference voltage

The STM32L031x4/6 embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with ultra low consumption
- One comparator with rail-to-rail inputs, fast or slow mode.
- The threshold can be one of the following:
  - External I/O pins
  - Internal reference voltage (V<sub>REFINT</sub>)
  - submultiple of Internal reference voltage(1/4, 1/2, 3/4) for the rail to rail comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

## 3.13 System configuration controller

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM21, TIM22 and LPTIM timer input captures. It also controls the routing of internal analog signals to the ADC, COMP1 and COMP2 and the internal reference voltage  $V_{\sf RFFINT}$ .

## 3.14 Timers and watchdogs

The ultra-low-power STM32L031x4/6 devices include three general-purpose timers, one low-power timer (LPTM), two watchdog timers and the SysTick timer.

*Table 9* compares the features of the general-purpose and basic timers.

Table 9. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2	16-bit	Up, down, up/down Any integer between 1 and 65536		Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No

STM32L031x4/6 Functional overview

Table 11. STM32L031x4/6 I<sup>2</sup>C implementation

I2C features <sup>(1)</sup>	I2C1
7-bit addressing mode	Х
10-bit addressing mode	Х
Standard mode (up to 100 kbit/s)	Х
Fast mode (up to 400 kbit/s)	Х
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X <sup>(2)</sup>
Independent clock	Х
SMBus	Х
Wakeup from STOP	Х

<sup>1.</sup> X = supported.

### 3.15.2 Universal synchronous/asynchronous receiver transmitter (USART)

The USART interface (USART2) is able to communicate at speeds of up to 4 Mbit/s.

it provides hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART2 also supports Smartcard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock that allows to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

USART2 interface can be served by the DMA controller.

Table 12 for the supported modes and features of USART interface.

Table 12. USART implementation

USART modes/features <sup>(1)</sup>	USART2
Hardware flow control for modem	X
Continuous communication using DMA	Х
Multiprocessor communication	Х
Synchronous mode <sup>(2)</sup>	Х
Smartcard mode	Х
Single-wire half-duplex communication	Х
IrDA SIR ENDEC block	Χ
LIN mode	Х
Dual clock domain and wakeup from Stop mode	Х
Receiver timeout interrupt	Χ
Modbus communication	Х
Auto baud rate detection (4 modes)	Х
Driver Enable	Х

<sup>1.</sup> X = supported.



<sup>2.</sup> See Table 15: Pin definitions on page 38 for the list of I/Os that feature Fast Mode Plus capability

STM32L031x4/6 Pin descriptions

Table 15. Pin definitions (continued)

		Pin	Num	ber								
TSSOP20	WLCSP25 <sup>(1)</sup>	UFQFPN28	UFQFPN28 (STM32L031GxUxS only)	LQFP32	UFQFPN32 <sup>(2)</sup>	LQFP48	Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
1	A5	27	1	31	31	44	воото	I	-	-	-	-
-	-	-	-	-	32	45	PB8	I/O	FTf	-	I2C1_SCL	-
-	-	ı	-	-	-	46	PB9	I/O	FTf	-	EVENTOUT, I2C1_SDA	-
-	ı	28	-	32	-	47	VSS	S	-	-	-	-
-	-	1	-	1	1	48	VDD	S	-	-	-	-

<sup>1.</sup> WLCSP25 package is in development. Its ballout is subject to change.

<sup>2.</sup> VSS pins are connected to the exposed pad (see Figure 40: UFQFPN32, 5 x 5 mm, 32-pin package outline).

### 6 Electrical characteristics

#### 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V<sub>SS</sub>.

#### 6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_A = 25$  °C and  $T_A = T_A$ max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3 $\sigma$ ).

#### 6.1.2 Typical values

Unless otherwise specified, typical data are based on  $T_A$  = 25 °C,  $V_{DD}$  = 3.6 V (for the 1.65 V  $\leq$  V $_{DD}$   $\leq$  3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$ ).

### 6.1.3 Typical curves

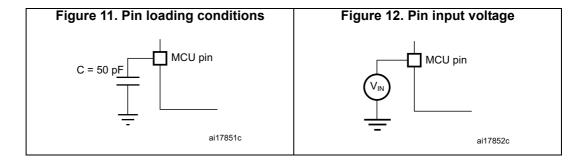
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 11.

#### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.



## 6.1.6 Power supply scheme

Standby-power circuitry (OSC32,RTC,Wake-up logic, RTC backup registers) Ю GP I/Os Kernel logic Logic (CPU, Digital & Memories) Regulator N × 100 nF + 1  $\times$  10  $\mu F$  $V_{\text{DDA}}$  $V_{\text{DDA}}$ Analog: 100 nF ■ + 1 µF RC,PLL,COMP, ADC  $V_{\text{SSA}}$ MSv36135V1

Figure 13. Power supply scheme

## 6.1.7 Current consumption measurement

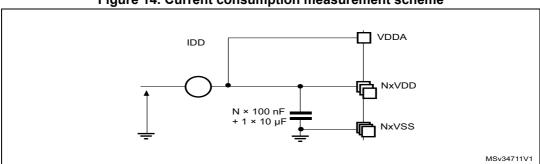


Figure 14. Current consumption measurement scheme

577

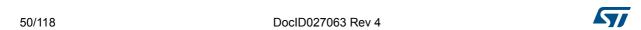
**Table 18. Current characteristics** 

Symbol	Ratings	Max.	Unit
$\Sigma I_{VDD}^{(2)}$	Total current into sum of all V <sub>DD</sub> power lines (source) <sup>(1)</sup>	105	
ΣI <sub>VSS</sub> <sup>(2)</sup>	Total current out of sum of all V <sub>SS</sub> ground lines (sink) <sup>(1)</sup>	105	
I <sub>VDD(PIN)</sub>	Maximum current into each V <sub>DD</sub> power pin (source) <sup>(1)</sup>	100	
I <sub>VSS(PIN)</sub>	Maximum current out of each V <sub>SS</sub> ground pin (sink) <sup>(1)</sup>	100	
	Output current sunk by any I/O and control pin except FTf pins	16	
I <sub>IO</sub>	Output current sunk by FTf pins	22	
	Output current sourced by any I/O and control pin	-16	
ΣI (3)	Total output current sunk by sum of all IOs and control pins <sup>(4)</sup>	45	mA
ΣΙ <sub>ΙΟ(PIN)</sub> <sup>(3)</sup>	Total output current sourced by sum of all IOs and control pins <sup>(4)</sup>	-45	
ΣI (5)	Total output current sunk by sum of all IOs and control pins <sup>(2)</sup>	90	
ΣΙ <sub>ΙΟ(PIN)</sub> <sup>(5)</sup>	Total output current sourced by sum of all IOs and control $pins^{(2)}$	-90	
	Injected current on FT, FFf, RST and B pins	-5/+0 <sup>(6)</sup>	
I <sub>INJ(PIN)</sub>	Injected current on TC pin	± 5 <sup>(7)</sup>	
ΣΙ <sub>ΙΝJ(PIN)</sub>	Total injected current (sum of all I/O and control pins) <sup>(8)</sup>	± 25	

- All main power (V<sub>DD</sub>, V<sub>DDA</sub>) and ground (V<sub>SS</sub>, V<sub>SSA</sub>) pins must always be connected to the external power supply, in the permitted range.
- This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
- 3. These values apply only to STM32L031GxUxS part number.
- 4. This current consumption must be correctly distributed over all I/Os and control pins. In particular, it must be located the closest possible to the couple of supply and ground, and distributed on both sides.
- 5. These values apply to all part numbers except for STM32L031GxUxS.
- Positive current injection is not possible on these I/Os. A negative injection is induced by V<sub>IN</sub><V<sub>SS</sub>. I<sub>INJ(PIN)</sub> must never be exceeded. Refer to *Table 17* for maximum allowed input voltage values.
- A positive injection is induced by V<sub>IN</sub> > V<sub>DD</sub> while a negative injection is induced by V<sub>IN</sub> < V<sub>SS</sub>. I<sub>INJ(PIN)</sub> must never be exceeded. Refer to Table 17: Voltage characteristics for the maximum allowed input voltage values.
- When several inputs are submitted to a current injection, the maximum ΣI<sub>INJ(PIN)</sub> is the absolute sum of the
  positive and negative injected currents (instantaneous values).

**Table 19. Thermal characteristics** 

Symbol	Ratings	Value	Unit
T <sub>STG</sub>	Storage temperature range	-65 to +150	°C
$T_J$	Maximum junction temperature	150	°C



	3, produce 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1					
Symbol	Parameter	Conditions	Тур	Max <sup>(1)</sup>	Unit	
	Supply current in Stop mode	$T_A = -40$ °C to 25°C	0.38	0.99		
		T <sub>A</sub> = 55°C	0.54	1.9		
I <sub>DD</sub> (Stop)		T <sub>A</sub> = 85°C	1.35	4.2	μΑ	
		T <sub>A</sub> = 105°C	3.1	9		
		T <sub>A</sub> = 125°C	7.55	19		

<sup>1.</sup> Guaranteed by characterization results at 125  $^{\circ}\text{C},$  unless otherwise specified.

Figure 18.  $I_{DD}$  vs  $V_{DD}$ , at  $T_A$ = 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive

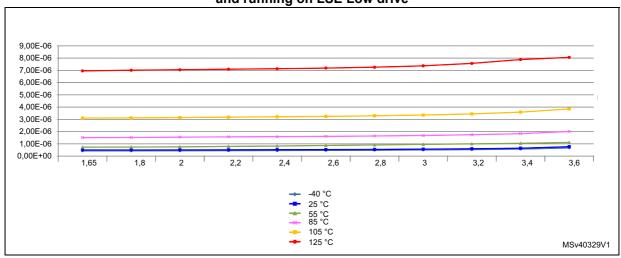
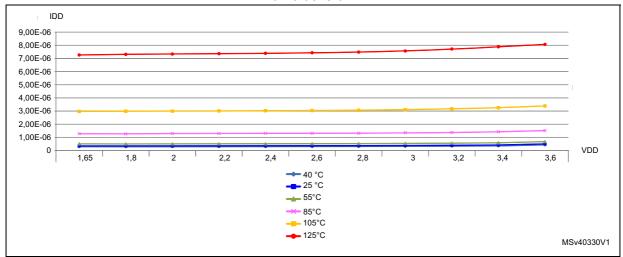


Figure 19.  $I_{DD}$  vs  $V_{DD}$ , at  $T_A$ = 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks off



#### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following tables. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V<sub>DD</sub> or V<sub>SS</sub> (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on

Table 34. Peripheral current consumption in Run or Sleep mode<sup>(1)</sup>

Peripheral		Туріс	al consumption,	V <sub>DD</sub> = 3.0 V, T <sub>A</sub> =	25 °C	
		Range 1, V <sub>CORE</sub> =1.8 V VOS[1:0] = 01	Range 2, V <sub>CORE</sub> =1.5 V VOS[1:0] = 10	Range 3, V <sub>CORE</sub> =1.2 V VOS[1:0] = 11	Low-power sleep and run	Unit
	WWDG	3	2	2	2	
	LPUART1	8	6.5	5.5	6	
APB1	I2C1	11	9.5	7.5	9	A /N/ILI-7 /f
AFDI	LPTIM1	10	8.5	6.5	8	μΑ/MHz (f <sub>HCLK</sub> )
	TIM2	10.5	8.5	7	9	
	USART2	14.5	12	9.5	11	
	ADC1 <sup>(2)</sup>	5.5	5	3.5	4	
	SPI1	4	3	3	2.5	
APB2	TIM21	7.5	6	5	5.5	A /N/Ll /f
APBZ	TIM22	7	6	5	6	μΑ/MHz (f <sub>HCLK</sub> )
	DBGMCU	1.5	1	1	0.5	]
	SYSCFG	2.5	2	2	1.5	]
	GPIOA	3.5	3	2.5	2.5	
Cortex-	GPIOB	3.5	2.5	2	2.5	
M0+ core I/O port	GPIOC	8.5	6.5	5.5	7	μΑ/MHz (f <sub>HCLK</sub> )
	GPIOH	1.5	1	1	0.5	
	CRC	1.5	1	1	1	
ALID	FLASH	0(3)	0(3)	0(3)	0(3)	]
AHB	DMA1	10	8	6.5	8.5	μΑ/MHz (f <sub>HCLK</sub> )
All enabled	1	101	83	66	85	
PWR		2.5	2	2	1	μΑ/MHz (f <sub>HCLK</sub> )

Data based on differential I<sub>DD</sub> measurement between all peripherals off an one peripheral with clock enabled, in the following conditions: f<sub>HCLK</sub> = 32 MHz (range 1), f<sub>HCLK</sub> = 16 MHz (range 2), f<sub>HCLK</sub> = 4 MHz (range 3), f<sub>HCLK</sub> = 64kHz (Low-power run/sleep), f<sub>APB1</sub> = f<sub>HCLK</sub>, f<sub>APB2</sub> = f<sub>HCLK</sub>, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.



<sup>2.</sup> HSI oscillator is off for this measure.

<sup>3.</sup> Current consumption is negligible and close to 0  $\mu A$ .

## Low-speed internal (LSI) RC oscillator

Table 42. LSI oscillator characteristics

Symbol	Parameter	Min	Тур	Max	Unit
f <sub>LSI</sub> <sup>(1)</sup>	LSI frequency	26	38	56	kHz
D <sub>LSI</sub> <sup>(2)</sup>	LSI oscillator frequency drift $0^{\circ}C \le T_A \le 85^{\circ}C$	-10	-	4	%
t <sub>su(LSI)</sub> <sup>(3)</sup>	LSI oscillator startup time	-	-	200	μs
I <sub>DD(LSI)</sub> (3)	LSI oscillator power consumption	-	400	510	nA

- 1. Guaranteed by test in production.
- 2. This is a deviation for an individual part, once the initial frequency has been measured.
- 3. Guaranteed by design.

## Multi-speed internal (MSI) RC oscillator

Table 43. MSI oscillator characteristics

Symbol	Parameter	Condition	Тур	Max	Unit	
		MSI range 0	65.5	-		
		MSI range 1	131	-	kHz	
		MSI range 2	262	-	NI IZ	
f <sub>MSI</sub>	Frequency after factory calibration, done at $V_{DD}$ = 3.3 V and $T_A$ = 25 °C	MSI range 3	524	-		
	TOD COLUMN IN THE COLUMN IN TH	MSI range 4	1.05	-		
		MSI range 5	2.1	-	MHz	
		MSI range 6	4.2	-		
ACC <sub>MSI</sub>	Frequency error after factory calibration	-	±0.5	-	%	
D <sub>TEMP(MSI)</sub> <sup>(1)</sup>	MSI oscillator frequency drift $0 \text{ °C} \leq T_A \leq 85 \text{ °C}$	-	±3	-	%	
D <sub>VOLT(MSI)</sub> <sup>(1)</sup>	MSI oscillator frequency drift 1.65 V $\leq$ V <sub>DD</sub> $\leq$ 3.6 V, T <sub>A</sub> = 25 °C	-	-	2.5	%/V	
		MSI range 0	0.75	-		
		MSI range 1	1	-		
		MSI range 2	1.5	-		
I <sub>DD(MSI)</sub> <sup>(2)</sup>	MSI oscillator power consumption	MSI range 3	2.5	-	μΑ	
		MSI range 4	4.5	-		
		MSI range 5	8	-		
		MSI range 6	15	-		

Cumbal	Doromotor		Unit			
Symbol	Parameter	Min Typ		Max <sup>(1)</sup>	Unit	
f <sub>PLL_OUT</sub>	PLL output clock	2	-	32	MHz	
t <sub>LOCK</sub>	PLL input = 16 MHz PLL VCO = 96 MHz	-	115	160	μs	
Jitter	Cycle-to-cycle jitter	-		± 600	ps	
I <sub>DDA</sub> (PLL)	Current consumption on V <sub>DDA</sub>	-	220	450		
I <sub>DD</sub> (PLL)	Current consumption on V <sub>DD</sub>	-	120	150	μΑ	

Table 44. PLL characteristics (continued)

## 6.3.9 Memory characteristics

#### **RAM** memory

Table 45. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
VRM	Data retention mode <sup>(1)</sup>	STOP mode (or RESET)	1.65	-	-	V

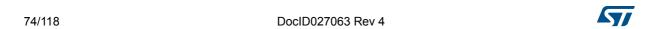
Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

## Flash memory and data EEPROM

Table 46. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Тур	Max <sup>(1)</sup>	Unit
V <sub>DD</sub>	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
+	Programming time for	Erasing	-	3.28	3.94	ms
<sup>L</sup> prog	word or half-page	Programming	-	3.28	3.94	1115
	Average current during the whole programming / erase operation		-	500	700	μΑ
I <sub>DD</sub>	Maximum current (peak) during the whole programming / erase operation	$T_A = 25  ^{\circ}C,  V_{DD} = 3.6  V$	-	1.5	2.5	mA

<sup>1.</sup> Guaranteed by design.



<sup>1.</sup> Guaranteed by characterization results.

<sup>2.</sup> Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f\_PLL\_OUT.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 51. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T <sub>A</sub> = +125 °C conforming to JESD78A	II level A

### 6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below  $V_{SS}$  or above  $V_{DD}$  (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

#### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of  $-5 \,\mu\text{A}/+0 \,\mu\text{A}$  range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the *Table 52*.

Table 52. I/O current injection susceptibility

		Functional s		
Symbol	Description	Negative injection	Positive injection	Unit
	Injected current on BOOT0	-0	NA	
	Injected current on PA0, PA2, PA4, PA5, PC15, PH0 and PH1	-5	0	mA
INJ	Injected current on any other FT and FTf pin	-5 <sup>(1)</sup>	NA	ША
	Injected current on any other pin	-5 <sup>(1)</sup>	+5	

It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

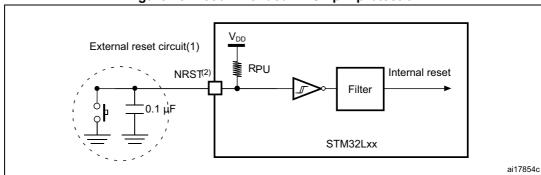


Figure 28. Recommended NRST pin protection

- 1. The reset network protects the device against parasitic resets.
- 2. The user must ensure that the level on the NRST pin can go below the V<sub>IL(NRST)</sub> max level specified in *Table 56*. Otherwise the reset will not be taken into account by the device.

#### 6.3.15 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 57* are values derived from tests performed under ambient temperature, f<sub>PCLK</sub> frequency and V<sub>DDA</sub> supply voltage conditions summarized in *Table 20: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 57. ADC characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V	Analog supply voltage for	Fast channel	1.65	-	3.6	V
$V_{DDA}$	ADC on	Standard channel	1.75 <sup>(1)</sup>	-	3.6	V
	Current consumption of the	1.14 Msps	-	200	-	
	ADC on V <sub>DDA</sub>	10 ksps	-	40	-	
I <sub>DDA</sub> (ADC)	Current consumption of the	1.14 Msps	-	70	-	μA
	ADC on V <sub>DD</sub> <sup>(2)</sup>	10 ksps	-	1	-	
	ADC clock frequency	Voltage scaling Range 1	0.14	-	16	
f <sub>ADC</sub>		Voltage scaling Range 2	0.14	-	8	MHz
		Voltage scaling Range 3	0.14	-	4	
f <sub>S</sub> <sup>(3)</sup>	Sampling rate		0.05	-	1.14	MHz
£ (3)	External trigger frequency	f <sub>ADC</sub> = 16 MHz	-	-	941	kHz
f <sub>TRIG</sub> <sup>(3)</sup>	External trigger frequency		-	-	17	1/f <sub>ADC</sub>
V <sub>AIN</sub>	Conversion voltage range		0	-	$V_{DDA}$	V
R <sub>AIN</sub> <sup>(3)</sup>	External input impedance	See Equation 1 and Table 58 for details	-	-	50	kΩ
R <sub>ADC</sub> <sup>(3)(4)</sup>	Sampling switch resistance		-	-	1	kΩ
C <sub>ADC</sub> <sup>(3)</sup>	Internal sample and hold capacitor		-	-	8	pF

#### LQFP32 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

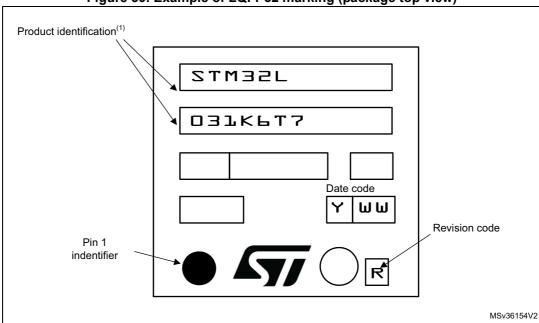


Figure 39. Example of LQFP32 marking (package top view)

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Revision history STM32L031x4/6

Table 79. Document revision history

Date	Revision	Changes
		Updated number of SPI interfaces on cover page and in <i>Table 2: Ultra-low-power STM32L031x4/x6 device features and peripheral counts.</i>
		Updated number of GPIOs for devices in UFQFPN28 in <i>Table 2: Ultra-low-power STM32L031x4/x6 device features and peripheral counts.</i>
		Updated Section 3.4.4: Boot modes.
01-Feb-2016	3	Updated Section 3.15.2: Universal synchronous/asynchronous receiver transmitter (USART) and Section 3.15.4: Serial peripheral interface (SPI) to mention the fact that USARTs with synchronous mode feature can be used as SPI master interfaces.
01-1 65-2010	3	Modified pin 2 in Figure 5: STM32L031x4/6 UFQFPN32 pinout.
		Added Figure 7: STM32L031GxUxS UFQFPN28 pinout.
		Table 15: Pin definitions:
		<ul> <li>Added UFQFPN28 for STM32L031GxUxS part number.</li> </ul>
		- Renamed PA0-WKUP-CK_IN into PA0-CK_IN
		- Renamed PA0-WKUP into PA0
		Updated <i>Table 18: Current characteristics</i> to add the total output current for STM32L031GxUxS.
		Added one power pair option in <i>Table 78: STM32L031x4/6 ordering information scheme</i> .

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