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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	60MHz
Connectivity	SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-VQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c51rb2-rlrim

Table 11 shows all SFRs with their address and their reset value.

Table 11. SFR Mapping

	Bit addressable	**Non Bit addressable**							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h		CH 0000 0000	CCAP0H XXXX	CCAP1H XXXX	CCAPL2H XXXX	CCAPL3H XXXX	CCAPL4H XXXX		FFh
F0h	B 0000 0000								F7h
E8h		CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAPL2L XXXX XXXX	CCAPL3L XXXX XXXX	CCAPL4L XXXX XXXX		EFh
E0h	ACC 0000 0000								E7h
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh
D0h	PSW 0000 0000	FCON [1] XXXX 0000							D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h				SPCON 0001 0100	SPSTA 0000 0000	SPDAT XXXX XXXX			C7h
B8h	IPL0 X000 000	SADEN 0000 0000							BFh
B0h	P3 1111 1111	IEN1 XXXXX 000	IPL1 XXXXX000	IPH1 XXXX X000				IPH0 X000 0000	B7h
A8h	IEN0 0000 0000	SADDR 0000 0000						CKCON1 XXXX XXX0	AFh
A0h	P2 1111 1111		AUXR1 XXXXX0X0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	BRL 0000 0000	BDRCON XXX0 0000	KBLS 0000 0000	KBE 0000 0000	KBF 0000 0000		9Fh
90h	P1 1111 1111							CKRL 1111 1111	97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XX0X 0000	CKCON0 0000 0000	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

1. FCON access is reserved for the Flash API and ISP software.

Reserved

Oscillator

To optimize the power consumption and execution time needed for a specific task, an internal, prescaler feature has been implemented between the oscillator and the CPU and peripherals.

Registers

Table 13. CKRL Register

CKRL – Clock Reload Register (97h)

7	6	5	4	3	2	1	0
CKRL7	CKRL6	CKRL5	CKRL4	CKRL3	CKRL2	CKRL1	CKRL0

Bit Number	Mnemonic	Description
7:0	CKRL	**Clock Reload Register** Prescaler value

Reset Value = 1111 1111b
Not bit addressable

Table 14. PCON Register

PCON – Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial Port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial Port Mode bit 0** Cleared to select SM0 bit in SCON register. Set to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-off Flag** Cleared to recognize next reset type. Set by hardware when V_{CC} rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General-purpose Flag** Cleared by software for general-purpose usage. Set by software for general-purpose usage.
2	GF0	**General-purpose Flag** Cleared by software for general-purpose usage. Set by software for general-purpose usage.
1	PD	**Power-down Mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle Mode bit** Cleared by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b Not bit addressable

Table 21. T2MOD Register

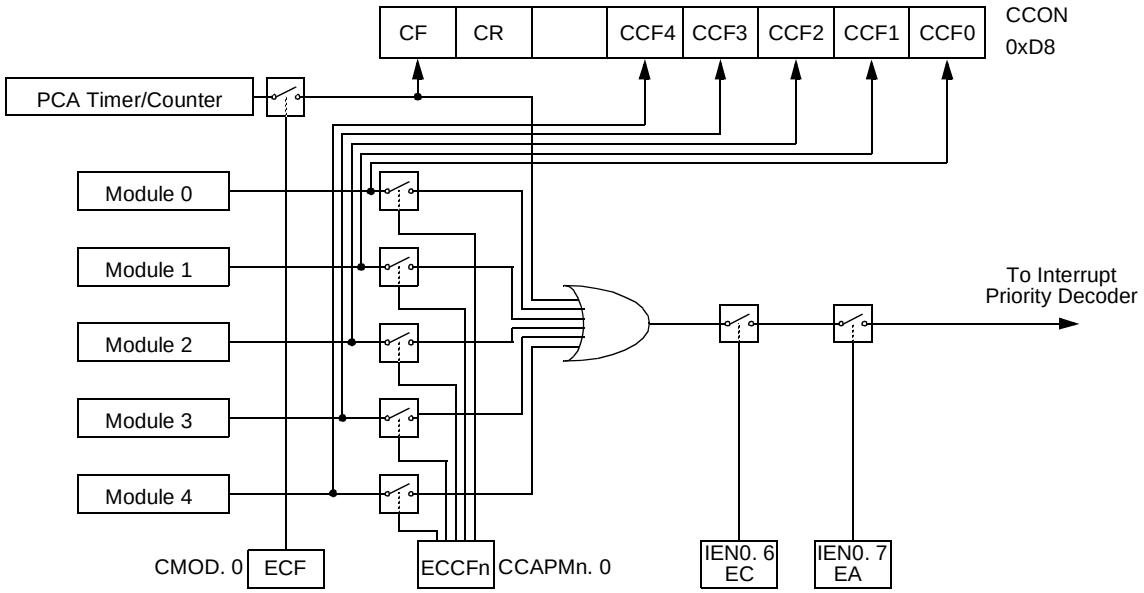
T2MOD – Timer 2 Mode Control Register (C9h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	T2OE	**Timer 2 Output Enable Bitt** Cleared to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.
0	DCEN	**Down Counter Enable Bit** Cleared to disable Timer 2 as up/down counter. Set to enable Timer 2 as up/down counter.

Reset Value = XXXX XX00b
Not bit addressable

Figure 12. PCA Interrupt System



PCA Modules: each one of the five compare/capture Modules has six possible functions. It can perform:

- 16-bit Capture, positive-edge triggered
- 16-bit Capture, negative-edge triggered
- 16-bit Capture, both positive and negative-edge triggered
- 16-bit Software Timer
- 16-bit High-speed Output
- 8-bit Pulse Width Modulator

In addition, Module 4 can be used as a Watchdog Timer.

Each Module in the PCA has a special function register associated with it. These registers are: CCAPM0 for Module 0, CCAPM1 for Module 1, etc. (see Table 24). The registers contain the bits that control the mode that each Module will operate in.

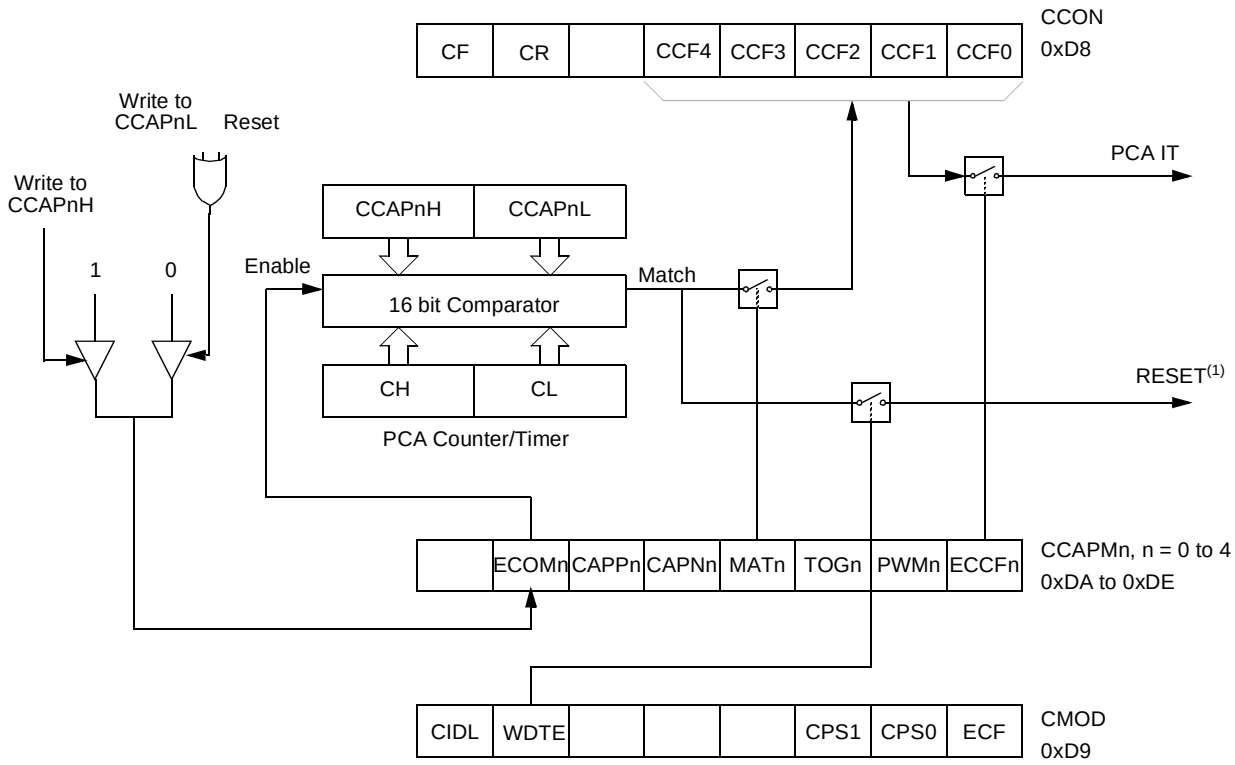
- The ECCF bit (CCAPMn. 0 where n = 0, 1, 2, 3, or 4 depending on the Module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated Module.
- PWM (CCAPMn. 1) enables the pulse width modulation mode.
- The TOG bit (CCAPMn. 2) when set causes the CEX output associated with the Module to toggle when there is a match between the PCA counter and the Module's capture/compare register.
- The match bit MAT (CCAPMn. 3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the Module's capture/compare register.
- The next two bits CAPN (CCAPMn. 4) and CAPP (CCAPMn. 5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition.
- The last bit in the register ECOM (CCAPMn. 6) when set enables the comparator function.

Table 24 shows the CCAPMn settings for the various PCA functions.

16-bit Software Timer/ Compare Mode

The PCA Modules can be used as software timers by setting both the ECOM and MAT bits in the Modules CCAPMn register. The PCA timer will be compared to the Module's capture registers and when a match occurs, an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the Module are both set (see Figure 14).

Figure 14. PCA Compare Mode and PCA Watchdog Timer



Note: 1. Only for Module 4

Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could occur. Writing to CCAPnH will set the ECOM bit.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

The SADEN byte is selected so that each slave may be addressed separately.
For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1.To communicate with slave A only, the master must send an address where bit 0 is clear (e. g. 1111 0000b).
For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e. g. 1111 0011b).
To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e. g. 1111 0001b).

Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e. g. :

SADDR0101 0110b
SADEN1111 1100b

Broadcast =SADDR OR SADEN1111 111Xb

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

Slave A:SADDR1111 0001b
SADEN1111 1010b
Broadcast1111 1X11b,

Slave B:SADDR1111 0011b
SADEN1111 1001b
Broadcast1111 1X11B,

Slave C:SADDR=1111 0011b
SADEN1111 1101b
Broadcast1111 1111b

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.

Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i. e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

Registers

Table 51. KBF Register

KBF - Keyboard Flag Register (9Eh)

7	6	5	4	3	2	1	0
KBF7	KBF6	KBF5	KBF4	KBF3	KBF2	KBF1	KBF0

Bit Number	Bit Mnemonic	Description
7	KBF7	**Keyboard Line 7 Flag** Set by hardware when the Port line 7 detects a programmed level. It generates a Keyboard interrupt request if the KBKBIE. 7 bit in KBIE register is set. Must be cleared by software.
6	KBF6	**Keyboard Line 6 Flag** Set by hardware when the Port line 6 detects a programmed level. It generates a Keyboard interrupt request if the KBIE. 6 bit in KBIE register is set. Must be cleared by software.
5	KBF5	**Keyboard Line 5 Flag** Set by hardware when the Port line 5 detects a programmed level. It generates a Keyboard interrupt request if the KBIE. 5 bit in KBIE register is set. Must be cleared by software.
4	KBF4	**Keyboard Line 4 Flag** Set by hardware when the Port line 4 detects a programmed level. It generates a Keyboard interrupt request if the KBIE. 4 bit in KBIE register is set. Must be cleared by software.
3	KBF3	**Keyboard Line 3 Flag** Set by hardware when the Port line 3 detects a programmed level. It generates a Keyboard interrupt request if the KBIE. 3 bit in KBIE register is set. Must be cleared by software.
2	KBF2	**Keyboard Line 2 Flag** Set by hardware when the Port line 2 detects a programmed level. It generates a Keyboard interrupt request if the KBIE. 2 bit in KBIE register is set. Must be cleared by software.
1	KBF1	**Keyboard Line 1 Flag** Set by hardware when the Port line 1 detects a programmed level. It generates a Keyboard interrupt request if the KBIE. 1 bit in KBIE register is set. Must be cleared by software.
0	KBF0	**Keyboard Line 0 Flag** Set by hardware when the Port line 0 detects a programmed level. It generates a Keyboard interrupt request if the KBIE. 0 bit in KBIE register is set. Must be cleared by software.

Reset Value = 0000 0000b

This register is read only access, all flags are automatically cleared by reading the register.

Error Conditions

The following flags in the SPSTA signal SPI error conditions:

Mode Fault (MODF)

Mode Fault error in Master mode SPI indicates that the level on the Slave Select ($\overline{SS}$) pin is inconsistent with the actual mode of the device. MODF is set to warn that there may be a multi-master conflict for system control. In this case, the SPI system is affected in the following ways:

- An SPI receiver/error CPU interrupt request is generated
- The SPEN bit in SPCON is cleared. This disables the SPI
- The MSTR bit in SPCON is cleared

When $\overline{SS}$ Disable (SSDIS) bit in the SPCON register is cleared, the MODF flag is set when the $\overline{SS}$ signal becomes '0'.

However, as stated before, for a system with one Master, if the $\overline{SS}$ pin of the Master device is pulled low, there is no way that another Master attempts to drive the network. In this case, to prevent the MODF flag from being set, software can set the SSDIS bit in the SPCON register and therefore making the $\overline{SS}$ pin as a general-purpose I/O pin.

Clearing the MODF bit is accomplished by a read of SPSTA register with MODF bit set, followed by a write to the SPCON register. SPEN Control bit may be restored to its original set state after the MODF bit has been cleared.

Write Collision (WCOL)

A Write Collision (WCOL) flag in the SPSTA is set when a write to the SPDAT register is done during a transmit sequence.

WCOL does not cause an interruption, and the transfer continues uninterrupted.

Clearing the WCOL bit is done through a software sequence of an access to SPSTA and an access to SPDAT.

Overrun Condition

An overrun condition occurs when the Master device tries to send several data Bytes and the Slave devise has not cleared the SPIF bit issuing from the previous data Byte transmitted. In this case, the receiver buffer contains the Byte sent after the SPIF bit was last cleared. A read of the SPDAT returns this Byte. All others Bytes are lost.

This condition is not detected by the SPI peripheral.

SS Error Flag (SSERR)

A Synchronous Serial Slave Error occurs when $\overline{SS}$ goes high before the end of a received data in slave mode. SSERR does not cause in interruption, this bit is cleared by writing 0 to SPEN bit (reset of the SPI state machine).

Interrupts

Two SPI status flags can generate a CPU interrupt requests:

Table 55. SPI Interrupts

Flag	Request
SPIF (SP data transfer)	SPI Transmitter Interrupt request
MODF (Mode Fault)	SPI Receiver/Error Interrupt Request (if SSDIS = '0')

Serial Peripheral data transfer flag, SPIF: This bit is set by hardware when a transfer has been completed. SPIF bit generates transmitter CPU interrupt requests.

Mode Fault flag, MODF: This bit becomes set to indicate that the level on the SS is inconsistent with the mode of the SPI. MODF with SSDIS reset, generates receiver/error CPU interrupt requests. When SSDIS is set, no MODF interrupt request is generated.

Figure 31 gives a logical view of the above statements.

Bit Number	Bit Mnemonic	Description			
1	SPR1	**SPR2**	**SPR1**	**SPR0**	**Serial Peripheral Rate**
		0	0	0	$F_{CLK\ PERIPH}$ /2
		0	0	1	$F_{CLK\ PERIPH}$ /4
		0	1	0	$F_{CLK\ PERIPH}$ /8
0	SPR0	0	1	1	$F_{CLK\ PERIPH}$ /16
		1	0	0	$F_{CLK\ PERIPH}$ /32
		1	0	1	$F_{CLK\ PERIPH}$ /64
		1	1	0	$F_{CLK\ PERIPH}$ /128
		1	1	1	Invalid

Reset Value = 0001 0100b

Not bit addressable

Serial Peripheral Status Register (SPSTA)

The Serial Peripheral Status Register contains flags to signal the following conditions:

- Data transfer complete
- Write collision
- Inconsistent logic level on $\overline{SS}$ pin (mode fault error)

Table 57 describes the SPSTA register and explains the use of every bit in the register.

Table 57. SPSTA Register

SPSTA - Serial Peripheral Status and Control register (0C4H)

7	6	5	4	3	2	1	0
SPIF	**WCOL**	**SSERR**	**MODF**	**-**	**-**	**-**	**-**

Bit Number	Bit Mnemonic	Description
7	SPIF	**Serial Peripheral Data Transfer Flag** Cleared by hardware to indicate data transfer is in progress or has been approved by a clearing sequence. Set by hardware to indicate that the data transfer has been completed.
6	WCOL	**Write Collision Flag** Cleared by hardware to indicate that no collision has occurred or has been approved by a clearing sequence. Set by hardware to indicate that a collision has been detected.
5	SSERR	**Synchronous Serial Slave Error Flag** Set by hardware when $\overline{SS}$ is deasserted before the end of a received data. Cleared by disabling the SPI (clearing SPEN bit in SPCON).
4	MODF	**Mode Fault** Cleared by hardware to indicate that the $\overline{SS}$ pin is at appropriate logic level, or has been approved by a clearing sequence. Set by hardware to indicate that the $\overline{SS}$ pin is at inappropriate logic level.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.

Bit Number	Bit Mnemonic	Description
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.

Reset Value = 00X0 XXXXb

Not Bit addressable

Serial Peripheral DATa Register (SPDAT)

The Serial Peripheral Data Register (Table 58) is a read/write buffer for the receive data register. A write to SPDAT places data directly into the shift register. No transmit buffer is available in this model.

A Read of the SPDAT returns the value located in the receive buffer and not the content of the shift register.

Table 58. SPDAT Register

SPDAT - Serial Peripheral Data Register (0C5H)

7	6	5	4	3	2	1	0
R7	**R6**	**R5**	**R4**	**R3**	**R2**	**R1**	**R0**

Reset Value = Indeterminate

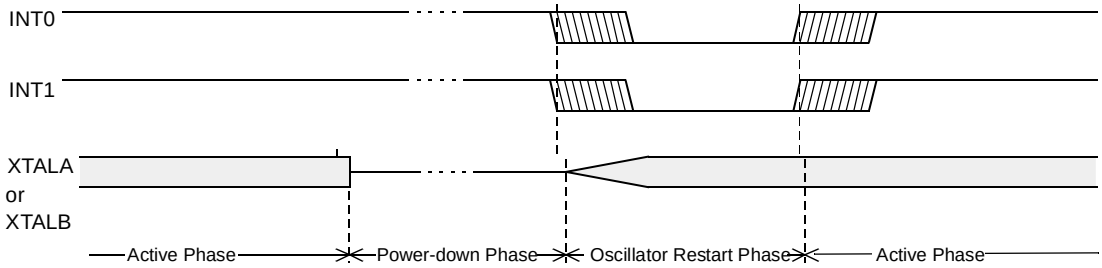
R7:R0: Receive data bits

SPCON, SPSTA and SPDAT registers may be read and written at any time while there is no on-going exchange. However, special care should be taken when writing to them while a transmission is on-going:

- Do not change SPR2, SPR1 and SPR0
- Do not change CPHA and CPOL
- Do not change MSTR
- Clearing SPEN would immediately disable the peripheral
- Writing to the SPDAT will cause an overflow.

be the one following the instruction that puts the AT89C51RB2/RC2 into Power-down mode.

Figure 34. Power-down Exit Waveform



Exit from Power-down by reset redefines all the SFRs, exit from Power-down by external interrupt does no affect the SFRs.

Exit from Power-down by either reset or external interrupt or keyboard interrupt does not affect the internal RAM content.

Note: If idle mode is activated with Power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

Table 62 shows the state of ports during idle and power-down modes.

Table 62. State of Ports

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data(1)	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data(1)	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

Port 0 can force a 0 level. A "one" will leave port floating.

Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0.As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 64. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
DPU	**-**	**M0**	**-**	**XRS1**	**XRS0**	**EXTRAM**	**AO**

Bit Number	Bit Mnemonic	Description
7	DPU	**Disable Weak Pull-up** Cleared to activate the permanent weak pull up when latch data is logic 1 Set to disactive the weak pull-up.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	M0	**Pulse Length** Cleared to stretch MOVX control: the $\overline{RD}$ and the $\overline{WR}$ pulse length is 6 clock periods (default). Set to stretch MOVX control: the $\overline{RD}$ and the $\overline{WR}$ pulse length is 30 clock periods.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	XRS1	**XRAM Size** XRS1 XRS0 XRAM size 0 0 256 Bytes (default) 0 1 512 Bytes 1 0 768 Bytes 1 1 1024 Bytes
2	XRS0	
1	EXTRAM	**EXTRAM Bit** Cleared to access internal XRAM using movx @ $\overline{Ri}$ @ DPTR. Set to access external memory. Programmed by hardware after Power-up regarding Hardware Security Byte (HSB), default setting, XRAM selected.
0	AO	**ALE Output Bit** Cleared, ALE is emitted at a constant rate of 1/6 the oscillator frequency (or 1/3 if X2 mode is used). (default) Set, ALE is active only during a MOVX or MOVC instruction is used.

Table 66. Program Lock Bits

Program Lock Bits				
Security Level	**LB0**	**LB1**	**LB2**	**Protection Description**
1	U	U	U	No program lock features enabled.
2	P	U	U	MOVC instruction executed from external program memory is disabled from fetching code Bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further parallel programming of the Flash is disabled. ISP and software programming with API are still allowed.
3	X	P	U	Same as 2, also verify through parallel programming interface is disabled.
4	X	X	P	Same as 3, also external execution is disabled. (Default)

Note: U: unprogrammed or "one" level.
P: programmed or "zero" level.
X: don't care
WARNING: Security level '2' and '3' should only be programmed after Flash and code verification.

These security bits protect the code access through the parallel programming interface. They are set by default to level 4. The code access through the ISP is still possible and is controlled by the "software security bits" which are stored in the extra Flash memory accessed by the ISP firmware.

To load a new application with the parallel programmer, a chip erase must first be done. This will set the HSB in its inactive state and will erase the Flash memory. The part reference can always be read using Flash parallel programming modes.

Default Values

The default value of the HSB provides parts ready to be programmed with ISP:

- BLJB: Programmed force ISP operation.
- X2: Unprogrammed to force X1 mode (Standard Mode).
- XRAM: Unprogrammed to valid XRAM
- LB2-0: Security level four to protect the code from a parallel access with maximum security.

Software Registers

Several registers are used, in factory and by parallel programmers, to make copies of hardware registers contents. These values are used by Atmel ISP.

These registers are in the "Extra Flash Memory" part of the Flash memory. This block is also called "XAF" or eXtra Array Flash. They are accessed in the following ways:

- Commands issued by the parallel memory programmer.
- Commands issued by the ISP software.
- Calls of API issued by the application software.

Several software registers are described in Table 67.

Table 67. Default Values

Mnemonic	Definition	Default value	Description
SBV	Software Boot Vector	FCh	
HSB	Hardware security Byte	101x 1011b	
BSB	Boot Status Byte	0FFh	
SSB	Software Security Byte	FFh	
	Copy of the Manufacturer Code	58h	ATMEL
	Copy of the Device ID #1: Family Code	D7h	C51 X2, Electrically Erasable
	Copy of the Device ID #2: memories size and type	F7h	AT89C51RB2/RC2 32KB
		FBh	AT89C51RB2/RC2 16 KB
	Copy of the Device ID #3: name and revision	EFh	AT89C51RB2/RC2 32KB, Revision 0
		FFh	AT89C51RB2/RC2 16 KB, Revision 0

After programming the part by ISP, the BSB must be cleared (00h) in order to allow the application to boot at 0000h.

The content of the Software Security Byte (SSB) is described in Table 67 and Table 69.

To assure code protection from a parallel access, the HSB must also be at the required level.

Table 68. Software Security Byte

7	6	5	4	3	2	1	0
-	-	-	-	-	-	LB1	LB0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** Do not clear this bit.
6	-	**Reserved** Do not clear this bit.
5	-	**Reserved** Do not clear this bit.
4	-	**Reserved** Do not clear this bit.
3	-	**Reserved** Do not clear this bit.
2	-	**Reserved** Do not clear this bit.
1-0	LB1-0	**User Memory Lock Bits** see Table 69

The two lock bits provide different levels of protection for the on-chip code and data, when programmed as shown in Table 69.

Table 69. Program Lock Bits of the SSB

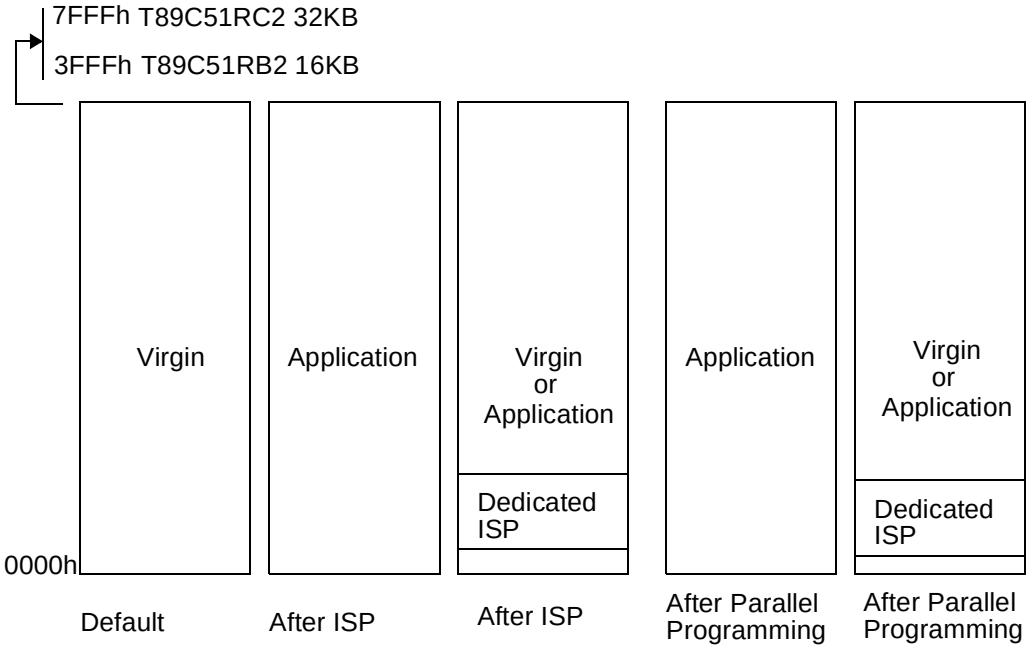
Program Lock Bits			
Security level	**LB0**	**LB1**	**Protection Description**
1	U	U	No program lock features enabled.
2	P	U	ISP programming of the Flash is disabled.
3	X	P	Same as 2, also verify through ISP programming interface is disabled.

Note: U: unprogrammed or "one" level.
P: programmed or "zero" level.
X: don't care
WARNING: Security level 2 and 3 should only be programmed after Flash and code verification.

Flash Memory Status

AT89C51RB2/RC2 parts are delivered in standard with the ISP boot in the Flash memory. After ISP or parallel programming, the possible contents of the Flash memory are summarized on Figure 35.

Figure 35. Flash Memory Possible Contents



Memory Organization

In the AT89C51RB2/RC2, the lowest 16K or 32K of the 64 KB program memory address space is filled by internal Flash.

When the $\overline{EA}$ pin is high, the processor fetches instructions from internal program Flash. Bus expansion for accessing program memory from 16K or 32K upward automatic since external instruction fetches occur automatically when the program counter exceeds 3FFFh (16K) or 7FFFh (32K). If the $\overline{EA}$ pin is tied low, all program memory fetches are from external memory.

ISP Commands Summary

Table 73. ISP Commands Summary

Command	Command Name	Data[0]	Data[1]	Command Effect
00h	Program Data			Program Nb Data Byte. Bootloader will accept up to 128 (80h) data Bytes. The data Bytes should be 128 Byte page Flash boundary.
03h	Write Function	01h	00h	Erase block0 (0000h-1FFFh)
			20h	Erase block1 (2000h-3FFFh)
			40h	Erase block2 (4000h-7FFFh)
			80h	Erase block3 (8000h- BFFFh)
			C0h	Erase block4 (C000h- FFFFh)
		03h	00h	Hardware Reset
		04h	00h	Erase SBV & BSB
		05h	00h	Program SSB level 1
			01h	Program SSB level 2
		06h	00h	Program BSB (value to write in data[2])
			01h	Program SBV (value to write in data[2])
		07h	-	Full Chip Erase (This command needs about 6 sec to be executed)
		0Ah	02h	Program Osc fuse (value to write in data[2])
			04h	Program BLJB fuse (value to write in data[2])
			08h	Program X2 fuse (value to write in data[2])
04h	Display Function	Data[0:1] = start address Data [2:3] = end address Data[4] = 00h -> Display data Data[4] = 01h -> Blank check		Display Data Note: The maximum number of data that can be read with a single command frame (difference between start and end address) is 1kbyte.
				Blank Check
05h	Read Function	00h	00h	Manufacturer ID
			01h	Device ID #1
			02h	Device ID #2
			03h	Device ID #3
		07h	00h	Read SSB
			01h	Read BSB
			02h	Read SBV
			06h	Read Extra Byte
		0Bh	00h	Read Hardware Byte
		0Eh	00h	Read Device Boot ID1
			01h	Read Device Boot ID2
		0Fh	00h	Read Bootloader Version

API Call Description

Several Application Program Interface (API) calls are available for use by an application program to permit selective erasing and programming of Flash pages. All calls are made through a common interface, PGM_MTP. The programming functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FFF0h. Results are returned in the registers.

When several Bytes have to be programmed, it is highly recommended to use the Atmel API "PROGRAM DATA PAGE" call. Indeed, this API call writes up to 128 Bytes in a single command.

All routines for software access are provided in the C Flash driver available at Atmel's web site.

The API calls description and arguments are shown in Table 74.

Table 74. API Call Summary

Command	R1	A	DPTR0	DPTR1	Returned Value	Command Effect
READ MANUF ID	00h	XXh	0000h	XXh	ACC = Manufacturer Id	Read Manufacturer identifier
READ DEVICE ID1	00h	XXh	0001h	XXh	ACC = Device Id 1	Read Device identifier 1
READ DEVICE ID2	00h	XXh	0002h	XXh	ACC = Device Id 2	Read Device identifier 2
READ DEVICE ID3	00h	XXh	0003h	XXh	ACC = Device Id 3	Read Device identifier 3
ERASE BLOCK	01h	XXh	DPH = 00h	00h	ACC = DPH	Erase block 0
			DPH = 20h			Erase block 1
			DPH = 40h			Erase block 2
PROGRAM DATA BYTE	02h	Vaue to write	Address of byte to program	XXh	ACC = 0: DONE	Program up one data byte in the on-chip flash memory.
PROGRAM SSB	05h	XXh	DPH = 00h DPL = 00h	00h	ACC = SSB value	Set SSB level 1
			DPH = 00h DPL = 01h			Set SSB level 2
			DPH = 00h DPL = 10h			Set SSB level 0
			DPH = 00h DPL = 11h			Set SSB level 1
PROGRAM BSB	06h	New BSB value	0000h	XXh	none	Program boot status byte
PROGRAM SBV	06h	New SBV value	0001h	XXh	none	Program software boot vector
READ SSB	07h	XXh	0000h	XXh	ACC = SSB	Read Software Security Byte
READ BSB	07h	XXh	0001h	XXh	ACC = BSB	Read Boot Status Byte
READ SBV	07h	XXh	0002h	XXh	ACC = SBV	Read Software Boot Vector
PROGRAM DATA PAGE	09h	Number of byte to program	Address of the first byte to program in the Flash memory	Address in XRAM of the first data to program	ACC = 0: DONE	Program up to 128 bytes in user Flash. Remark: number of bytes to program is limited such as the Flash write remains in a single 128 bytes page. Hence, when ACC is 128, valid values of DPL are 00h, or, 80h.

T_A = -40°C to +85°C; V_{SS} = 0V;

V_{CC} =2.7V to 5.5V and F = 0 to 40 MHz (both internal and external code execution)

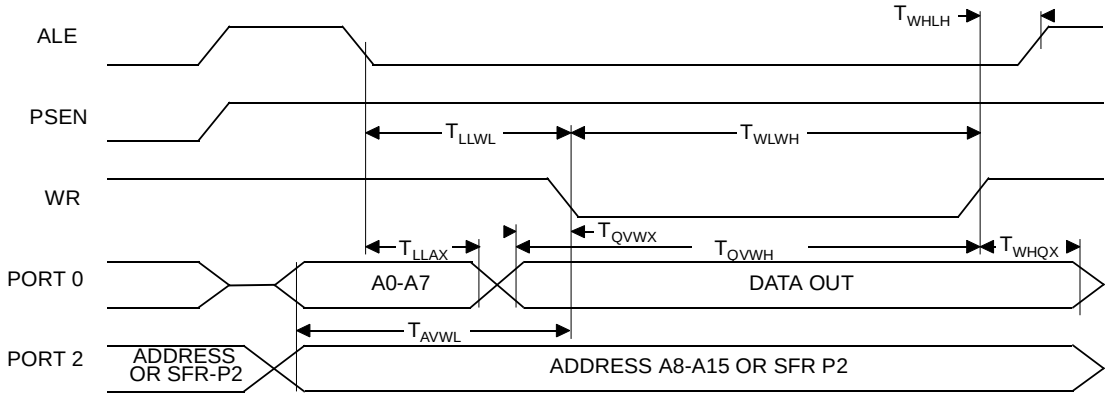
V_{CC} =4.5V to 5.5V and F = 0 to 60 MHz (internal code execution only) (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH1}	Output High Voltage, port 0, ALE, $\overline{PSEN}$	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	V_{CC} = 5V ± 10% I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA
		0.9 V_{CC}			V	VCC = 2.7V to 5.5V I_{OH} = -10 µA
R_{RST}	RST Pulldown Resistor	50	200[5]	250	kΩ	
I_{IL}	Logical 0 Input Current ports 1, 2, 3, 4 and 5			-50	µA	V_{IN} = 0.45V
I_{LI}	Input Leakage Current for P0 only			±10	µA	0.45V < V_{IN} < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4			-650	µA	V_{IN} = 2.0V
C_{IO}	Capacitance of I/O Buffer			10	pF	Fc = 3 MHz T_A = 25°C
I_{PD}	Power Down Current		100	150	µA	4.5V < V_{CC} < 5.5V[3]
I_{CCOP}	Power Supply Current on normal mode			0.4 x Frequency (MHz) + 5	mA	V_{CC} = 5.5V[1]
I_{CCIDLE}	Power Supply Current on idle mode			0.3 x Frequency (MHz) + 5	mA	V_{CC} = 5.5V[1]
I_{CCProg}	Power Supply Current during flash Write / Erase		0.4 x Frequency (MHz) + 20		mA	V_{CC} = 5.5V[8]

Notes:
1. Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 49.), V_{IL} = V_{SS} + 0.5V,
   V_{IH} = V_{CC} - 0.5V; XTAL2 N.C.; $\overline{EA}$ = RST = Port 0 = V_{CC}. I_{CC} would be slightly higher if a crystal oscillator used (see Figure 46).
2. Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5V, V_{IH} = V_{CC} - 0.5V; XTAL2 N.C; Port 0 = V_{CC}; $\overline{EA}$ = RST = V_{SS} (see Figure 47).
3. Power Down I_{CC} is measured with all output pins disconnected; $\overline{EA}$ = V_{SS}, PORT 0 = V_{CC}; XTAL2 NC.; RST = V_{SS} (see Figure 48).
4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi V_{OL} peak 0.6V. A Schmitt Trigger use is not necessary.
5. Typical are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
6. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
7. For other values, please contact your sales office.
8. Icc Flash Write operation current while an on-chip flash page write is on going.
9. Flash Retention is guaranteed with the same formula for V_{CC} Min down to 0.

Symbol	Type	Standard Clock	X2 Clock	X Parameter for - M Range	X Parameter for - L Range	Units
T_{RLRH}	Min	6 T - x	3 T - x	25	25	ns
T_{WLWH}	Min	6 T - x	3 T - x	25	25	ns
T_{RLDV}	Max	5 T - x	2.5 T - x	30	30	ns
T_{RHDX}	Min	x	x	0	0	ns
T_{RHDZ}	Max	2 T - x	T - x	25	25	ns
T_{LLDV}	Max	8 T - x	4T -x	45	45	ns
T_{AVDV}	Max	9 T - x	4.5 T - x	65	65	ns
T_{LLWL}	Min	3 T - x	1.5 T - x	30	30	ns
T_{LLWL}	Max	3 T + x	1.5 T + x	30	30	ns
T_{AVWL}	Min	4 T - x	2 T - x	30	30	ns
T_{QVWX}	Min	T - x	0.5 T - x	20	20	ns
T_{QVWH}	Min	7 T - x	3.5 T - x	20	20	ns
T_{WHQX}	Min	T - x	0.5 T - x	15	15	ns
T_{RLAZ}	Max	x	x	0	0	ns
T_{WHLH}	Min	T - x	0.5 T - x	20	20	ns
T_{WHLH}	Max	T + x	0.5 T + x	20	20	ns

External Data Memory Write Cycle



Datasheet Change Log

Changes from 4180A-08/02 to 4180B-04/03

1. Changed the endurance of Flash to 100, 000 Write/Erase cycles.
2. Added note on Flash retention formula for V_{IH1}, in Section “DC Parameters for Standard Voltage”, page 107.

Changes from 4180B-04/03 to 4180C-12/03

1. Max frequency update for 4.5 to 5.5V range up to 60 MHz (internal code execution).

Changes from 4180C-12/03 - 4180D - 06/05

1. Added Green product ordering information. Page 119.

Changes from 4180D - 06/05 to 4180E - 10/06

1. Correction to PDIL40 figure on page 9.