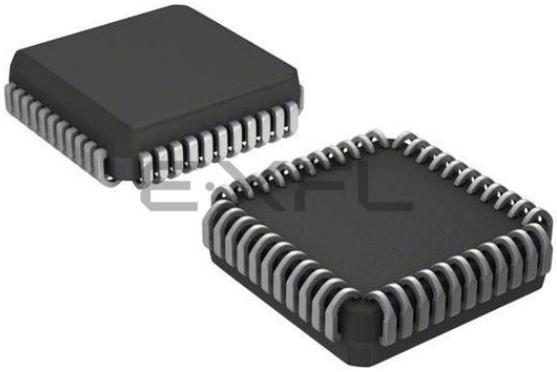

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	80C51
Core Size	8-Bit
Speed	40MHz
Connectivity	SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c51rb2-slsul

The AT89C51RB2/RC2 retains all features of the 80C52 with 256 Bytes of internal RAM, a 9-source 4-level interrupt controller and three timer/counters.

In addition, the AT89C51RB2/RC2 has a Programmable Counter Array, an XRAM of 1024 Bytes, a Hardware Watchdog Timer, a Keyboard Interface, an SPI Interface, a more versatile serial channel that facilitates multiprocessor communication (EUART) and a speed improvement mechanism (X2 mode).

The Pinout is the standard 40/44 pins of the C52.

The fully static design reduces system power consumption of the AT89C51RB2/RC2 by allowing it to bring the clock frequency down to any value, even DC, without loss of data.

The AT89C51RB2/RC2 has 2 software-selectable modes of reduced activity and 8-bit clock prescaler for further reduction in power consumption. In Idle mode, the CPU is frozen while the peripherals and the interrupt system are still operating. In power-down mode, the RAM is saved and all other functions are inoperative.

The added features of the AT89C51RB2/RC2 make it more powerful for applications that need pulse width modulation, high speed I/O and counting capabilities such as alarms, motor control, corded phones, and smart card readers.

Table 1. Memory Size

Part Number	Flash (Bytes)	XRAM (Bytes)	TOTAL RAM (Bytes)	I/O
AT89C51RB2	16K	1024	1280	32
AT89C51RC2	32K	1024	1280	32
AT89C51IC2	32K	1024	1280	32

Oscillator

To optimize the power consumption and execution time needed for a specific task, an internal, prescaler feature has been implemented between the oscillator and the CPU and peripherals.

Registers

Table 13. CKRL Register

CKRL – Clock Reload Register (97h)

7	6	5	4	3	2	1	0
CKRL7	CKRL6	CKRL5	CKRL4	CKRL3	CKRL2	CKRL1	CKRL0

Bit Number	Mnemonic	Description
7:0	CKRL	**Clock Reload Register** Prescaler value

Reset Value = 1111 1111b
Not bit addressable

Table 14. PCON Register

PCON – Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial Port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial Port Mode bit 0** Cleared to select SM0 bit in SCON register. Set to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-off Flag** Cleared to recognize next reset type. Set by hardware when V_{CC} rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General-purpose Flag** Cleared by software for general-purpose usage. Set by software for general-purpose usage.
2	GF0	**General-purpose Flag** Cleared by software for general-purpose usage. Set by software for general-purpose usage.
1	PD	**Power-down Mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle Mode bit** Cleared by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b Not bit addressable

Table 15. CKCON0 Register

CKCON0 - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	WDX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2

Bit Number	Bit Mnemonic	Description
7	Reserved	
6	WDX2	**Watchdog Clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
5	PCAX2	**Programmable Counter Array Clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
4	SIX2	**Enhanced UART Clock (Mode 0 and 2)** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
3	T2X2	**Timer 2 Clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
2	T1X2	**Timer 1 Clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
1	T0X2	**Timer0 Clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
0	X2	**CPU Clock** Cleared to select 12 clock periods per machine cycle (STD, X1 mode) for CPU and all the peripherals. Set to select 6 clock periods per machine cycle (X2 mode) and to enable the individual peripherals'X2' bits. Programmed by hardware after Power-up regarding Hardware Security Byte (HSB), Default setting, X2 is cleared.

Reset Value = 0000 000'HSB. X2'b (see Table 65 "Hardware Security Byte")
Not bit addressable

- Instructions that use indirect addressing access the Upper 128 Bytes of data RAM. For example: MOV @R0, # data where R0 contains 0A0h, accesses the data Byte at address 0A0h, rather than P2 (whose address is 0A0h).
- The XRAM Bytes can be accessed by indirect addressing, with EXTRAM bit cleared and MOVX instructions. This part of memory that is physically located on-chip, logically occupies the first Bytes of external data memory. The bits XRS0 and XRS1 are used to hide a part of the available XRAM as explained in Table 18. This can be useful if external peripherals are mapped at addresses already used by the internal XRAM.
- With EXTRAM = 0, the XRAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. An access to XRAM will not affect ports P0, P2, P3.6 (WR) and P3.7 (RD). For example, with EXTRAM = 0, MOVX @R0, # data where R0 contains 0A0H, accesses the XRAM at address 0A0H rather than external memory. An access to external data memory locations higher than the accessible size of the XRAM will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, with P0 and P2 as data/address busses, and P3.6 and P3.7 as write and read timing signals. Accesses to XRAM above 0FFH can only be done by the use of DPTR.
- With EXTRAM = 1, MOVX @RI and MOVX @DPTR will be similar to the standard 80C51. MOVX @ Ri will provide an eight-bit address multiplexed with data on Port0 and any output port pins can be used to output higher order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a sixteen-bit address. Port2 outputs the high-order eight address bits (the contents of DPH) while Port0 multiplexes the low-order eight address bits (DPL) with data. MOVX @ RI and MOVX @DPTR will generate either read or write signals on P3.6 ($\overline{WR}$) and P3.7 ($\overline{RD}$).

The stack pointer (SP) may be located anywhere in the 256 Bytes RAM (lower and upper RAM) internal data memory. The stack may not be located in the XRAM.

The M0 bit allows to stretch the XRAM timings; if M0 is set, the read and write pulses are extended from 6 to 30 clock periods. This is useful to access external slow peripherals.

Timer 2

The Timer 2 in the AT89C51RB2/RC2 is the standard C52 Timer 2.

It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2 are cascaded. It is controlled by T2CON (Table 20) and T2MOD (Table 21) registers. Timer 2 operation is similar to Timer 0 and Timer 1C/$\overline{T2}$ selects F_{OSC}/12 (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to increment by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/$\overline{RL2}$ (T2CON).

see the Atmel 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

Auto-reload Mode

The auto-reload mode configures Timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, Timer 2 behaves as in 80C52 (see the Atmel C51 Microcontroller Hardware description). If DCEN bit is set, Timer 2 acts as an Up/down timer/counter as shown in Figure 9. In this mode the T2EX pin controls the direction of count.

When T2EX is high, Timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, Timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when Timer 2 overflows or underflows according to the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.

Registers

Table 22. CMOD Register

CMOD – PCA Counter Mode Register (D9h)

7	6	5	4	3	2	1	0
CIDL	**WDTE**	**-**	**-**	**-**	**CPS1**	**CPS0**	**ECF**

Bit Number	Bit Mnemonic	Description
7	CIDL	**Counter Idle Control** Cleared to program the PCA Counter to continue functioning during idle Mode. Set to program PCA to be gated off during idle.
6	WDTE	**Watchdog Timer Enable** Cleared to disable Watchdog Timer function on PCA Module 4. Set to enable Watchdog Timer function on PCA Module 4.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	CPS1	**PCA Count Pulse Select** CPS1 CPS0 Selected PCA input 0 0 Internal clock $F_{CLK\ PERIPH}/6$ 0 1 Internal clock $F_{LK\ PERIPH}/2$ 1 0 Timer 0 Overflow 1 1 External clock at ECI/P1.2 pin (max rate = fCLK PERIPH/ 4)
1	CPS0	
0	ECF	**PCA Enable Counter Overflow Interrupt** Cleared to disable CF bit in CCON to inhibit an interrupt. Set to enable CF bit in CCON to generate an interrupt.

Reset Value = 00XX X000b
Not bit addressable

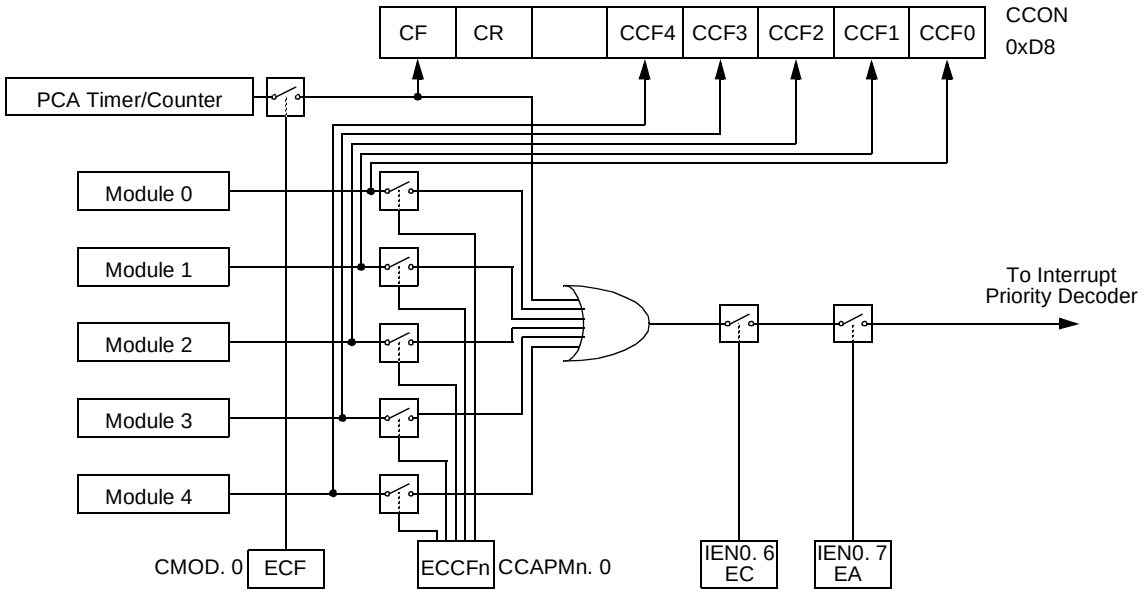
The CMOD register includes three additional bits associated with the PCA.

- The CIDL bit which allows the PCA to stop during idle mode.
- The WDTE bit which enables or disables the watchdog function on Module 4.
- The ECF bit which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows.

The CCON register contains the run control bit for the PCA and the flags for the PCA timer (CF) and each Module (see Table 23).

- Bit CR (CCON. 6) must be set by software to run the PCA. The PCA is shut off by clearing this bit.
- Bit CF: The CF bit (CCON. 7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software.
- Bits 0 through 4 are the flags for the Modules (bit 0 for Module 0, bit 1 for Module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

Figure 12. PCA Interrupt System



PCA Modules: each one of the five compare/capture Modules has six possible functions. It can perform:

- 16-bit Capture, positive-edge triggered
- 16-bit Capture, negative-edge triggered
- 16-bit Capture, both positive and negative-edge triggered
- 16-bit Software Timer
- 16-bit High-speed Output
- 8-bit Pulse Width Modulator

In addition, Module 4 can be used as a Watchdog Timer.

Each Module in the PCA has a special function register associated with it. These registers are: CCAPM0 for Module 0, CCAPM1 for Module 1, etc. (see Table 24). The registers contain the bits that control the mode that each Module will operate in.

- The ECCF bit (CCAPMn. 0 where n = 0, 1, 2, 3, or 4 depending on the Module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated Module.
- PWM (CCAPMn. 1) enables the pulse width modulation mode.
- The TOG bit (CCAPMn. 2) when set causes the CEX output associated with the Module to toggle when there is a match between the PCA counter and the Module's capture/compare register.
- The match bit MAT (CCAPMn. 3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the Module's capture/compare register.
- The next two bits CAPN (CCAPMn. 4) and CAPP (CCAPMn. 5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition.
- The last bit in the register ECOM (CCAPMn. 6) when set enables the comparator function.

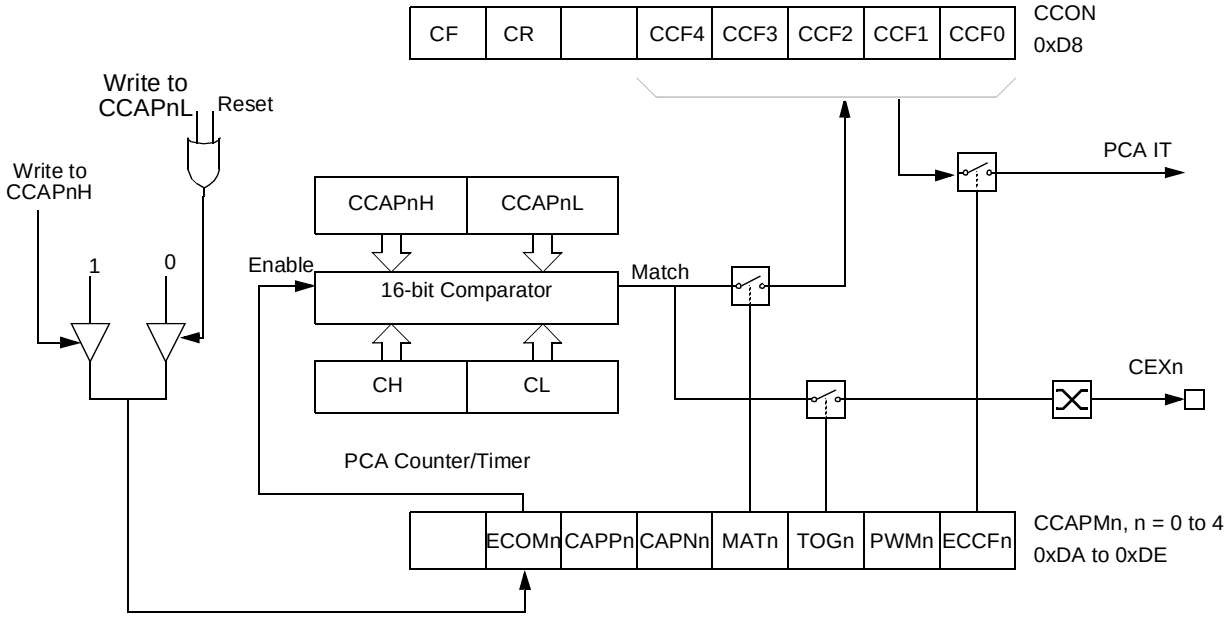
Table 24 shows the CCAPMn settings for the various PCA functions.

High-speed Output Mode

In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the modules capture registers. To activate this mode the TOG, MAT, and ECOM bits in the modules CCAPMn SFR must be set (see Figure 15).

A prior write must be done to CCAPnL and CCAPnH before writing the ECOMn bit.

Figure 15. PCA High-speed Output Mode



Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non-zero value, otherwise an unwanted match could occur.

Once ECOM is set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

Table 42. BDRCON Register

BDRCON - Baud Rate Control Register (9Bh)

7	6	5	4	3	2	1	0
-	-	-	BRR	TBCK	RBCK	SPD	SRC

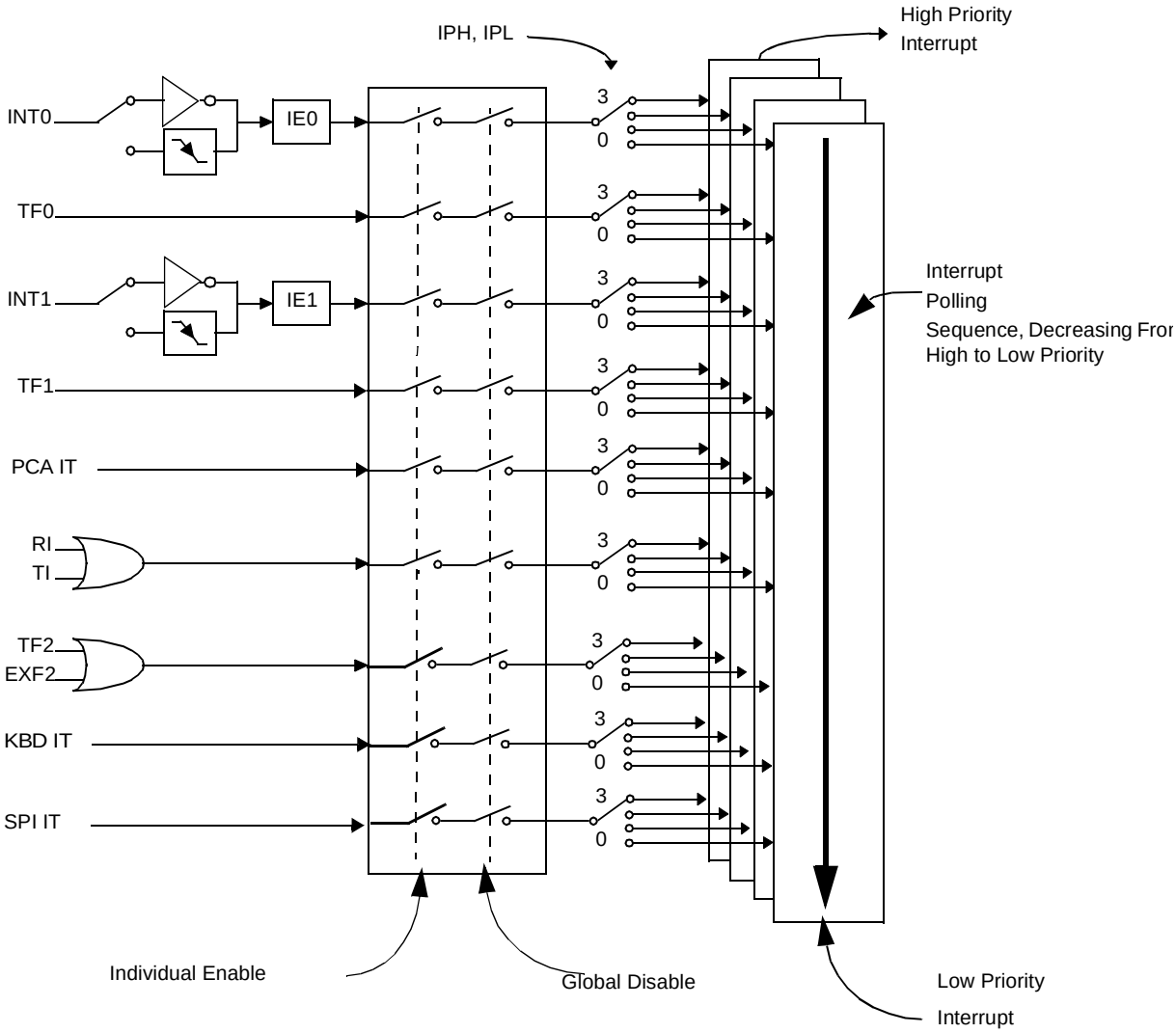
Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	BRR	**Baud Rate Run Control bit** Cleared to stop the internal Baud Rate Generator. Set to start the internal Baud Rate Generator.
3	TBCK	**Transmission Baud rate Generator Selection bit for UART** Cleared to select Timer 1 or Timer 2 for the Baud Rate Generator. Set to select internal Baud Rate Generator.
2	RBCK	**Reception Baud Rate Generator Selection bit for UART** Cleared to select Timer 1 or Timer 2 for the Baud Rate Generator. Set to select internal Baud Rate Generator.
1	SPD	**Baud Rate Speed Control bit for UART** Cleared to select the SLOW Baud Rate Generator. Set to select the FAST Baud Rate Generator.
0	SRC	**Baud Rate Source select bit in Mode 0 for UART** Cleared to select $F_{OSC}/12$ as the Baud Rate Generator ($F_{CLK\ PERIPH}/6$ in X2 mode). Set to select the internal Baud Rate Generator for UARTs in mode 0.

Reset Value = XXX0 0000b
Not bit addressablef

Interrupt System

The AT89C51RB2/RC2 has a total of 9 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (timers 0, 1 and 2), the serial port interrupt, SPI interrupt, Keyboard interrupt and the PCA global interrupt. These interrupts are shown in Figure 22.

Figure 22. Interrupt Control System



Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (Table 45 and Table 47). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (Table 48) and in the Interrupt Priority High register (Table 46 and Table 47) shows the bit values and priority levels associated with each combination.

Table 44. IENO Register

IEN0 - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	EC	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	**Enable All Interrupt Bit** Cleared to disable all interrupts. Set to enable all interrupts.
6	EC	**PCA Interrupt Enable Bit** Cleared to disable. Set to enable.
5	ET2	**Timer 2 Overflow Interrupt Enable Bit** Cleared to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	**Serial Port Enable Bit** Cleared to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	**Timer 1 Overflow Interrupt Enable Bit** Cleared to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	**External Interrupt 1 Enable Bit** Cleared to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	**Timer 0 Overflow Interrupt Enable Bit** Cleared to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	**External Interrupt 0 Enable Bit** Cleared to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0000 0000b
Bit addressable

Interrupt Sources and Vector Addresses

Table 50. Interrupt Sources and Vector Addresses

Number	Polling Priority	Interrupt Source	Interrupt Request	Vector Address
0	0	Reset		0000h
1	1	INT0	IE0	0003h
2	2	Timer 0	TF0	000Bh
3	3	INT1	IE1	0013h
4	4	Timer 1	IF1	001Bh
5	6	UART	RI+TI	0023h
6	7	Timer 2	TF2+EXF2	002Bh
7	5	PCA	CF + CCFn (n = 0-4)	0033h
8	8	Keyboard	KBDIT	003Bh
9	9	SPI	SPIIT	004Bh

Flash Registers and Memory Map

The AT89C51RB2/RC2 Flash memory uses several registers for its management:

- Hardware registers can only be accessed through the parallel programming modes which are handled by the parallel programmer.
- Software registers are in a special page of the Flash memory which can be accessed through the API or with the parallel programming modes. This page, called "Extra Flash Memory", is not in the internal Flash program memory addressing space.

Hardware Register

The only hardware register of the AT89C51RB2/RC2 is called Hardware Security Byte (HSB).

Table 65. Hardware Security Byte (HSB)

7	6	5	4	3	2	1	0
X2	**BLJB**	**-**	**-**	**XRAM**	**LB2**	**LB1**	**LB0**

Bit Number	Bit Mnemonic	Description
7	X2	**X2 Mode** Programmed (‘0’ value) to force X2 mode (6 clocks per instruction) after reset. Unprogrammed (‘1’ Value) to force X1 mode, Standard Mode, after reset (Default).
6	BLJB	**Boot Loader Jump Bit** Unprogrammed (‘1’ value) to start the user’s application on next reset at address 0000h. Programmed (‘0’ value) to start the boot loader at address F800h on next reset (Default).
5	-	**Reserved**
4	-	**Reserved**
3	XRAM	**XRAM Config Bit (only programmable by programmer tools)** Programmed to inhibit XRAM after reset. Unprogrammed, this bit to valid XRAM after reset (Default).
2-0	LB2-0	**User Memory Lock Bits (only programmable by programmer tools)** See Table 66.

Boot Loader Jump Bit (BLJB)

One bit of the HSB, the BLJB bit, is used to force the boot address:

- When this bit is programmed (‘1’ value) the boot address is 0000h.
- When this bit is unprogrammed (‘1’ value) the boot address is F800h. By default, this bit is unprogrammed and the ISP is enabled.

Flash Memory Lock Bits

The three lock bits provide different levels of protection for the on-chip code and data, when programmed as shown in Table 66.

Example

```
Display data from address 0000h to 0020h
HOST          : 05 0000 04 0000 0020 00 D7
BOOTLOADER    : 05 0000 04 0000 0020 00 D7
BOOTLOADER    0000=-----data------ CR LF   (16 data)
BOOTLOADER    0010=-----data------ CR LF   (16 data)
BOOTLOADER    0020=data CR LF              ( 1 data)
```

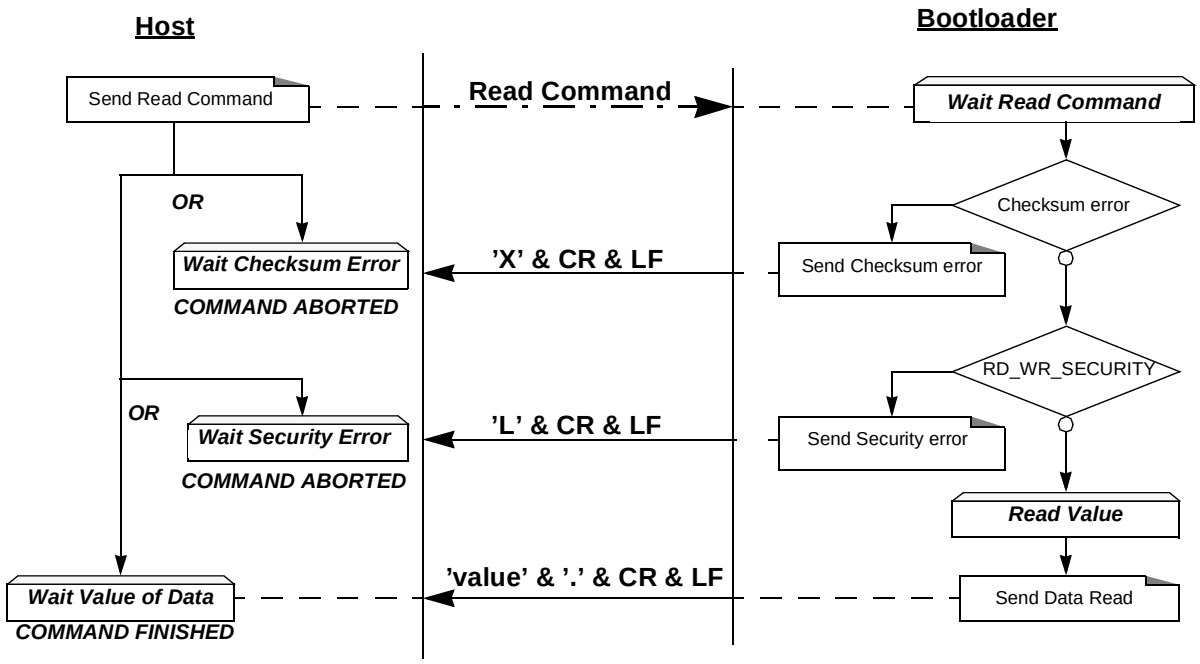
Read Function

This flow is similar for the following frames:

- Reading Frame
- EOF Frame/Atmel Frame (only reading Atmel Frame)

Description

Figure 45. Read Flow



Example

```
Read function (read SBV)
HOST          : 02 0000 05 07 02 F0
BOOTLOADER    : 02 0000 05 07 02 F0 Value . CR LF
Atmel Read function (read Bootloader version)
HOST          : 02 0000 01 02 00 FB
BOOTLOADER    : 02 0000 01 02 00 FB Value . CR LF
```

ISP Commands Summary

Table 73. ISP Commands Summary

Command	Command Name	Data[0]	Data[1]	Command Effect
00h	Program Data			Program Nb Data Byte. Bootloader will accept up to 128 (80h) data Bytes. The data Bytes should be 128 Byte page Flash boundary.
03h	Write Function	01h	00h	Erase block0 (0000h-1FFFh)
			20h	Erase block1 (2000h-3FFFh)
			40h	Erase block2 (4000h-7FFFh)
			80h	Erase block3 (8000h- BFFFh)
			C0h	Erase block4 (C000h- FFFFh)
		03h	00h	Hardware Reset
		04h	00h	Erase SBV & BSB
		05h	00h	Program SSB level 1
			01h	Program SSB level 2
		06h	00h	Program BSB (value to write in data[2])
			01h	Program SBV (value to write in data[2])
		07h	-	Full Chip Erase (This command needs about 6 sec to be executed)
		0Ah	02h	Program Osc fuse (value to write in data[2])
			04h	Program BLJB fuse (value to write in data[2])
			08h	Program X2 fuse (value to write in data[2])
04h	Display Function	Data[0:1] = start address Data [2:3] = end address Data[4] = 00h -> Display data Data[4] = 01h -> Blank check		Display Data Note: The maximum number of data that can be read with a single command frame (difference between start and end address) is 1kbyte.
				Blank Check
05h	Read Function	00h	00h	Manufacturer ID
			01h	Device ID #1
			02h	Device ID #2
			03h	Device ID #3
		07h	00h	Read SSB
			01h	Read BSB
			02h	Read SBV
			06h	Read Extra Byte
		0Bh	00h	Read Hardware Byte
		0Eh	00h	Read Device Boot ID1
			01h	Read Device Boot ID2
		0Fh	00h	Read Bootloader Version

Electrical Characteristics

Absolute Maximum Ratings

C = commercial.....0°C to 70°C
I = industrial .....-40°C to 85°C
Storage Temperature ..... -65°C to + 150°C
Voltage on V_{CC} to V_{SS} (standard voltage).....-0.5V to + 6.5V
Voltage on V_{CC} to V_{SS} (low voltage).....-0.5V to + 4.5V
Voltage on Any Pin to V_{SS}.....-0.5V to V_{CC} + 0.5V
Power Dissipation ..... 1 W

Note: Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
Power dissipation value is based on the maximum allowable die temperature and the thermal resistance of the package.

DC Parameters for Standard Voltage

T_A = -40°C to +85°C; V_{SS} = 0V;

V_{CC} =2.7V to 5.5V and F = 0 to 40 MHz (both internal and external code execution)

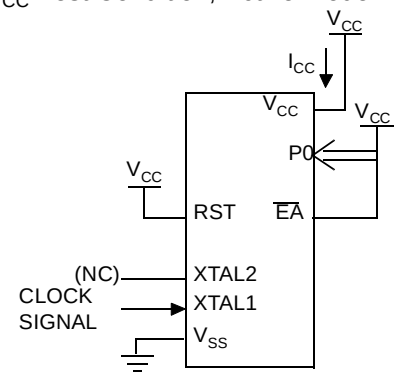
V_{CC} =4.5V to 5.5V and F = 0 to 60 MHz (internal code execution only)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except RST, XTAL1	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}[9]	Input High Voltage RST, XTAL1	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3, 4 [6]					VCC = 4.5V to 5.5V
				0.3	V	I_{OL} = 100 µA[4]
				0.45	V	I_{OL} = 1.6 mA[4]
				1.0	V	I_{OL} = 3.5 mA[4]
				0.45	V	VCC = 2.7V to 5.5V I_{OL} = 0.8 mA[4]
V_{OL1}	Output Low Voltage, port 0, ALE, $\overline{PSEN}$ [6]					VCC = 4.5V to 5.5V
				0.3	V	I_{OL} = 200 µA[4]
				0.45	V	I_{OL} = 3.2 mA[4]
				1.0	V	I_{OL} = 7.0 mA[4]
				0.45	V	VCC = 2.7V to 5.5V I_{OL} = 1.6 mA[4]
V_{OH}	Output High Voltage, ports 1, 2, 3, 4					V_{CC} = 5V ± 10%
		V_{CC} - 0.3			V	I_{OH} = -10 µA
		V_{CC} - 0.7			V	I_{OH} = -30 µA
		V_{CC} - 1.5			V	I_{OH} = -60 µA
		0.9 V_{CC}			V	VCC = 2.7V to 5.5V I_{OH} = -10 µA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

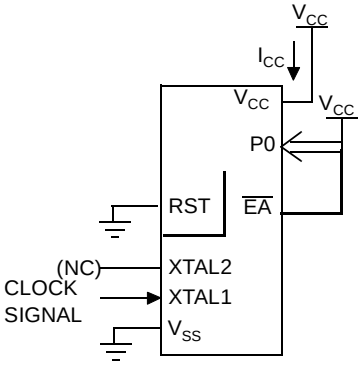
7. For other values, please contact your sales office.
8. Icc Flash Write operation current while an on-chip flash page write is on going.

Figure 46. I_{CC} Test Condition, Active Mode



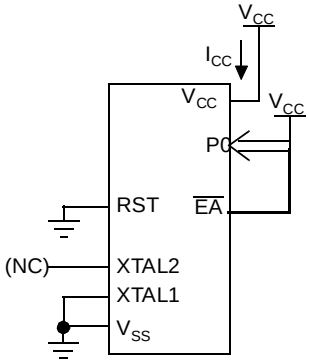
All other pins are disconnected.

Figure 47. I_{CC} Test Condition, Idle Mode



All other pins are disconnected.

Figure 48. I_{CC} Test Condition, Power-down Mode



All other pins are disconnected.

Figure 49. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes

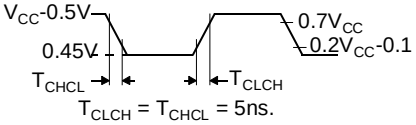


Table 79. AC Parameters for a Fix Clock

Symbol	-M		-L		Units
	Min	Max	Min	Max	
T_{RLRH}	125		125		ns
T_{WLWH}	125		125		ns
T_{RLDV}		95		95	ns
T_{RHDX}	0		0		ns
T_{RHDZ}		25		25	ns
T_{LLDV}		155		155	ns
T_{AVDV}		160		160	ns
T_{LLWL}	45	105	45	105	ns
T_{AVWL}	70		70		ns
T_{QVWX}	5		5		ns
T_{QVWH}	155		155		ns
T_{WHQX}	10		10		ns
T_{RLAZ}	0		0		ns
T_{WHLH}	5	45	5	45	ns

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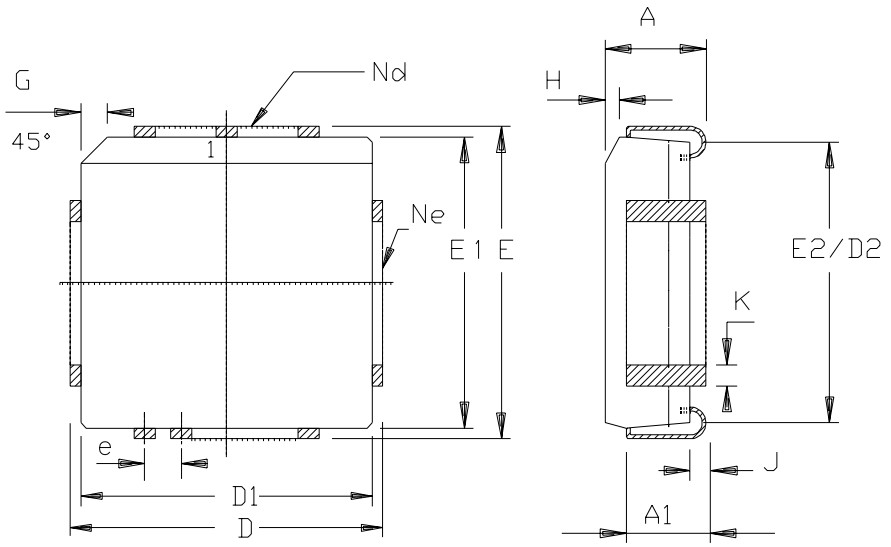

	MM		INCH	
A	4.20	4.57	.165	.180
A1	2.29	3.04	.090	.120
D	17.40	17.65	.685	.695
D1	16.44	16.66	.647	.656
D2	14.99	16.00	.590	.630
E	17.40	17.65	.685	.695
E1	16.44	16.66	.647	.656
E2	14.99	16.00	.590	.630
e	1.27	BSC	.050	BSC
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	–	.020	–
K	0.33	0.53	.013	.021
Nd	11		11	
Ne	11		11	
PKG STD	00			

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