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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	I²C, SIO, UART/USART, USB
Peripherals	POR, WDT
Number of I/O	45
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f337pmc-ge1

FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13735-6E

16-bit Microcontroller

CMOS

F²MC-16LX MB90335 Series

MB90337/F337/V330A

■ DESCRIPTION

The MB90335 series are 16-bit microcontrollers designed for applications, such as personal computer peripheral devices, that require USB communications. The USB feature supports not only 12-Mbps Function operation but also HOST operation. It is equipped with functions that are suitable for personal computer peripheral devices such as displays and audio devices, and control of mobile devices that support USB communications. While inheriting the AT architecture of the F²MC* family, the instruction set supports the C language and extended addressing modes and contains enhanced signed multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions. In addition, long word processing is now available by introducing a 32-bit accumulator.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- **Clock**
  - Built-in oscillation circuit and PLL clock frequency multiplication circuit
  - Oscillation clock
  - The main clock is the oscillation clock divided into 2 (for oscillation 6 MHz : 3 MHz)
  - Clock for USB is 48 MHz
  - Machine clock frequency of 6 MHz, 12 MHz or 24 MHz selectable
  - Minimum execution time of instruction : 41.7 ns (6 MHz oscillation clock, 4-time multiplied : machine clock 24 MHz and at operating V_{CC} = 3.3 V)
- **The maximum memory space: 16 Mbytes**
- **24-bit addressing**
- **Bank addressing**

(Continued)

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

2010.5

■ PRODUCT LINEUP

Part number	MB90V330A	MB90F337	MB90337
Type	For evaluation	Built-in Flash Memory	Built-in MASK ROM
ROM capacity	No	64 Kbytes	
RAM capacity	28 Kbytes	4 Kbytes	
Emulator-specific power supply *	Used bit	—	
CPU functions	Number of basic instructions : 351 instructions Minimum instruction execution time : 41.7 ns / at oscillation of 6 MHz (When 4 times are used : Machine clock of 24 MHz) Addressing type : 23 types Program Patch Function : For 2 address pointers Maximum memory space : 16 Mbytes		
Ports	I/O Ports(CMOS) Max 45 ports		
UART	Equipped with full-duplex double buffer Clock synchronous or asynchronous operation selectable. It can also be used for I/O serial. Built-in special baud-rate generator Built-in 2 channels		
16-bit reload timer	16-bit reload timer operation Built-in 1 channel		
Multi-functional timer	8/16-bit PPG timer (8-bit mode × 4 channels, 16-bit mode × 2 channels) 16-bit PWC timer × 1 channel		
DTP/External interrupt	8 channels Interrupt factor : “L”→“H” edge /“H”→“L” edge /“L” level /“H” level selectable		
I^2C	1 channel		
Extended I/O serial interface	1 channel		
USB	1 channel USB function (supports USB Full Speed) USB HOST function		
Withstand voltage of 5 V	8 ports (Excluding UTEST and I/O for I^2C)		
Low Power Consumption Mode	Sleep mode/Timebase timer mode/Stop mode/CPU intermittent mode		
Process	CMOS		
Operating voltage V_{CC}	3.3 V ± 0.3 V (at maximum machine clock 24 MHz)		

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used. Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply Switching) about details.

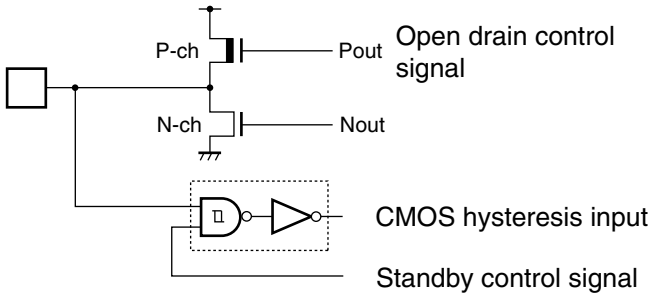
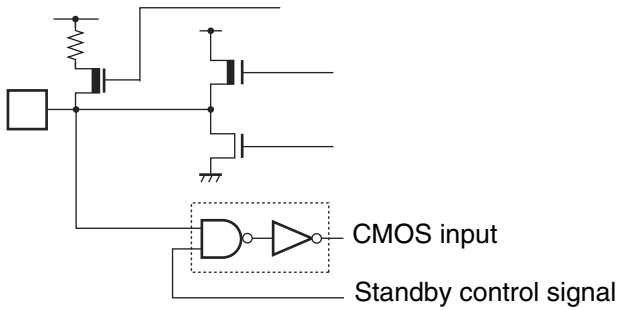
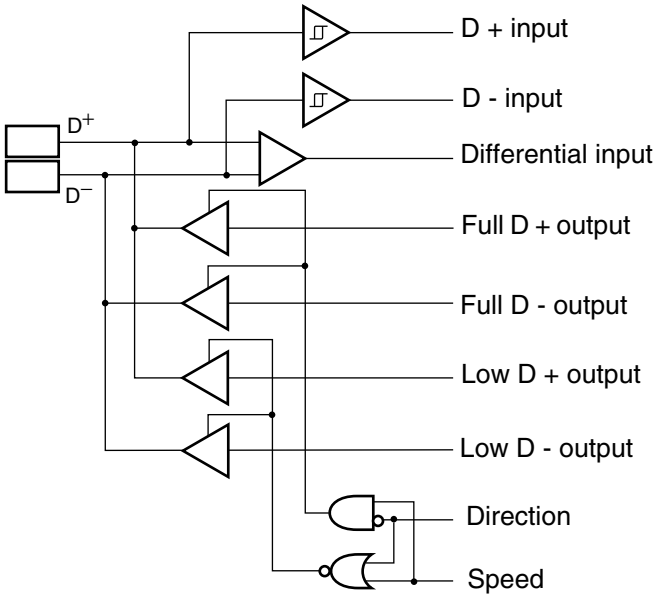
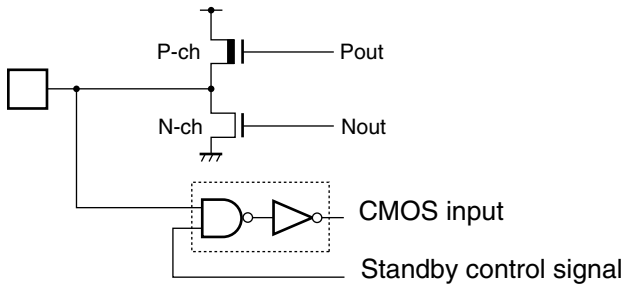
■ PACKAGES AND PRODUCT MODELS

Package	MB90337	MB90F337	MB90V330A
FPT-64P-M23 (LQFP)	○	○	×
PGA-299C-A01 (PGA)	×	×	○

○ : Yes × : No

Note : See “■ PACKAGE DIMENSIONS” for details.

(Continued)

Type	Circuit	Remarks
H		• CMOS output • CMOS hysteresis input (With input interception function at standby) With open drain control signal
I		• CMOS output • CMOS input (With input interception function at standby) • Programmable input pull-up resistor
J		USB I/O pin
K		• CMOS output • CMOS input (With input interception function at standby)

7. Stabilization of supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the V_{CC} supply voltage operating range. For stabilization reference, the supply voltage should be stabilized so that V_{CC} ripple variations (peak-to-peak value) at commercial frequencies (50 MHz to 60 MHz) fall below 10% of the standard V_{CC} supply voltage and the transient regulation does not exceed 0.1 V/ms at temporary changes such as power supply switching.

8. Writing to flash memory

For serial writing to flash memory, always make sure that the operating voltage V_{CC} is between 3.13 V and 3.6 V.

For normal writing to flash memory, always make sure that the operating voltage V_{CC} is between 3.0 V and 3.6 V.

9. Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.
Consider receiving of wrong data when designing the system. For example, apply a checksum to detect an error. If an error is detected, retransmit the data.

■ I/O MAP

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
000000H	PDR0	Port 0 Data Register	R/W	Port 0	XXXXXXXXB
000001H	PDR1	Port 1 Data Register	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 Data Register	R/W	Port 2	XXXXXXXXB
000003H	Prohibited				
000004H	PDR4	Port 4 Data Register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 Data Register	R/W	Port 5	- - - XXXXXB
000006H	PDR6	Port 6 Data Register	R/W	Port 6	XXXXXXXXB
000007H to 00000FH	Prohibited				
000010H	DDR0	Port 0 Direction Register	R/W	Port 0	0 0 0 0 0 0 0 0B
000011H	DDR1	Port 1 Direction Register	R/W	Port 1	0 0 0 0 0 0 0 0B
000012H	DDR2	Port 2 Direction Register	R/W	Port 2	0 0 0 0 0 0 0 0B
000013H	Prohibited				
000014H	DDR4	Port 4 Direction Register	R/W	Port 4	0 0 0 0 0 0 0 0B
000015H	DDR5	Port 5 Direction Register	R/W	Port 5	- - - 0 0 0 0 0B
000016H	DDR6	Port 6 Direction Register	R/W	Port 6	0 0 0 0 0 0 0 0B
000017H to 00001AH	Prohibited				
00001BH	ODR4	Port 4 Output Pin Register	R/W	Port 4 (Open-drain control)	0 0 0 0 0 0 0 0B
00001CH	RDR0	Port 0 Pull-up Resistance Register	R/W	Port 0 (PULL-UP)	0 0 0 0 0 0 0 0B
00001DH	RDR1	Port 1 Pull-up Resistance Register	R/W	Port 1 (PULL-UP)	0 0 0 0 0 0 0 0B
00001EH	Prohibited				
00001FH					
000020H	SMR0	Serial Mode Register 0	R/W	UART0	0 0 1 0 0 0 0 0B
000021H	SCR0	Serial Control Register 0	R/W		0 0 0 0 0 1 0 0B
000022H	SIDR0	Serial Input Data Register 0	R		XXXXXXXXB
	SODR0	Serial Output Data Register 0	W		
000023H	SSR0	Serial Status Register 0	R/W		0 0 0 0 1 0 0 0B
000024H	UTRLR0	UART Prescaler Reload Register 0	R/W	Communication Prescaler (UART0)	0 0 0 0 0 0 0 0B
000025H	UTCR0	UART Prescaler Control Register 0	R/W		0 0 0 0 - 0 0 0B
000026H	SMR1	Serial Mode Register 1	R/W	UART1	0 0 1 0 0 0 0 0B
000027H	SCR1	Serial Control Register 1	R/W		0 0 0 0 0 1 0 0B
000028H	SIDR1	Serial Input Data Register 1	R		XXXXXXXXB
	SODR1	Serial Output Data Register 1	W		
000029H	SSR1	Serial Status Register 1	R/W		0 0 0 0 1 0 0 0B

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
0000B0H	ICR00	Interrupt Control Register 00	R/W	Interrupt Controller	0 0 0 0 0 1 1 1B
0000B1H	ICR01	Interrupt Control Register 01	R/W		0 0 0 0 0 1 1 1B
0000B2H	ICR02	Interrupt Control Register 02	R/W		0 0 0 0 0 1 1 1B
0000B3H	ICR03	Interrupt Control Register 03	R/W		0 0 0 0 0 1 1 1B
0000B4H	ICR04	Interrupt Control Register 04	R/W		0 0 0 0 0 1 1 1B
0000B5H	ICR05	Interrupt Control Register 05	R/W		0 0 0 0 0 1 1 1B
0000B6H	ICR06	Interrupt Control Register 06	R/W		0 0 0 0 0 1 1 1B
0000B7H	ICR07	Interrupt Control Register 07	R/W		0 0 0 0 0 1 1 1B
0000B8H	ICR08	Interrupt Control Register 08	R/W		0 0 0 0 0 1 1 1B
0000B9H	ICR09	Interrupt Control Register 09	R/W		0 0 0 0 0 1 1 1B
0000BAH	ICR10	Interrupt Control Register 10	R/W		0 0 0 0 0 1 1 1B
0000BBH	ICR11	Interrupt Control Register 11	R/W		0 0 0 0 0 1 1 1B
0000BCH	ICR12	Interrupt Control Register 12	R/W		0 0 0 0 0 1 1 1B
0000BDH	ICR13	Interrupt Control Register 13	R/W		0 0 0 0 0 1 1 1B
0000BEH	ICR14	Interrupt Control Register 14	R/W		0 0 0 0 0 1 1 1B
0000BFH	ICR15	Interrupt Control Register 15	R/W		0 0 0 0 0 1 1 1B
0000C0H	HCNT0	Host Control Register 0	R/W	USB HOST	0 0 0 0 0 0 0 0B
0000C1H	HCNT1	Host Control Register 1	R/W		0 0 0 0 0 0 0 1B
0000C2H	HIRQ	Host Interruption Register	R/W		0 0 0 0 0 0 0 0B
0000C3H	HERR	Host Error Status Register	R/W		0 0 0 0 0 0 1 1B
0000C4H	HSTATE	Host State Status Register	R/W		XX 0 1 0 0 1 0B
0000C5H	HFCOMP	SOF Interrupt FRAME Compare Register	R/W		0 0 0 0 0 0 0 0B
0000C6H	HRTIMER	Retry Timer Setting Register	R/W		0 0 0 0 0 0 0 0B
0000C7H			R/W		0 0 0 0 0 0 0 0B
0000C8H			R/W		XXXXXX 0 0B
0000C9H	HADR	Host Address Register	R/W		X 0 0 0 0 0 0 0B
0000CAH	HEOF	EOF Setting Register	R/W		0 0 0 0 0 0 0 0B
0000CBH			R/W		XX 0 0 0 0 0 0B
0000CCH	HFRAME	FRAME Setting Register	R/W		0 0 0 0 0 0 0 0B
0000CDH			R/W		XXXXX 0 0 0B
0000CEH	HTOKEN	Host Token End Point Register	R/W		0 0 0 0 0 0 0 0B
0000CFH	Prohibited				
0000D0H	UDCC	UDC Control Register	R/W	USB Function	1 0 1 0 0 0 0 0B
0000D1H			R/W		0 0 0 0 0 0 0 0B

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
0000D2H	EP0C	EP0 Control Register	R/W	USB Function	0 1 0 0 0 0 0 0B
0000D3H			R/W		XXXX 0 0 0 0B
0000D4H	EP1C	EP1 Control Register	R/W		0 0 0 0 0 0 0 0B
0000D5H			R/W		0 1 1 0 0 0 0 1B
0000D6H	EP2C	EP2 Control Register	R/W		0 1 0 0 0 0 0 0B
0000D7H			R/W		0 1 1 0 0 0 0 0B
0000D8H	EP3C	EP3 Control Register	R/W		0 1 0 0 0 0 0 0B
0000D9H			R/W		0 1 1 0 0 0 0 0B
0000DAH	EP4C	EP4 Control Register	R/W		0 1 0 0 0 0 0 0B
0000DBH			R/W		0 1 1 0 0 0 0 0B
0000DCH	EP5C	EP5 Control Register	R/W		0 1 0 0 0 0 0 0B
0000DDH			R/W		0 1 1 0 0 0 0 0B
0000DEH	TMSP	Time Stamp Register	R		0 0 0 0 0 0 0 0B
0000DFH			R		XXXXX0 0 0B
0000E0H	UDCS	UDC Status Register	R/W		XX0 0 0 0 0 0B
0000E1H	UDCIE	UDC Interrupt Enable Register	R/W		0 0 0 0 0 0 0 0B
0000E2H	EP0IS	EP0I Status Register	R/W		XXXXXXXXB
0000E3H			R/W		1 0 XXX 1 XXB
0000E4H	EP0OS	EP0O Status Register	R/W, R		0 XXXXXXXB
0000E5H			R/W		1 0 0 XX 0 0 0B
0000E6H	EP1S	EP1 Status Register	R		XXXXXXXXB
0000E7H			R/W		1 0 0 0 0 0 0 XB
0000E8H	EP2S	EP2 Status Register	R		XXXXXXXXB
0000E9H			R/W		1 0 0 0 0 0 0 0B
0000EAH	EP3S	EP3 Status Register	R		XXXXXXXXB
0000EBH			R/W		1 0 0 0 0 0 0 0B
0000ECH	EP4S	EP4 Status Register	R		XXXXXXXXB
0000EDH			R/W		1 0 0 0 0 0 0 0B
0000EEH	EP5S	EP5 Status Register	R		XXXXXXXXB
0000EFH			R/W		1 0 0 0 0 0 0 0B
0000F0H	EP0DT	EP0 Data Register	R/W		XXXXXXXXB
0000F1H			R/W		XXXXXXXXB
0000F2H	EP1DT	EP1 Data Register	R/W		XXXXXXXXB
0000F3H			R/W		XXXXXXXXB
0000F4H	EP2DT	EP2 Data Register	R/W		XXXXXXXXB
0000F5H			R/W		XXXXXXXXB
0000F6H	EP3DT	EP3 Data Register	R/W		XXXXXXXXB
0000F7H			R/W		XXXXXXXXB
0000F8H	EP4DT	EP4 Data Register	R/W		XXXXXXXXB
0000F9H			R/W		XXXXXXXXB

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource name	Initial Value
0000FA$_H$	EP5DT	EP5 Data Register	R/W	USB Function	XXXXXXXX$_B$
0000FB$_H$			R/W		XXXXXXXX$_B$
0000FC$_H$ to 0000FF$_H$	Prohibited				
000100$_H$ to 001100$_H$	RAM Area				
001FF0$_H$	PADR0	Program Address Detection Register ch.0 Lower	R/W	Address Match Detection	XXXXXXXX$_B$
001FF1$_H$		Program Address Detection Register ch.0 Middle	R/W		XXXXXXXX$_B$
001FF2$_H$		Program Address Detection Register ch.0 Upper	R/W		XXXXXXXX$_B$
001FF3$_H$	PADR1	Program Address Detection Register ch.1 Lower	R/W		XXXXXXXX$_B$
001FF4$_H$		Program Address Detection Register ch.1 Middle	R/W		XXXXXXXX$_B$
001FF5$_H$		Program Address Detection Register ch.1 Upper	R/W		XXXXXXXX$_B$
007900$_H$	PRLL0	PPG Reload Register Lower ch.0	R/W	PPG ch.0	XXXXXXXX$_B$
007901$_H$	PRLH0	PPG Reload Register Upper ch.0	R/W		XXXXXXXX$_B$
007902$_H$	PRLL1	PPG Reload Register Lower ch.1	R/W	PPG ch.1	XXXXXXXX$_B$
007903$_H$	PRLH1	PPG Reload Register Upper ch.1	R/W		XXXXXXXX$_B$
007904$_H$	PRLL2	PPG Reload Register Lower ch.2	R/W	PPG ch.2	XXXXXXXX$_B$
007905$_H$	PRLH2	PPG Reload Register Upper ch.2	R/W		XXXXXXXX$_B$
007906$_H$	PRLL3	PPG Reload Register Lower ch.3	R/W	PPG ch.3	XXXXXXXX$_B$
007907$_H$	PRLH3	PPG Reload Register Upper ch.3	R/W		XXXXXXXX$_B$
007908$_H$ to 00790B$_H$	Prohibited				
00790C$_H$	FWR0	Flash Memory Program Control Register 0	R/W	Flash	0 0 0 0 0 0 0 0$_B$
00790D$_H$	FWR1	Flash Memory Program Control Register 1	R/W	Flash	0 0 0 0 0 0 0 0$_B$
00790E$_H$	SSR0	Sector Conversion Setting Register	R/W	Flash	0 0 XXXXX0$_B$
00790F$_H$ to 00791F$_H$	Prohibited				

(Continued)

■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS support	μDMAC	Interrupt vector			Interrupt control register		Priority
			Number*1		Address	ICR	Address	
Reset	×	×	#08	08H	FFFFDCH	—	—	High
INT 9 instruction	×	×	#09	09H	FFFFD8H	—	—	
Exceptional treatment	×	×	#10	0AH	FFFFD4H	—	—	
USB Function1	×	0, 1	#11	0BH	FFFFD0H	ICR00	0000B0H	
USB Function2	×	2 to 6*2	#12	0CH	FFFFCCH			
USB Function3	×	×	#13	0DH	FFFFC8H	ICR01	0000B1H	
USB Function4	×	×	#14	0EH	FFFFC4H			
USB HOST1	×	×	#15	0FH	FFFFC0H	ICR02	0000B2H	
USB HOST2	×	×	#16	10H	FFFFBCH			
I²C ch.0	×	×	#17	11H	FFFFB8H	ICR03	0000B3H	
DTP/External interrupt ch.0/ch.1	○	×	#18	12H	FFFFB4H			
No	—	—	#19	13H	FFFFB0H	ICR04	0000B4H	
DTP/External interrupt ch.2/ch.3	○	×	#20	14H	FFFFACH			
No	—	—	#21	15H	FFFFA8H	ICR05	0000B5H	
DTP/External interrupt ch.4/ch.5	○	×	#22	16H	FFFFA4H			
PWC/Reload timer ch.0	△	14	#23	17H	FFFFA0H	ICR06	0000B6H	
DTP/External interrupt ch.6/ch.7	△	×	#24	18H	FFFF9CH			
No	—	—	#25	19H	FFFF98H	ICR07	0000B7H	
No	—	—	#26	1AH	FFFF94H			
No	—	—	#27	1BH	FFFF90H	ICR08	0000B8H	
No	—	—	#28	1CH	FFFF8CH			
No	—	—	#29	1DH	FFFF88H	ICR09	0000B9H	
PPG ch.0/ch.1	×	×	#30	1EH	FFFF84H			
No	—	—	#31	1FH	FFFF80H	ICR10	0000BAH	
PPG ch.2/ch.3	×	×	#32	20H	FFFF7CH			
No	—	—	#33	21H	FFFF78H	ICR11	0000BBH	
No	—	—	#34	22H	FFFF74H			
No	—	—	#35	23H	FFFF70H	ICR12	0000BCH	
No	—	—	#36	24H	FFFF6CH			
UART (Send completed) ch.0/ch.1	○	13	#37	25H	FFFF68H	ICR13	0000BDH	
Extended serial I/O	×	9	#38	26H	FFFF64H			
UART(Reception completed) ch.0/ch.1	◎	12	#39	27H	FFFF60H	ICR14	0000BEH	
Time-base timer	×	×	#40	28H	FFFF5CH			
Flash memory status	×	×	#41	29H	FFFF58H	ICR15	0000BFH	
Delay interrupt output module	×	×	#42	2AH	FFFF54H			Low

(Continued)

■ USB

1. USB Function

The USB function is an interface supporting the USB (Universal Serial Bus) communications protocol.

Features of USB function

- Supports USB Full Speed
- Supports full speed (12 Mbps).
- The device status is auto-answer.
- Bit stripping, bit stuffing, and automatic generation and check of CRC5 and CRC16.
- Toggle check by data synchronization bit.
- Automatic response to all standard commands except Get/SetDescriptor and SynchFrame commands (these three commands can be processed the same way as the class vendor commands).
- The class vendor commands can be received as data and responded via firmware.
- Supports up to a maximum of six EndPoints (EndPoint0 is fixed to control transfer).
- Two built-in transfer data buffers for each end point (one IN buffer and one OUT buffer for end point 0).
- Supports automatic transfer mode for transfer data via DMA (except buffers for EndPoint0).

2. USB HOST

USB HOST provides minimal host operations required and is a function that enables data to be transferred between devices without PC intervention.

• Features of USB HOST
- Automatic detection of Low Speed/Full Speed transfer
- Low Speed/Full Speed transfer support
- Automatic detection of connection and cutting device
- Reset sending function support to USB-bus
- Support of IN/OUT/SETUP/SOF token
- In-token handshake packet automatic transmission (excluding STALL)
- Handshake packet automatic detection at out-token
- Supports a maximum packet length of 256 bytes
- Error (CRC error/toggle error/time-out) various supports
- Wake-Up function support

• Restrictions on USB HOST

		USB HOST
HUB support		○ *
Transfer	Bulk transfer	○
	Control transfer	○
	Interrupt transfer	○
	Isochronous transfer	×
Transfer speed	Low Speed	○
	Full Speed	○
PRE packet support		×
SOF packet support		○
Error	CRC error	○
	Toggle error	○
	Time-out	○
	Maximum packet < receive data	○
Detection of connection and cutting of device		○
Transfer speed detection		○

○ : Supported
× : Not supported

* : Only supports full speed, and supports hubs up to one level.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
		V_{SS} – 0.3	V_{SS} + 6.0	V	N-ch open-drain (Withstand voltage I/O of 5 V)*3
		– 0.5	V_{SS} + 4.5	V	USB I/O
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
		– 0.5	V_{SS} + 4.5	V	USB I/O
Maximum clamp current	I_{CLAMP}	– 2.0	+2.0	mA	*4
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	—	20	mA	*4
"L" level maximum output current	I_{OL1}	—	10	mA	Other than USB I/O*5
	I_{OL2}	—	43	mA	USB I/O*5
"L" level average output current	I_{OLAV1}	—	4	mA	*6
	I_{OLAV2}	—	15/4.5	mA	USB-IO (Full speed/Low speed) *6
"L" level maximum total output current	ΣI_{OL}	—	100	mA	
"L" level average total output current	ΣI_{OLAV}	—	50	mA	*7
"H" level maximum output current	I_{OH1}	—	– 10	mA	Other than USB I/O*5
	I_{OH2}	—	– 43	mA	USB I/O*5
"H" level average output current	I_{OHAV1}	—	– 4	mA	*6
	I_{OHAV2}	—	–15/–4.5	mA	USB-IO (Full speed/Low speed) *6
"H" level maximum total output current	ΣI_{OH}	—	– 100	mA	
"H" level average total output current	ΣI_{OHAV}	—	– 50	mA	*7
Power consumption	Pd	—	270	mW	
Operating temperature	T_A	– 40	+ 85	°C	
Storage temperature	Tstg	– 55	+ 150	°C	
		– 55	+ 125	°C	USB I/O

*1 : The parameter is based on V_{SS} = 0.0 V.

*2 : V_I and V_O must not exceed V_{CC} + 0.3 V. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*3 : Applicable to pins : P60 to P67, UTEST

(Continued)

(Continued)

(V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input capacitance	C_{IN}	Other than Vcc and Vss	—	—	5	15	pF	
Pull-up resistor	R_{up}	$\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistor	R_{down}	MD2	V_{CC} = 3.0 V At T_A = +25 °C	25	50	100	kΩ	MB90337
USB I/O output impedance	Z_{USB}	DVP, DVM HVP, HVM	—	3	—	14	Ω	

Note : P60 to P67 are N-ch open-drain pins usually used as CMOS.

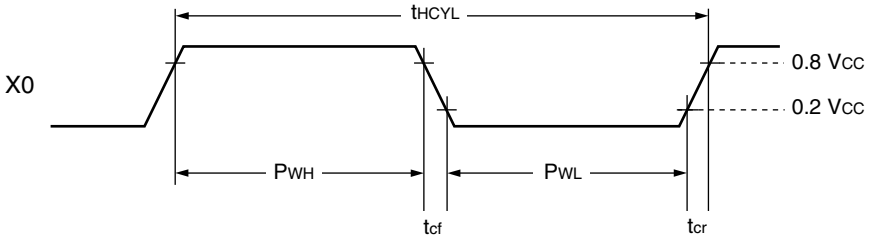
4. AC Characteristics

(1) Clock input timing

(V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CH}	X0, X1	—	6	—	MHz	When oscillator is used
			6	—	24	MHz	External clock input
Clock cycle time	t_{HCYL}	X0, X1	—	166.7	—	ns	When oscillator is used
			166.7	—	41.7	ns	External clock input
Input clock pulse width	P_{WH} P_{WL}	X0	10	—	—	ns	A reference duty ratio is 30% to 70%.
Input clock rise time and fall time	tcr tcf	X0	—	—	5	ns	At external clock
Internal operating clock frequency	f_{CP}	—	3	—	24	MHz	When main clock is used
Internal operating clock cycle time	t_{CP}	—	42	—	333	ns	When main clock is used

• Clock Timing



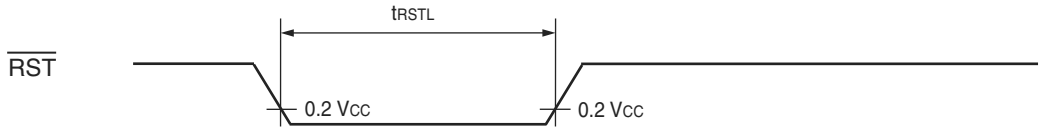
(2) Reset

(V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

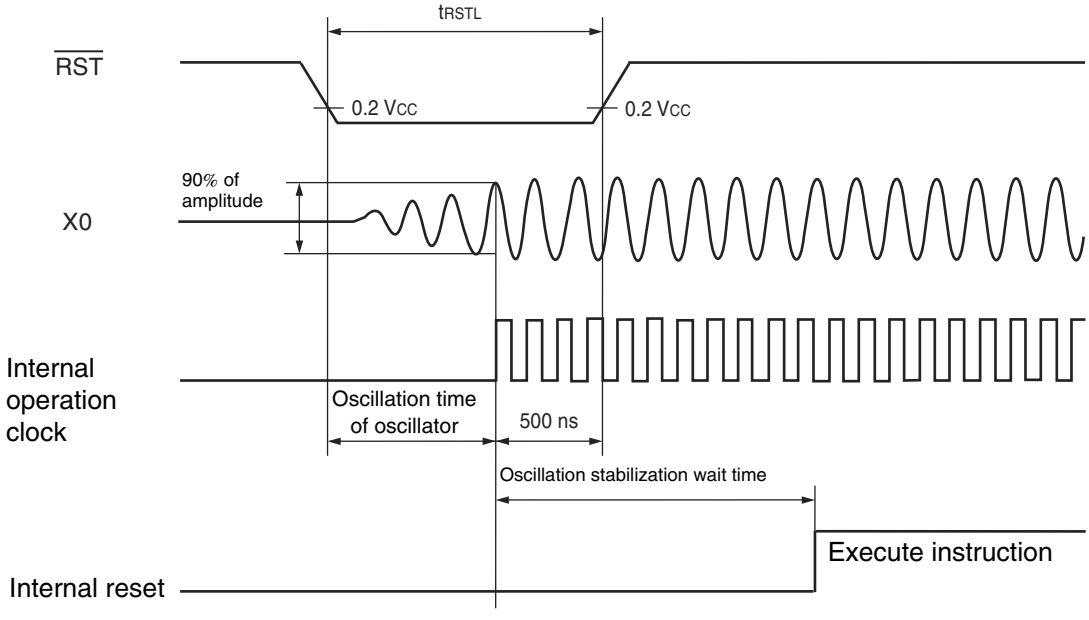
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	500	—	ns	At normal operating, At time base timer mode, At main sleep mode, At PLL sleep mode
				Oscillation time of oscillator* + 500 ns	—	µs	At stop mode

* : Oscillation time of oscillator is the time that the amplitude reaches 90 %. It takes several milliseconds to several dozens of milliseconds on a crystal oscillator, several hundreds of microseconds to several milliseconds on a ceramic oscillator, and 0 milliseconds on an external clock.

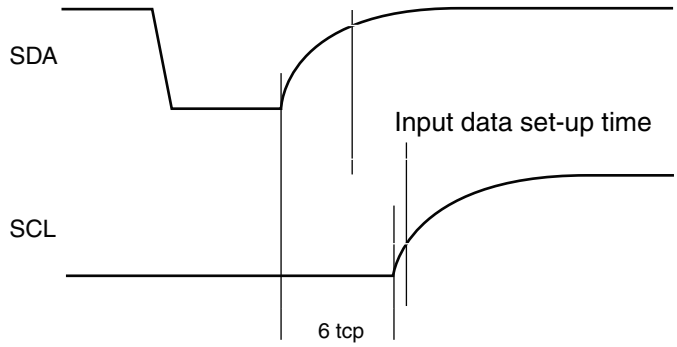
• During normal operation, time-base timer mode, main sleep mode and PLL sleep mode



• During stop mode

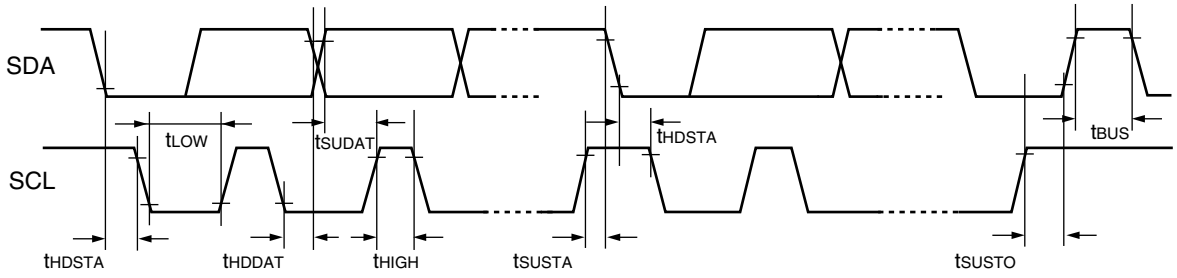


•Note of SDA, SCL set-up time



Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

•Timing definition



■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F337PMC MB90337PMC	64-pin plastic LQFP (FPT-64P-M23)	
MB90V330ACR	299-pin ceramic PGA (PGA-299C-A01)	For evaluation

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
35	■ ELECTRICAL CHARACTERISTICS 4.AC Characteristics (3) Power-on reset	Corrected as follows; Voltage of RAM data hold: 3.0 V → 1.8 V

The vertical lines marked in the left side of the page show the changes.

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