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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|---|
| Product Status | Obsolete |
| Core Processor | ARM7® |
| Core Size | 32-Bit Single-Core |
| Speed | 66MHz |
| Connectivity | CANbus, EBI/EMI, HDLC, I²C, SmartCard, SPI, UART/USART, USB |
| Peripherals | PWM, WDT |
| Number of I/O | 48 |
| Program Memory Size | 128KB (128K x 8 + 16K) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 4x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/str710fz1t6 |

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1 Introduction

This datasheet provides the STR71x pinout, ordering information, mechanical and electrical device characteristics.

For complete information on the STR71x microcontroller memory, registers and peripherals. please refer to the STR71x reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash programming reference manual.

For information on the ARM7TDMI core please refer to the ARM7TDMI technical reference manual.

Table 2. Device overview

| Features | STR710 FZ1 | STR710 FZ2 | STR710 RZ | STR711 FR0 | STR711 FR1 | STR711 FR2 | STR712 FR0 | STR712 FR1 | STR712 FR2 | STR715 FRx | | | | | | |
|-----------------------|--|---------------|------------------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|--|--|--|--|--|--|
| Flash - Kbytes | 128+16 | 256+16 | 0 | 64+16 | 128+16 | 256+16 | 64+16 | 128+16 | 256+16 | 64+16 | | | | | | |
| RAM - Kbytes | 32 | 64 | 64 | 16 | 32 | 64 | 16 | 32 | 64 | 16 | | | | | | |
| Peripheral Functions | CAN, EMI, USB, 48 I/Os | | | USB, 30 I/Os | | | CAN, 32 I/Os | | | 32 I/Os | | | | | | |
| Operating Voltage | 3.0 to 3.6 V | | | | | | | | | | | | | | | |
| Operating Temperature | -40 to +85°C or 0 to 70° C | | | | | | | | | | | | | | | |
| Packages | T=LQFP144 20 x 20 H=LFBGA144 10 x10 | | T=LQFP64 10 x10 | | | | | | | | | | | | | |



3.2 Related documentation

Available from www.arm.com:

ARM7TDMI Technical reference manual

Available from <http://www.st.com>:

STR71x Reference manual

STR7 Flash programming manual

AN1774 - STR71x Software development getting started

AN1775 - STR71x Hardware development getting started

AN1776 - STR71x Enhanced interrupt controller

AN1777 - STR71x memory mapping

AN1780 - Real time clock with STR71x

AN1781 - Four 7 segment display drive using the STR71x

The above is a selected list only, a full list STR71x application notes can be viewed at

<http://www.st.com>.

3.3 Pin description for 144-pin packages

Figure 2. STR710 LQFP pinout

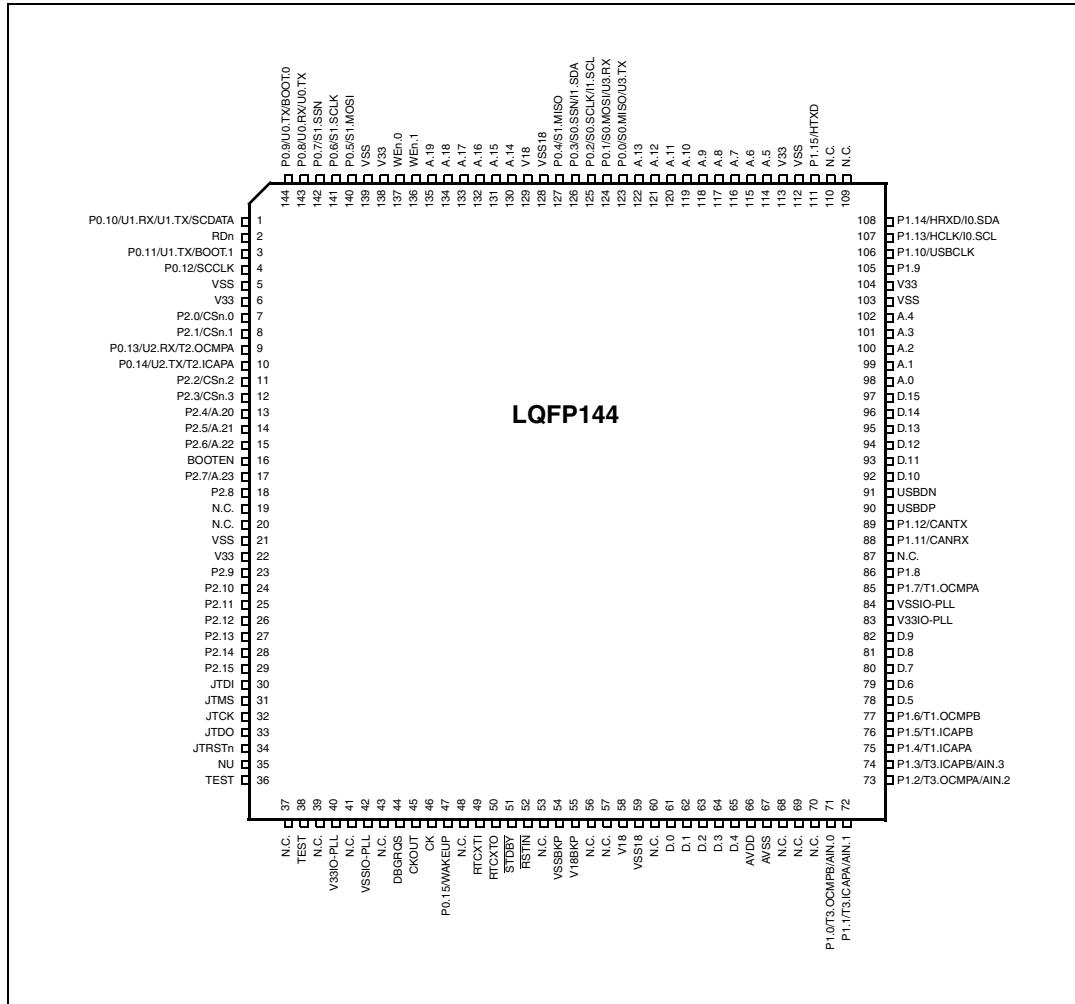


Figure 7. Mapping of Flash memory versions

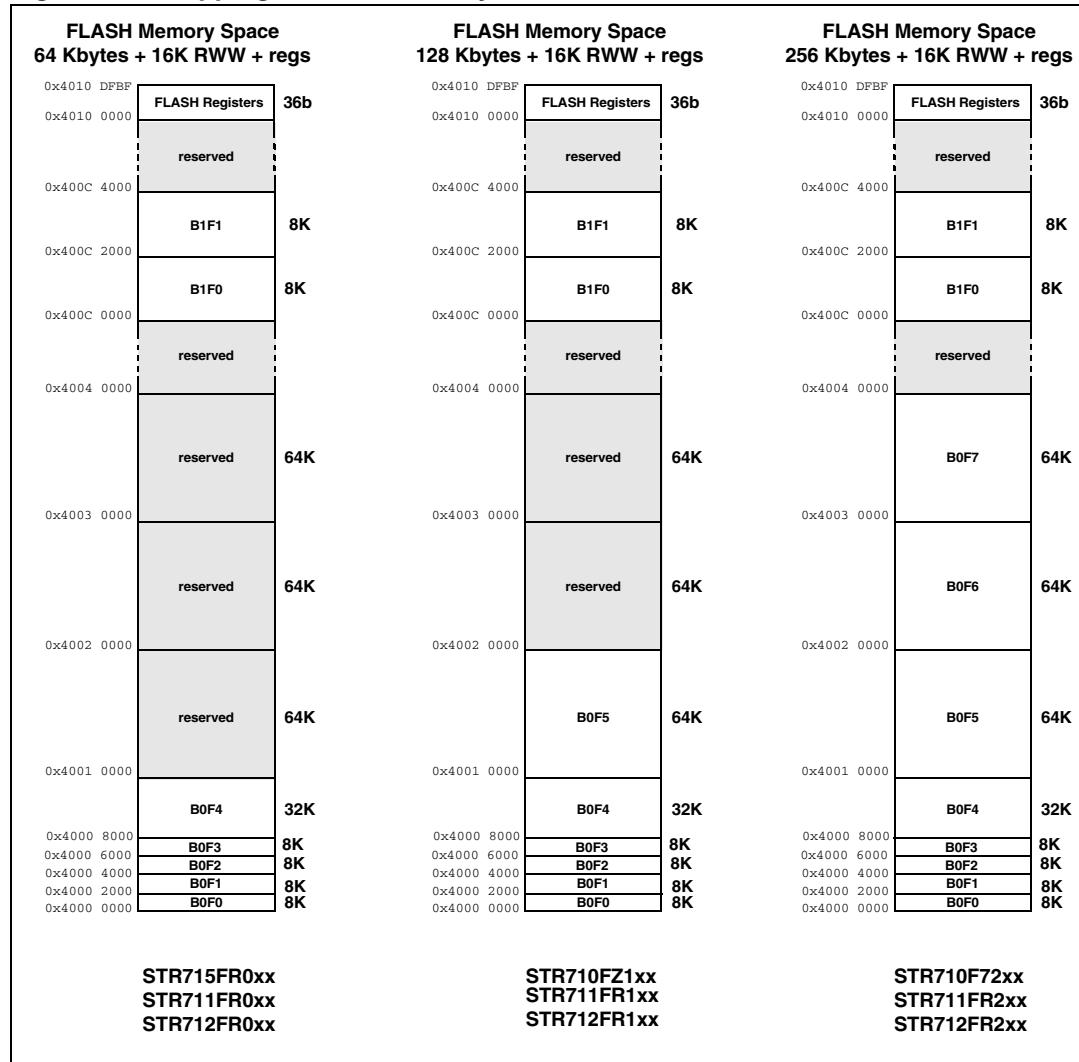


Table 7. RAM memory mapping

| Part number | RAM size | Start address | End address |
|--|-----------|---------------|-------------|
| STR715FR0xx STR711FR0xx STR712FR0xx | 16 Kbytes | 0x2000 0000 | 0x2000 3FFF |
| STR710FZ1xx STR711FR1xx STR712FR1xx | 32 Kbytes | 0x2000 0000 | 0x2000 7FFF |
| STR710FR2xx STR710Rxx STR711FR2xx STR712FR2xx | 64 Kbytes | 0x2000 0000 | 0x2000 FFFF |

Table 9. Current characteristics

| Symbol | Ratings | Max. | Unit |
|-------------------------------------|---|----------|------|
| I_{V33} | Total current into $V_{33}/V_{33\text{IO-PLL}}$ power lines (source) ²⁾ | 150 | mA |
| I_{VSS} | Total current out of $V_{SS}/V_{SS\text{IO-PLL}}$ ground lines (sink) ²⁾ | 150 | |
| I_{IO} | Output current sunk by any I/O and control pin | 25 | |
| | Output current source by any I/Os and control pin | - 25 | |
| $I_{INJ(PIN)}$ ^{1) 3)} | Injected current on \overline{RSTIN} pin | ± 5 | |
| | Injected current on CK pin | ± 5 | |
| | Injected current on any other pin ⁴⁾ | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ ¹⁾ | Total injected current (sum of all I/O and control pins) ⁴⁾ | ± 25 | |

The $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{33}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected. Data based on $T_A = 25^\circ\text{C}$.

All 3.3V power (V_{33} , AV_{DD} , $V_{33\text{IO-PLL}}$) and ground (V_{SS} , AV_{SS} , $V_{SS\text{IO-PLL}}$) pins must always be connected to the external 3.3V supply.

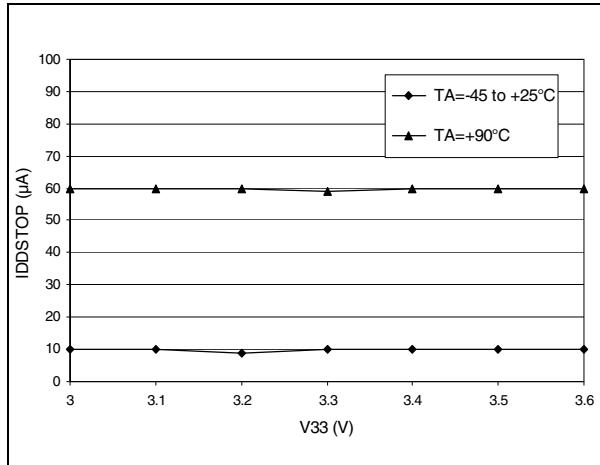
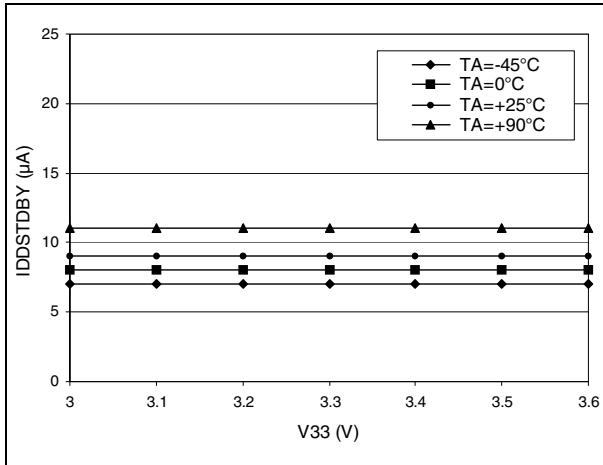
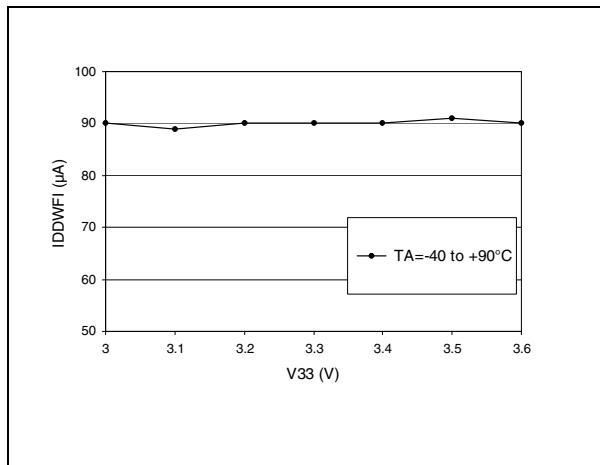
Negative injection disturbs the analog performance of the device. See note in [Section 4.3.11: ADC characteristics on page 66](#).

When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Only when using external 1.8V power supply. All the power (V_{18} , $V_{18\text{BKP}}$) and ground (V_{SS18} , V_{SSBKP}) pins must always be connected to the external 1.8V supply.

Table 10. Thermal characteristics

| Symbol | Ratings | Value | Unit |
|-----------|---|-------------|------|
| T_{STG} | Storage temperature range | -65 to +150 | °C |
| T_J | Maximum junction temperature (see Section 5.2: Thermal characteristics on page 73) | | |

Figure 11. STOP I_{DD} vs. V₃₃**Figure 12. STANDBY I_{DD} vs. V₃₃****Figure 13. WFI I_{DD} vs. V₃₃**

4.3.2 Clock and timing characteristics

External clock sources

Subject to general operating conditions for V_{33} , and T_A .

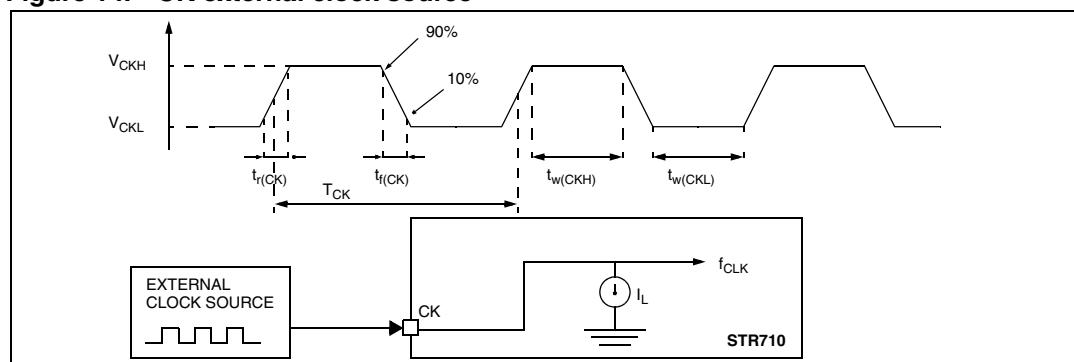
Table 16. CK external clock characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|------------------------------------|----------------------------------|---------------|-----|---------------|---------|
| f_{CK} | External clock source frequency | | 0 | | 16.5 | MHz |
| V_{CKH} | CK input pin high level voltage | | 0.7x V_{33} | | V_{33} | V |
| V_{CKL} | CK input pin low level voltage | | V_{SS} | | 0.3x V_{33} | |
| $t_w(CK)$ $t_w(CK)$ | CK high or low time ¹⁾ | | 25 | | | ns |
| $t_r(CK)$ $t_f(CK)$ | CK rise or fall time ¹⁾ | | | | 20 | |
| $C_{IN(CK)}$ | CK input capacitance ¹⁾ | | | 5 | | pF |
| DuCy(XT1) | Duty cycle | | 40 | | 60 | % |
| I_L | CK Input leakage current | $V_{SS} \leq V_{IN} \leq V_{33}$ | | | ± 1 | μA |

Notes:

1. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 14. CK external clock source



4.3.3 Memory characteristics

Flash memory

$V_{33} = 3.0$ to $3.6V$, $T_A = -40$ to $85^\circ C$ unless otherwise specified.

Table 22. Flash memory characteristics

| Symbol | Parameter | Test conditions | Value | | | Unit |
|----------------|------------------------------------|--|-------|------------|-------------------|---------|
| | | | Min. | Typ | Max ¹⁾ | |
| t_{PW} | Word Program | | | 40 | | μs |
| t_{PDW} | Double Word Program | | | 60 | | μs |
| t_{PB0} | Bank 0 Program (256K) | Double Word Program | | 1.6 | 2.1 | s |
| t_{PB1} | Bank 1 Program (16K) | Double Word Program | | 130 | 170 | ms |
| t_{ES} | Sector Erase (64K) | Not preprogrammed Preprogrammed | | 2.3 1.9 | 4.0 3.3 | s |
| t_{ES} | Sector Erase (8K) | Not preprogrammed Preprogrammed | | 0.7 0.6 | 1.1 1.0 | s |
| t_{ES} | Bank 0 Erase (256K) | Not preprogrammed Preprogrammed | | 8.0 6.6 | 13.7 11.2 | s |
| t_{ES} | Bank 1 Erase (16K) | Not preprogrammed Preprogrammed | | 0.9 0.8 | 1.5 1.3 | s |
| $t_{RPD}^{2)}$ | Recovery when disabled | | | | 20 | μs |
| $t_{PSL}^{2)}$ | Program Suspend Latency | | | | 10 | μs |
| $t_{ESL}^{2)}$ | Erase Suspend Latency | | | | 300 | μs |
| N_{END_B0} | Endurance (Bank 0 sectors) | | 10 | | | kcycles |
| N_{END_B1} | Endurance (Bank 1 sectors) | | 100 | | | kcycles |
| t_{RET} | Data Retention (Bank 0 and Bank 1) | $T_A=85^\circ$ | 20 | | | Years |
| t_{ESR} | Erase Suspend Rate | Min time from Erase Resume to next Erase Suspend | 20 | | | ms |

Notes:

1. $T_A=45^\circ C$ after 0 cycles. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production

