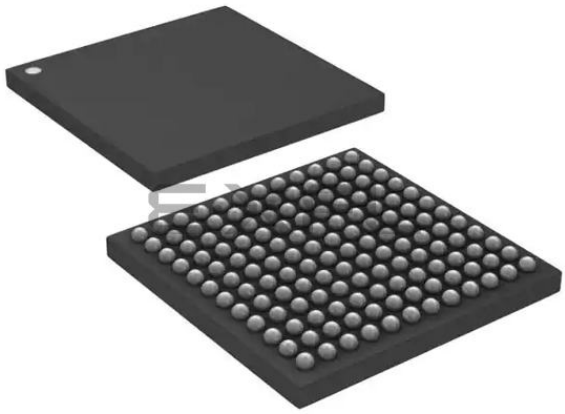

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, HDLC, I²C, SmartCard, SPI, UART/USART, USB
Peripherals	PWM, WDT
Number of I/O	48
Program Memory Size	256KB (256K x 8 + 16K)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str710fz2h6

Contents

3.3 Pin description for 144-pin packages

Figure 2. STR710 LQFP pinout

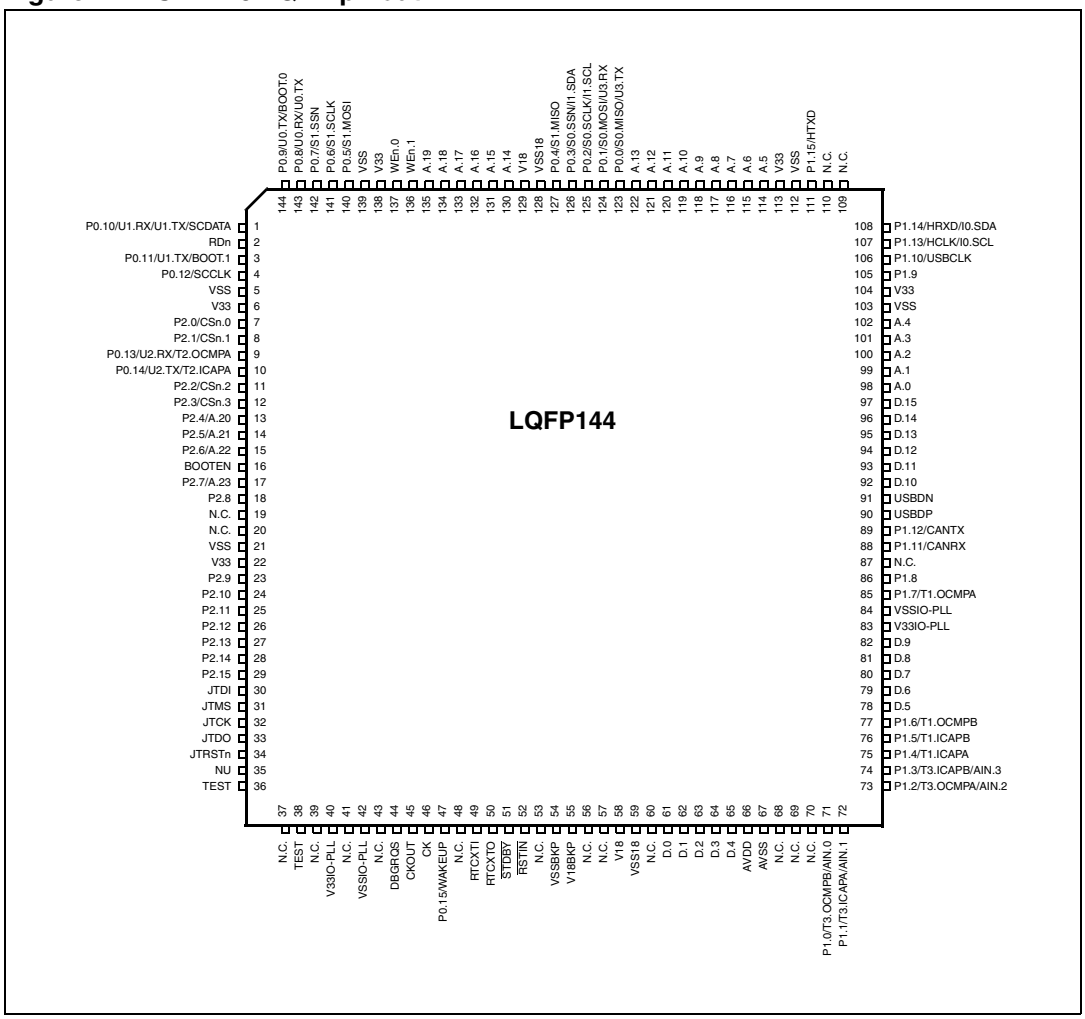


Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP			
13	E3	P2.4/A.20	I/O	pd[3]	C_T		8mA	X	X		Port 2.4	External Memory Interface: address bus
14	E4	P2.5/A.21	I/O	pd[3]	C_T		8mA	X	X		Port 2.5	
15	F1	P2.6/A.22	I/O	pd[3]	C_T		8mA	X	X		Port 2.6	
16	G1	BOOTEN	I		C_T						Boot control input. Enables sampling of BOOT[1:0] pins	
17	E5	P2.7/A.23	I/O	pd[3]	C_T		8mA	X	X		Port 2.7	External Memory Interface: address bus
18	F2	P2.8	I/O	pu	C_T	X	4mA	X	X		Port 2.8	External interrupt INT2
19	F3	N.C.									Not connected (not bonded)	
20	F4	N.C.									Not connected (not bonded)	
21	F5	V_{SS}	S								Ground voltage for digital I/Os[4]	
22	F6	V_{33}	S								Supply voltage for digital I/Os[4]	
23	G2	P2.9	I/O	pu	C_T	X	4mA	X	X		Port 2.9	External interrupt INT3
24	G3	P2.10	I/O	pu	C_T	X	4mA	X	X		Port 2.10	External interrupt INT4
25	G4	P2.11	I/O	pu	C_T	X	4mA	X	X		Port 2.11	External interrupt INT5
26	H1	P2.12	I/O	pu	C_T		4mA	X	X		Port 2.12	
27	J1	P2.13	I/O	pu	C_T		4mA	X	X		Port 2.13	
28	G5	P2.14	I/O	pu	C_T		4mA	X	X		Port 2.14	
29	K1	P2.15	I/O	pu	C_T		4mA	X	X		Port 2.15	
30	L1	JTDI	I		T_T						JTAG Data input. External pull-up required.	
31	H2	JTMS	I		T_T						JTAG Mode Selection Input. External pull-up required.	
32	H3	JTCK	I		C						JTAG Clock Input. External pull-up or pull-down required.	
33	H4	JTDO	O				8mA		X		JTAG Data output. **Note:** Reset state = HiZ.	
34	J2	JTRST	I		T_T						JTAG Reset Input. External pull-up required.	
35	J3	NU									Reserved, must be forced to ground.	
36	K2	TEST									Reserved, must be forced to ground.	
37	M1	N.C.									Not connected (not bonded)	
38	L2	TEST									Reserved, must be forced to ground.	
39	L3	N.C.									Not connected (not bonded)	

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
125	A7	P0.2/S0.SCLK /I1.SCL	I/O	pu	C_T	X	4mA	X	X		Port 0.2	BSPI0: Serial Clock	I2C1: Serial clock
												Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
126	A6	P0.3/S0.$\overline{SS}$/ I1.SDA	I/O	pu	C_T		4mA	X	X		Port 0.3	SPI0: Slave Select input active low.	I2C1: Serial Data
												Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
127	C7	P0.4/S1.MISO	I/O	pu	C_T		4mA	X	X		Port 0.4	SPI1: Master in/Slave out data	
128	D7	V_{SS18}	S								Stabilization for main voltage regulator.		
129	E7	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
130	F7	A.14	O	7)			8mA		X		External Memory Interface: address bus		
131	B6	A.15	O	7)			8mA		X				
132	C6	A.16	O	7)			8mA		X				
133	D6	A.17	O	7)			8mA		X				
134	E6	A.18	O	7)			8mA		X				
135	A5	A.19	O	7)			8mA		X				
136	B5	$\overline{WE}$.1	O	5)			8mA		X		External Memory Interface: active low MSB write enable output		
137	C5	$\overline{WE}$.0	O	5)			8mA		X		External Memory Interface: active low LSB write enable output		
138	A3	V_{33}	S								Supply voltage for digital I/Os[4]		
139	A2	V_{SS}	S								Ground voltage for digital I/Os[4]		
140	D5	P0.5/S1.MOSI	I/O	pu	C_T		4mA	X	X		Port 0.5	SPI1: Master out/Slave In data	
141	A4	P0.6/S1.SCLK	I/O	pu	C_T	X	4mA	X	X		Port 0.6	SPI1: Serial Clock	
142	B4	P0.7/S1.$\overline{SS}$	I/O	pu	C_T		4mA	X	X		Port 0.7	SPI1: Slave Select input active low	

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1)]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
20	P0.15/ WAKEUP	I		T_T	X				X	Port 0.15	Wakeup from Standby mode input.	
										Note: This port is input only.		
21	RTCXTI									Realtime Clock input and input of 32 kHz oscillator amplifier circuit		
22	RTCXTO									Output of 32 kHz oscillator amplifier circuit		
23	$\overline{STDBY}$	I/O		C_T		4mA	X		X	Input: Hardware Standby mode entry input active low. **Caution:** External pull-up to V_{33} required to select normal mode. Output: Standby mode active low output following Software Standby mode entry. **Note**: In Standby mode all pins are in high impedance except those marked Active in Stdby.		
24	$\overline{RSTIN}$	I		C_T					X	Reset input		
25	V_{SSBKP}			S					X	Stabilization for low power voltage regulator.		
26	V_{18BKP}			S					X	Stabilization for low power voltage regulator. Requires external capacitors of at least 1µF between V_{18BKP} and $V_{SS18BKP}$. See *Figure 5*. **Note:** If the low power voltage regulator is bypassed, this pin can be connected to an external 1.8V supply.		
27	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
28	V_{SS18}	S								Stabilization for main voltage regulator.		
29	V_{DDA}	S								Supply voltage for A/D Converter		
30	V_{SSA}	S								Ground voltage for A/D Converter		
31	P1.0/T3.OCMPB/AIN.0	I/O	pu	C_T		4mA	X	X		Port 1.0	Timer 3: Output Compare B	ADC: Analog input 0
32	P1.1/T3.ICAPA/T3.EXTCLK/AIN.1	I/O	pu	C_T		4mA	X	X		Port 1.1	Timer 3: Input Capture A or External Clock input	ADC: Analog input 1
33	P1.2/T3.OCMPA/AIN.2	I/O	pu	C_T		4mA	X	X		Port 1.2	Timer 3: Output Compare A	ADC: Analog input 2
34	P1.3/T3.ICAPB/AIN.3	I/O	pu	C_T		4mA	X	X		Port 1.3	Timer 3: Input Capture B	ADC: Analog input 3
35	P1.4/T1.ICAPA/T1.EXTCLK	I/O	pu	C_T		4mA	X	X		Port 1.4	Timer 1: Input Capture A	Timer 1: External Clock input

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1)]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
52	P0.0/S0.MISO /U3.TX	I/O	pu	C_T		4mA	X	X		Port 0.0	SPI0 Master in/Slave out data	UART3 Transmit data output
											Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
53	P0.1/S0.MOSI /U3.RX	I/O	pu	C_T	X	4mA	X	X		Port 0.1	BSPI0: Master out/Slave in data	UART3: Receive Data input
											Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
54	P0.2/S0.SCLK /I1.SCL	I/O	pu	C_T	X	4mA	X	X		Port 0.2	BSPI0: Serial Clock	I2C1: Serial clock
											Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
55	P0.3/S0.$\overline{SS}$/I1 .SDA	I/O	pu	C_T		4mA	X	X		Port 0.3	SPI0: Slave Select input active low.	I2C1: Serial Data
											Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
56	P0.4/S1.MISO	I/O	pu	C_T		4mA	X	X		Port 0.4	SPI1: Master in/Slave out data	
57	V_{SS18}	S								Stabilization for main voltage regulator.		
58	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
59	V_{SS}	S								Ground voltage for digital I/Os		
60	P0.5/S1.MOSI	I/O	pu	C_T		4mA	X	X		Port 0.5	SPI1: Master out/Slave In data	
61	P0.6/S1.SCLK	I/O	pu	C_T	X	4mA	X	X		Port 0.6	SPI1: Serial Clock	
62	P0.7/S1.$\overline{SS}$	I/O	pu	C_T		4mA	X	X		Port 0.7	SPI1: Slave Select input active low	

3.6 I/O port configuration

Table 6. Port bit configuration table

Configuration mode		Input buffer	PxD register		PxC2 register	PxC1 register	PxC0 register
			Read access	Write access			
INPUT	TTL Input Floating	TTL floating	I/O pin	don't care	0	0	1
	CMOS Input Floating	CMOS floating	I/O pin	don't care	0	1	0
	CMOS Input Pull-Down (IPUPD)	CMOS Pull-Down	I/O pin	0	0	1	1
	CMOS Input Pull-Up (IPUPD)	CMOS Pull-Up	I/O pin	1	0	1	1
	Analog input	AIN	0	don't care	0	0	0
OUTPUT	Output Open-Drain	N.A.	I/O pin	0 or 1	1	0	0
	Output Push-Pull	N.A.	last value written	0 or 1	1	0	1
	Alternate Function Open-Drain	CMOS floating	I/O pin	don't care	1	1	0
	Alternate Function Push-Pull	CMOS floating	I/O pin	don't care	1	1	1

Legend:

AIN: Analog Input

CMOS: CMOS Input levels

IPUPD: Input Pull Up /Pull Down

TTL: TTL Input levels

N.A.: not applicable. In Output mode, a read access to the port gets the output latch value.

Figure 7. Mapping of Flash memory versions

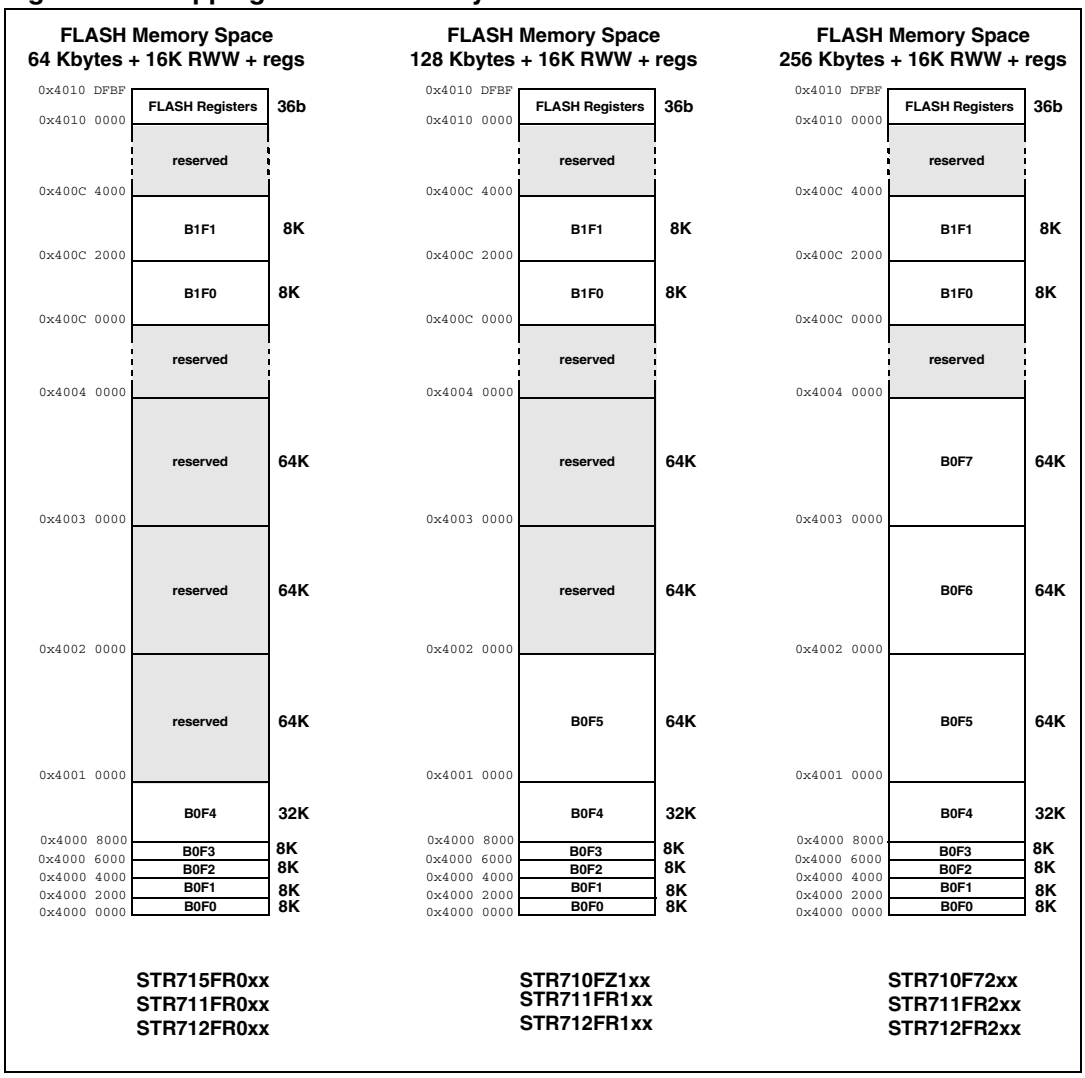


Table 7. RAM memory mapping

Part number	RAM size	Start address	End address
STR715FR0xx STR711FR0xx STR712FR0xx	16 Kbytes	0x2000 0000	0x2000 3FFF
STR710FZ1xx STR711FR1xx STR712FR1xx	32 Kbytes	0x2000 0000	0x2000 7FFF
STR710FR2xx STR710Rxx STR711FR2xx STR712FR2xx	64 Kbytes	0x2000 0000	0x2000 FFFF

4 Electrical parameters

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

4.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25°C and T_A=$T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

4.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25°C, V_{33}=3.3V (for the 3.0V≤V_{33}≤3.6V voltage range) and V_{18}=1.8V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

4.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

4.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

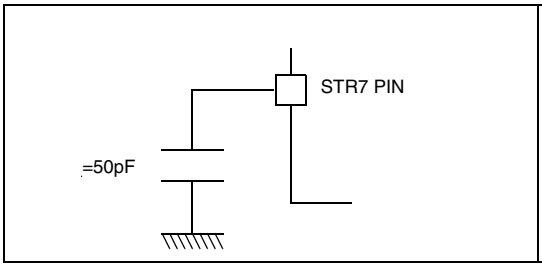


Figure 10. Pin input voltage

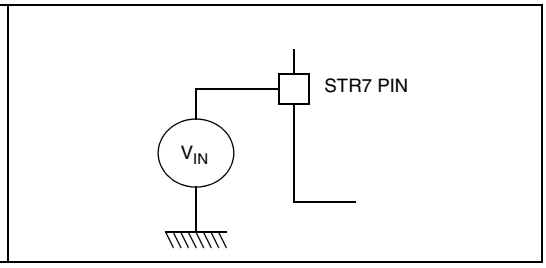


Table 9. Current characteristics

Symbol	Ratings	Max.	Unit
I_{V33}	Total current into $V_{33}/V_{33IO-PLL}$ power lines (source) [2]	150	mA
I_{VSS}	Total current out of $V_{SS}/V_{SSIO-PLL}$ ground lines (sink) [2]	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$ [1] [3]	Injected current on $\overline{RSTIN}$ pin	± 5	
	Injected current on CK pin	± 5	
	Injected current on any other pin [4]	± 5	
$\Sigma I_{INJ(PIN)}$ [1]	Total injected current (sum of all I/O and control pins) [4]	± 25	

The $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{33}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected. Data based on T_A = 25 °C.

All 3.3V power (V_{33}, AV_{DD}, $V_{33IO-PLL}$) and ground (V_{SS}, AV_{SS}, $V_{SSIO-PLL}$) pins must always be connected to the external 3.3V supply.

Negative injection disturbs the analog performance of the device. See note in *Section 4.3.11: ADC characteristics on page 66*.

When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Only when using external 1.8V power supply. All the power (V_{18}, V_{18BKP}) and ground (V_{SS18}, V_{SSBKP}) pins must always be connected to the external 1.8V supply.

Table 10. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature (see *Section 5.2: Thermal characteristics on page 73*)		

4.3 Operating conditions

Subject to general operating conditions for V_{33}, and T_A.

Table 11. General operating conditions

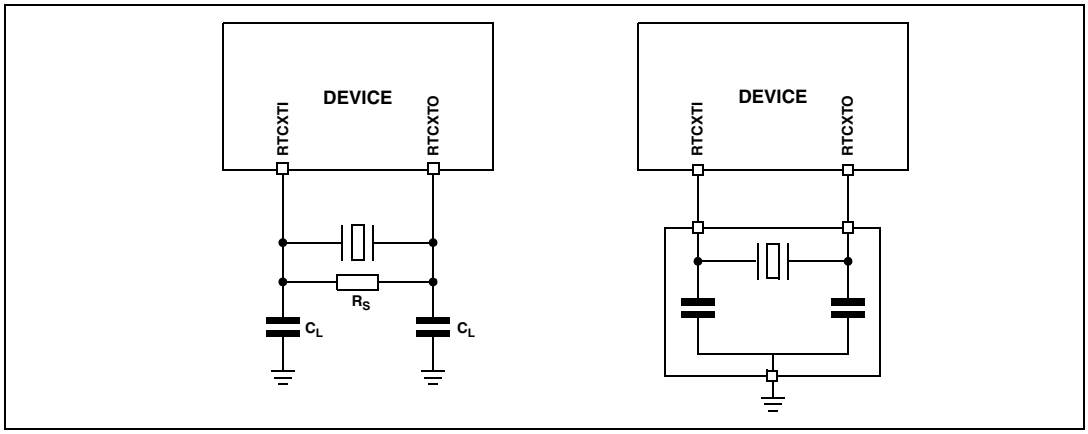
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	Internal CPU Clock frequency	Accessing SRAM or external memory with 0 wait states	0	66	MHz
		Accessing FLASH in burst mode	0	50	
		Executing from FLASH with RWW	0	45 [1)]	
		Accessing FLASH with 0 wait states	0	33	
f_{PCLK}	Internal APB Clock frequency		0	33	MHz
V_{33}	Standard Operating Voltage (includes V_{33I0_PLL})		3.0	3.6	V
V_{18BKP}	Backup Operating Voltage		1.4	1.8	V
T_A	Ambient temperature range	6 Partnumber Suffix	-40	85	°C

1. Data guaranteed by characterization, not tested in production

Table 12. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{V33}	V_{33} rise time rate	Subject to general operating conditions for T_A.	20			µs/V
					20	ms/V

Figure 16. RTC crystal oscillator and resonator



PLL electrical characteristics

V_{33} = 3.0 to 3.6V, $V_{33IOPLL}$ = 3.0 to 3.6V, T_A = -40 / 85 °C unless otherwise specified.

Table 19. PLL1 characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$f_{PLLCLK1}$	PLL multiplier output clock				165	MHz
f_{PLL1}	PLL input clock	FREF_RANGE = 0	1.5		3.0	MHz
		FREF_RANGE = 1 MX[1:0]='00' or '01'	3.0		8.25	MHz
		FREF_RANGE = 1 MX[1:0]='10' or '11'	3.0		6	MHz
	PLL input clock duty cycle		25		75	%
f_{FREE1}	PLL free running frequency	FREF_RANGE = 0 MX[1:0]='01' or '11'		125		kHz
		FREF_RANGE = 0 MX[1:0]='00' or '10'		250		kHz
		FREF_RANGE = 1 MX[1:0]='01' or '11'		250		kHz
		FREF_RANGE = 1 MX[1:0]='00' or '10'		500		kHz
t_{LOCK1}	PLL lock time	FREF_RANGE = 0 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			300	µs
		FREF_RANGE = 1 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			600	µs

4.3.5 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{33} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

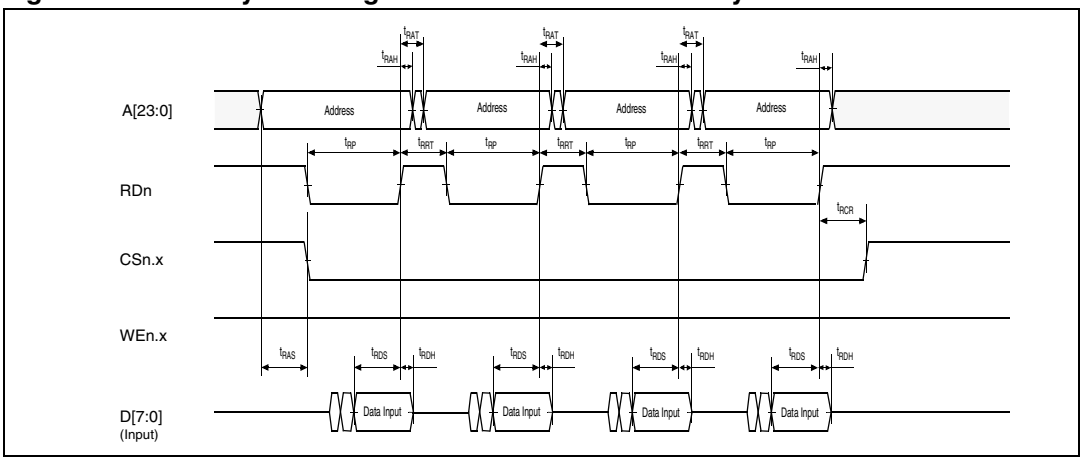
Table 27. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage 1)	CMOS ports			$0.3V_{33}$	V
V_{IH}	Input high level voltage 1)		$0.7V_{33}$			
V_{hys}	Schmitt trigger voltage hysteresis 2)			0.8		V
V_{IL}	Input low level voltage 1)	P0.15 WAKEUP		0.9	0.8	V
V_{IH}	Input high level voltage 1)		2	1.35		
V_{hys}	Schmitt trigger voltage hysteresis 2)			0.4		V
V_{IL}	Input low level voltage 1)	TTL ports			0.8	V
V_{IH}	Input high level voltage 1)		2.0			
$I_{INJ(PIN)}$	Injected Current on any I/O pin				± 4	mA
$\Sigma I_{INJ(PIN)}$ 3)	Total injected current (sum of all I/O and control pins)				± 25	
I_{lkg}	Input leakage current 4)	$V_{SS} \le V_{IN} \le V_{33}$			±1	µA
R_{PU}	Weak pull-up equivalent resistor5)	$V_{IN}=V_{SS}$	110	150	700	kΩ
R_{PD}	Weak pull-down equivalent resistor5)	$V_{IN}=V_{33}$	110	150	700	kΩ
C_{IO}	I/O pin capacitance			5		pF

Notes:

1. Data based on characterization results, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
3. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{33}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Refer to *Section 4.2 on page 35* for more details.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. The R_{PU} pull-up and R_{PD} pull-down equivalent resistor are based on a resistive transistor (corresponding I_{PU} and I_{PD} current characteristics described in *Figure 18* to *Figure 19*).

Figure 28. Read cycle timing: 32-bit read on 8-bit memory



See *Table 32* for read timing data.

Figure 29. Write cycle timing: 16-bit write on 16-bit memory

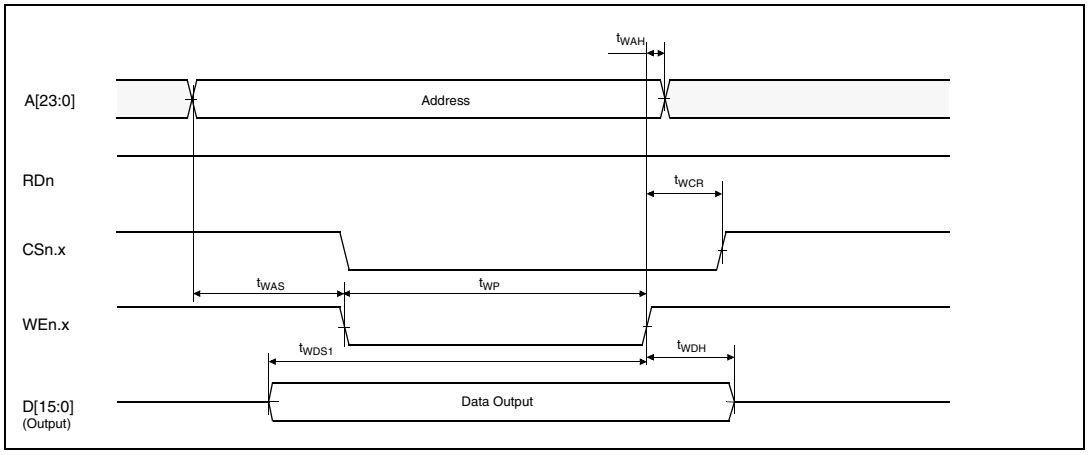
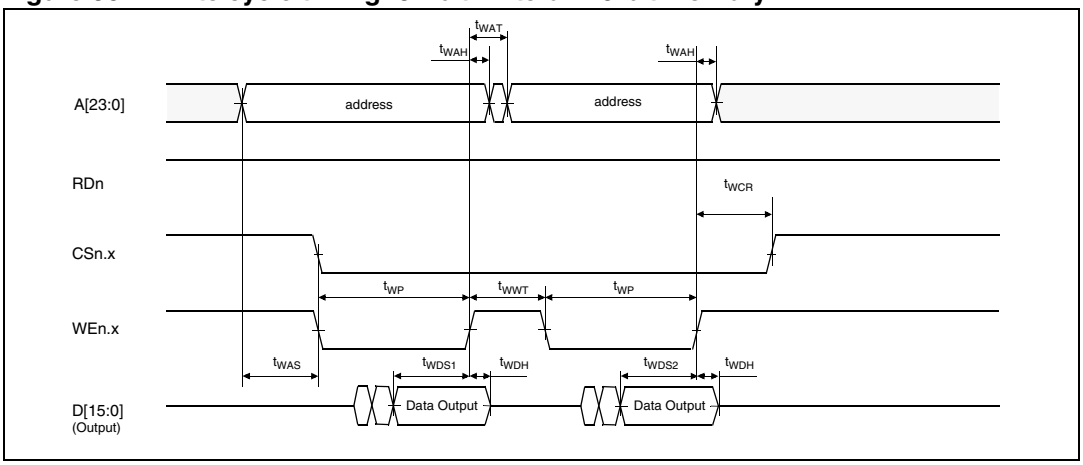


Figure 30. Write cycle timing: 32-bit write on 16-bit memory



See *Table 44* for write timing data.

Table 34. I2C characteristics

Symbol	Parameter	Standard mode I^2C		Fast mode I^2C[5]		Unit
		Min [1]	Max [1]	Min [1]	Max [1]	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0 [3]		0 [2]	900 [3]	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	20+0.1C_b	300	
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

Notes:

1. Data based on standard I^2C protocol requirement, not tested in production.
2. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
3. The maximum hold time $t_{h(SDA)}$ is not applicable.
4. Measurement points are done at CMOS levels: $0.3xV_{DD}$ and $0.7xV_{DD}$.
5. f_{PCLK1}, must be at least 8 MHz to achieve max fast I^2C speed (400 kHz).
6. The following table gives the values to be written in the I2CCCR register to obtain the required I^2C SCL line frequency.

Figure 34. SPI slave timing diagram with CPHA=0[1)]

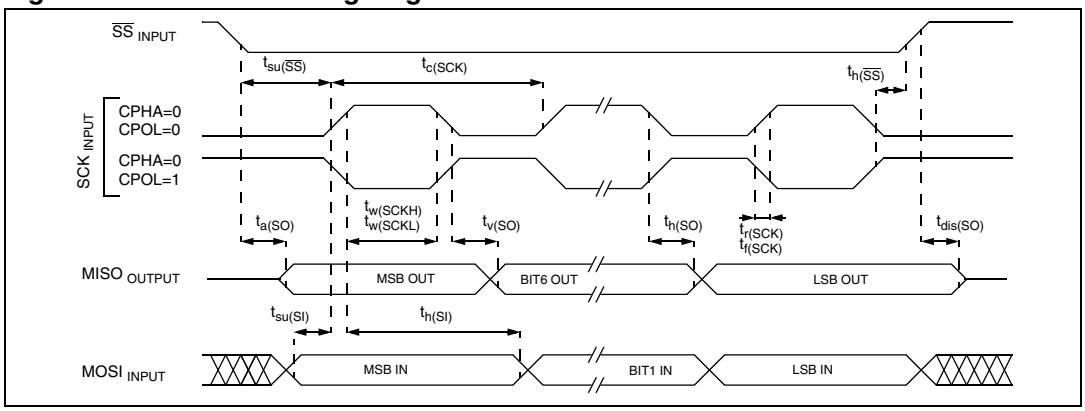


Figure 35. SPI slave timing diagram with CPHA=1[1)]

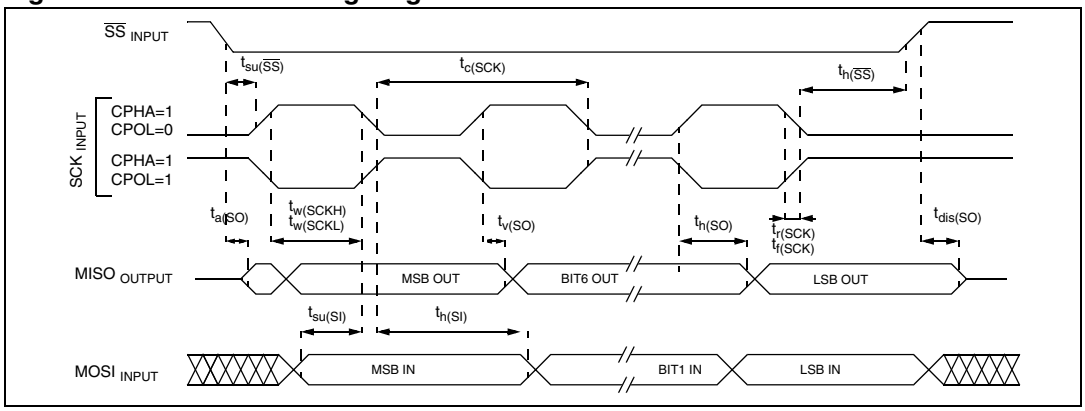
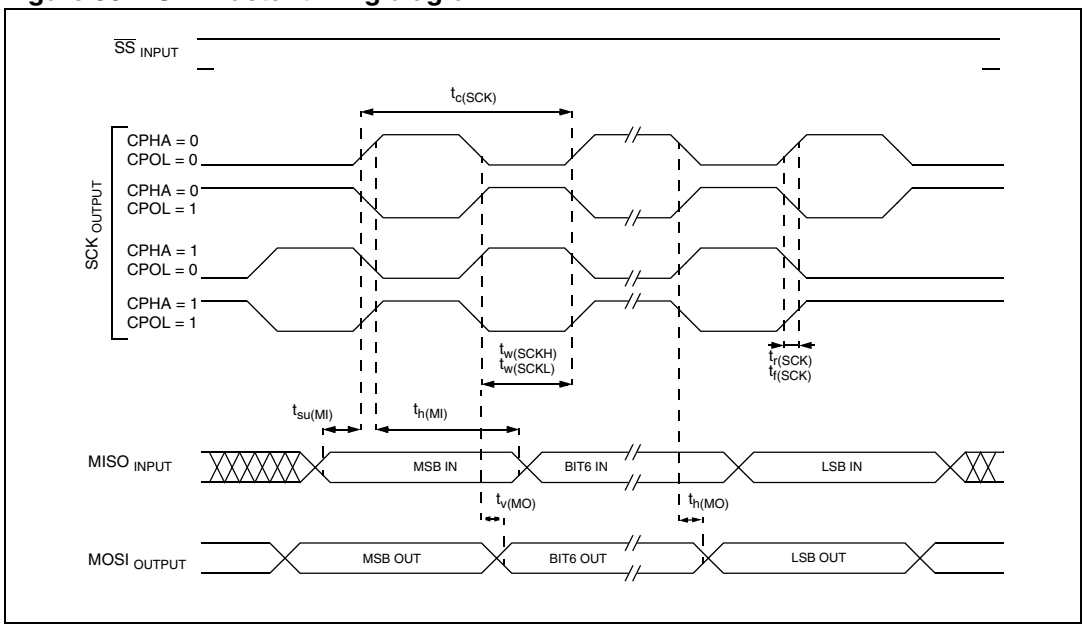


Figure 36. SPI master timing diagram[1)]



1. Measurement points are done at CMOS levels: $0.3xV_{33}$ and $0.7xV_{33}$

4.3.11 ADC characteristics

Subject to general operating conditions for AV_{DD}, f_{PCLK2}, and T_A unless otherwise specified.

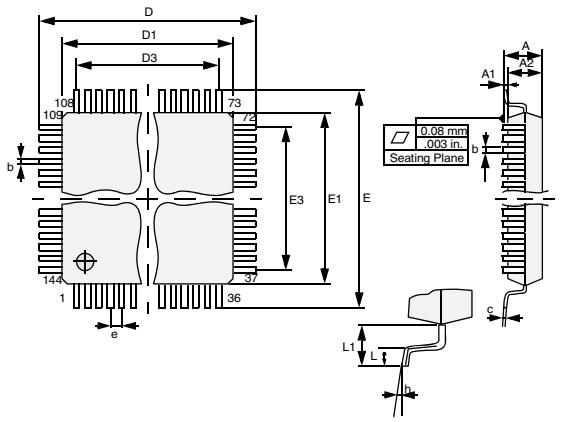
Table 40. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
f_{MOD}	Modulator Oversampling frequency				2.1	MHz
V_{AIN}	Conversion voltage range [2][3]		0		2.5	V
I_{lkg}	Negative input leakage current on analog pins	$V_{IN}<V_{SS}$, $\lvert I_{IN} \rvert <$ 400µA on adjacent analog pin		5	6	µA
PBR	Passband Ripple				0.1	dB
SINAD	S/N and Distortion		56	63		dB
THD	Total Harmonic Distortion		60	74		dB
Z_{IN}	Input Impedance	f_{MOD} = 2 MHz	1			MΩ
C_{ADC}	Internal sample and hold capacitor				3.2	pF
t_{CONV}	Total Conversion time (including sampling time)		2048/ f_{MOD} (max)			
I_{ADC}	Normal mode	T_A = 27 °C		2.5	3.0	mA
	Standby mode	T_A = 27 °C			1	µA

Notes:

1. Unless otherwise specified, typical data are based on T_A=25°C and AV_{DD}-AV_{SS}=3.3V. They are given only as design guidelines and are not tested.
2. Any added external serial resistor will downgrade the ADC accuracy (especially for resistance greater than 10kΩ). Data based on characterization results, not tested in production.
3. Calibration is needed once after each power-up.

Figure 41. 144-Pin low profile quad flat package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053		0.057
b	0.17	0.22	0.27	0.007		0.011
c	0.09		0.20	0.004		0.008
D	21.80	22.00	22.20	0.858	0.867	0.874
D1	19.80	20.00	20.20	0.780	0.787	0.795
D3		17.50			0.689	
E	21.80	22.00	22.20	0.858	0.867	0.874
E1	19.80	20.00	20.20	0.780	0.787	0.795
E3		17.50			0.689	
e		0.50			0.020	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	144					

Jedec Ref. MS-026-BFB

1.Values in inches are converted from mm and rounded to 3 decimal digits.

Recommended footprint (dimensions in mm)

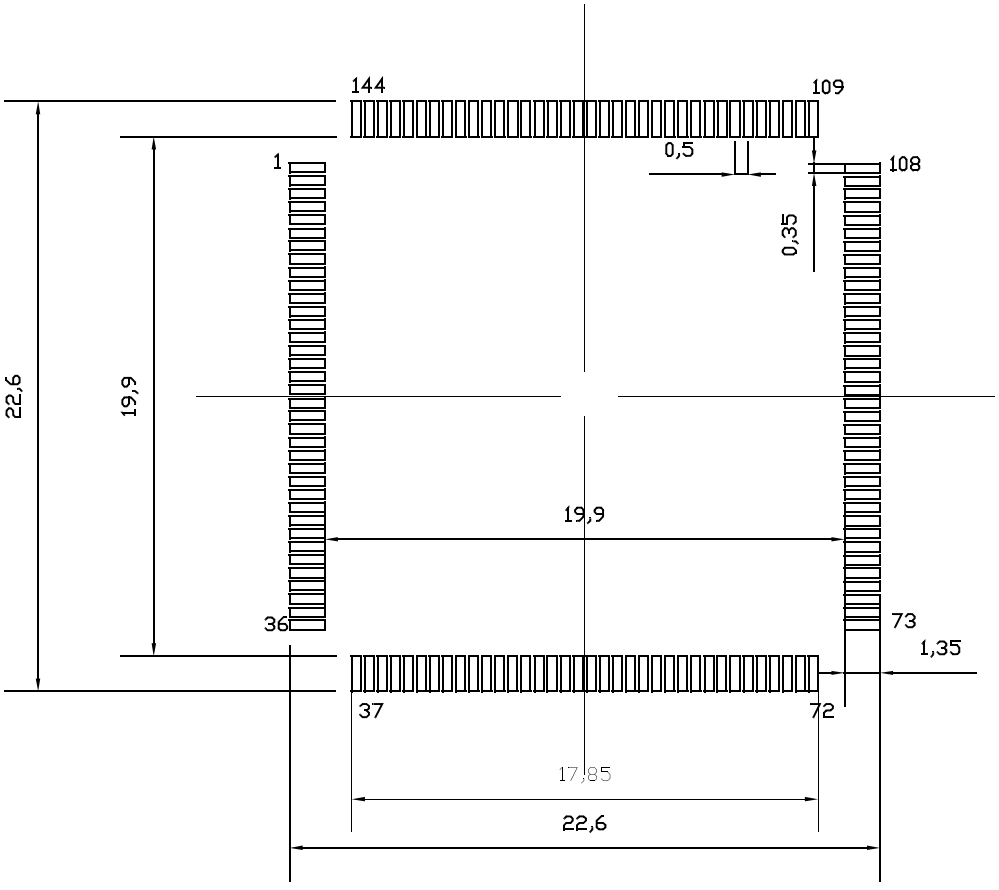
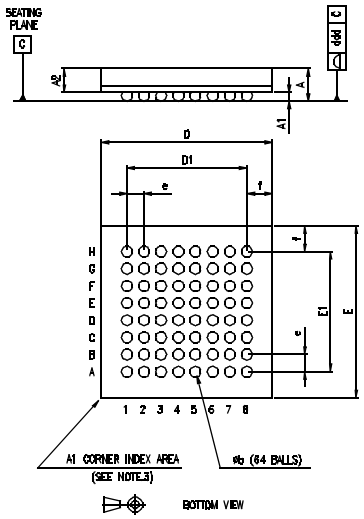
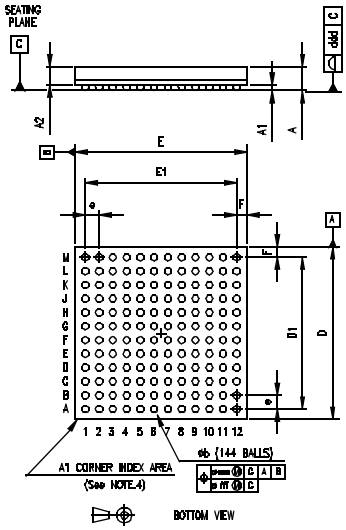


Figure 42. 64-Low profile fine pitch ball grid array package



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	1.210		1.700	0.048		0.067
A1	0.270			0.011		
A2		1.120			0.044	
b	0.450	0.500	0.550	0.018	0.020	0.022
D	7.750	8.000	8.150	0.305	0.315	0.321
D1		5.600			0.220	
E	7.750	8.000	8.150	0.305	0.315	0.321
E1		5.600			0.220	
e	0.720	0.800	0.880	0.028	0.031	0.035
f	1.050	1.200	1.350	0.041	0.047	0.053
ddd			0.120			0.005
	Number of Pins					
N	64					

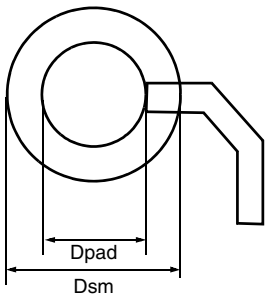
Figure 43. 144-low profile fine pitch ball grid array package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	1.21		1.70	0.0476		0.0669
A1	0.21			0.0083		
A2		1.085			0.0427	
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
D	9.85	10.00	10.15	0.3878	0.3937	0.3996
D1		8.80			0.3465	
E	9.85	10.00	10.15	0.3878	0.3937	0.3996
E1		8.80			0.3465	
e		0.80			0.0315	
F		0.60			0.0236	
ddd			0.10			0.0039
eee			0.15			0.0059
fff			0.08			0.0031
	Number of Pins					
N	144					

[1]Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. Recommended PCB design rules (0.80/0.75mm pitch BGA)



Dpad	0.37 mm
Dsm	0.52 mm typ. (depends on solder mask registration tolerance
Solder paste	0.37 mm aperture diameter
– Non solder mask defined pads are recommended – 4 to 6 mils screen print	

5.2 Thermal characteristics

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

- T_A is the Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the Chip Internal Power.

$P_{I/O}$ represents the Power Dissipation on Input and Output Pins;

Most of the time for the application $P_{I/O} < P_{INT}$ and can be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273°C) \quad (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

where:

K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 42. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal Resistance Junction-Ambient LQFP 144 - 20 x 20 mm / 0.5 mm pitch	42	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LFBGA 144 - 10 x 10 x 1.7mm	50	°C/W