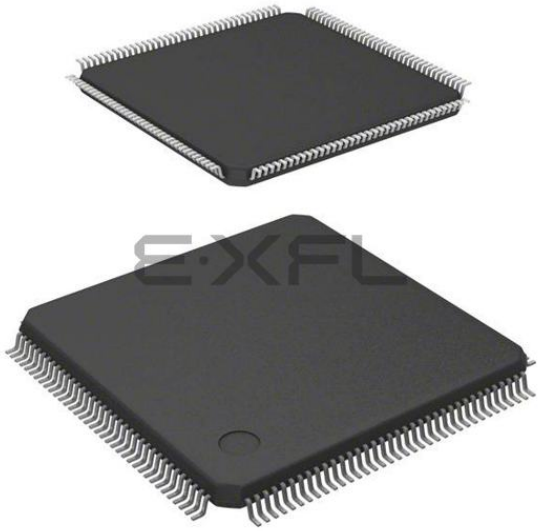

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, HDLC, I²C, SmartCard, SPI, UART/USART, USB
Peripherals	PWM, WDT
Number of I/O	48
Program Memory Size	256KB (256K x 8 + 16K)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str710fz2t6

Contents

List of figures

1 Introduction

This datasheet provides the STR71x pinout, ordering information, mechanical and electrical device characteristics.

For complete information on the STR71x microcontroller memory, registers and peripherals. please refer to the STR71x reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash programming reference manual.

For information on the ARM7TDMI core please refer to the ARM7TDMI technical reference manual.

Table 2. Device overview

Features	STR710 FZ1	STR710 FZ2	STR710 RZ	STR711 FR0	STR711 FR1	STR711 FR2	STR712 FR0	STR712 FR1	STR712 FR2	STR715 FRx
Flash - Kbytes	128+16	256+16	0	64+16	128+16	256+16	64+16	128+16	256+16	64+16
RAM - Kbytes	32	64	64	16	32	64	16	32	64	16
Peripheral Functions	CAN, EMI, USB, 48 I/Os			USB, 30 I/Os			CAN, 32 I/Os			32 I/Os
Operating Voltage	3.0 to 3.6 V									
Operating Temperature	-40 to +85°C or 0 to 70° C									
Packages	**T**=LQFP144 20 x 20 **H**=LFBGA144 10 x10			**T**=LQFP64 10 x10						

.

3 System architecture

Package choice: low pin-count 64-pin or feature-rich 144-pin LQFP or BGA

The STR71x family is available in 5 main versions.

The 144-pin versions have the full set of all features including CAN, USB and External Memory Interface (EMI).

- **STR710F:** 144-pin BGA or LQFP with CAN, USB and EMI
- **STR710R:** Flashless 144-pin BGA or LQFP with CAN, USB and EMI (no internal Flash memory)

The three 64-pin versions (LQFP) do not include External Memory Interface.

- **STR715F:** 64-pin LQFP without CAN or USB
- **STR711F:** 64-pin LQFP with USB
- **STR712F:** 64-pin LQFP with CAN

High speed Flash memory (STR71xF)

The Flash program memory is organized in two banks of 32-bit wide Burst Flash memories enabling true read-while-write (RWW) operation. Device Bank 0 is up to 256 Kbytes in size, typically for the application program code. Bank 1 is 16 Kbytes, typically used for storing data constants. Both banks are accessed by the CPU with zero wait states @ 33 MHz

Bank 0 memory endurance is 10K write/erase cycles and Bank 1 endurance is 100K write/erase cycles. Data retention is 20 years at 85°C on both banks. The two banks can be accessed independently in read or write. Flash memory can be accessed in two modes:

- Burst mode: 64-bit wide memory access at up to 50 MHz.
- Direct 32-bit wide memory access for deterministic operation at up to 33 MHz.

The STR7 embedded Flash memory can be programmed using In-Circuit Programming or In-Application programming.

IAP (in-application programming): The IAP is the ability to re-program the Flash memory of a microcontroller while the user program is running.

ICP (in-circuit programming): The ICP is the ability to program the Flash memory of a microcontroller using JTAG protocol while the device is mounted on the user application board.

The Flash memory can be protected against different types of unwanted access (read/write/erase). There are two types of protection:

- Sector Write Protection
- Flash Debug Protection (locks JTAG access)

Refer to the STR7 Flash Programming Reference manual for details.

Optional external memory (STR710)

The non-multiplexed 16-bit data/24-bit address bus available on the STR710 (144-pin) supports four 16-Mbyte banks of external memory. Wait states are programmable individually for each bank allowing different memory types (Flash, EPROM, ROM, SRAM etc.) to be used to store programs or data.

Figure 1 shows the general block diagram of the device family.

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1)]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
52	P0.0/S0.MISO /U3.TX	I/O	pu	C_T		4mA	X	X		Port 0.0	SPI0 Master in/Slave out data	UART3 Transmit data output
											Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
53	P0.1/S0.MOSI /U3.RX	I/O	pu	C_T	X	4mA	X	X		Port 0.1	BSPI0: Master out/Slave in data	UART3: Receive Data input
											Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
54	P0.2/S0.SCLK /I1.SCL	I/O	pu	C_T	X	4mA	X	X		Port 0.2	BSPI0: Serial Clock	I2C1: Serial clock
											Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
55	P0.3/S0.$\overline{SS}$/I1 .SDA	I/O	pu	C_T		4mA	X	X		Port 0.3	SPI0: Slave Select input active low.	I2C1: Serial Data
											Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
56	P0.4/S1.MISO	I/O	pu	C_T		4mA	X	X		Port 0.4	SPI1: Master in/Slave out data	
57	V_{SS18}	S								Stabilization for main voltage regulator.		
58	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
59	V_{SS}	S								Ground voltage for digital I/Os		
60	P0.5/S1.MOSI	I/O	pu	C_T		4mA	X	X		Port 0.5	SPI1: Master out/Slave In data	
61	P0.6/S1.SCLK	I/O	pu	C_T	X	4mA	X	X		Port 0.6	SPI1: Serial Clock	
62	P0.7/S1.$\overline{SS}$	I/O	pu	C_T		4mA	X	X		Port 0.7	SPI1: Slave Select input active low	

3.6 I/O port configuration

Table 6. Port bit configuration table

Configuration mode		Input buffer	PxD register		PxC2 register	PxC1 register	PxC0 register
			Read access	Write access			
INPUT	TTL Input Floating	TTL floating	I/O pin	don't care	0	0	1
	CMOS Input Floating	CMOS floating	I/O pin	don't care	0	1	0
	CMOS Input Pull-Down (IPUPD)	CMOS Pull-Down	I/O pin	0	0	1	1
	CMOS Input Pull-Up (IPUPD)	CMOS Pull-Up	I/O pin	1	0	1	1
	Analog input	AIN	0	don't care	0	0	0
OUTPUT	Output Open-Drain	N.A.	I/O pin	0 or 1	1	0	0
	Output Push-Pull	N.A.	last value written	0 or 1	1	0	1
	Alternate Function Open-Drain	CMOS floating	I/O pin	don't care	1	1	0
	Alternate Function Push-Pull	CMOS floating	I/O pin	don't care	1	1	1

Legend:

AIN: Analog Input

CMOS: CMOS Input levels

IPUPD: Input Pull Up /Pull Down

TTL: TTL Input levels

N.A.: not applicable. In Output mode, a read access to the port gets the output latch value.

Figure 7. Mapping of Flash memory versions

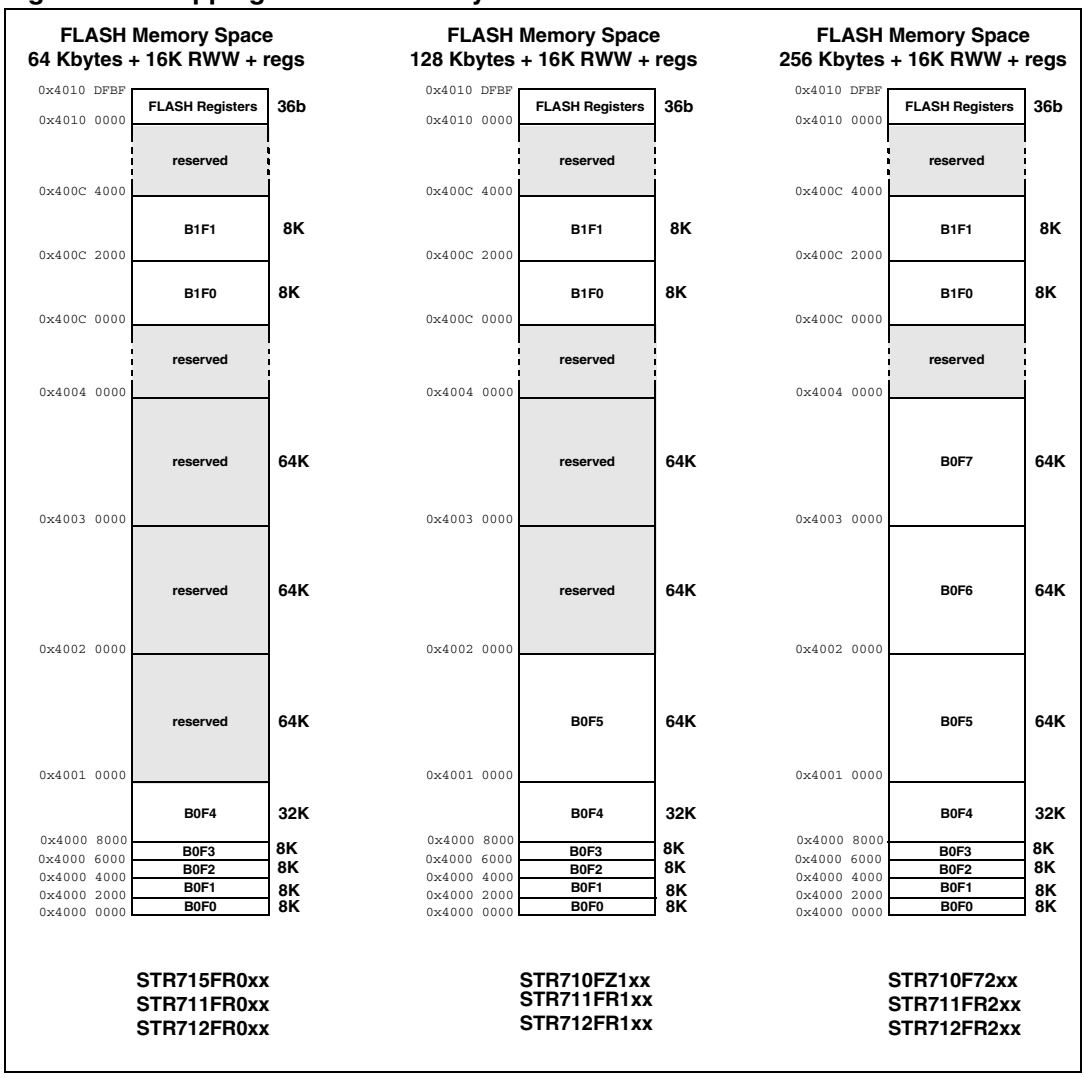


Table 7. RAM memory mapping

Part number	RAM size	Start address	End address
STR715FR0xx STR711FR0xx STR712FR0xx	16 Kbytes	0x2000 0000	0x2000 3FFF
STR710FZ1xx STR711FR1xx STR712FR1xx	32 Kbytes	0x2000 0000	0x2000 7FFF
STR710FR2xx STR710Rxx STR711FR2xx STR712FR2xx	64 Kbytes	0x2000 0000	0x2000 FFFF

4.3 Operating conditions

Subject to general operating conditions for V_{33}, and T_A.

Table 11. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	Internal CPU Clock frequency	Accessing SRAM or external memory with 0 wait states	0	66	MHz
		Accessing FLASH in burst mode	0	50	
		Executing from FLASH with RWW	0	45 [1)]	
		Accessing FLASH with 0 wait states	0	33	
f_{PCLK}	Internal APB Clock frequency		0	33	MHz
V_{33}	Standard Operating Voltage (includes V_{33I0_PLL})		3.0	3.6	V
V_{18BKP}	Backup Operating Voltage		1.4	1.8	V
T_A	Ambient temperature range	6 Partnumber Suffix	-40	85	°C

1. Data guaranteed by characterization, not tested in production

Table 12. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{V33}	V_{33} rise time rate	Subject to general operating conditions for T_A.	20			µs/V
					20	ms/V

Figure 11. STOP I_{DD} vs. V_{33}

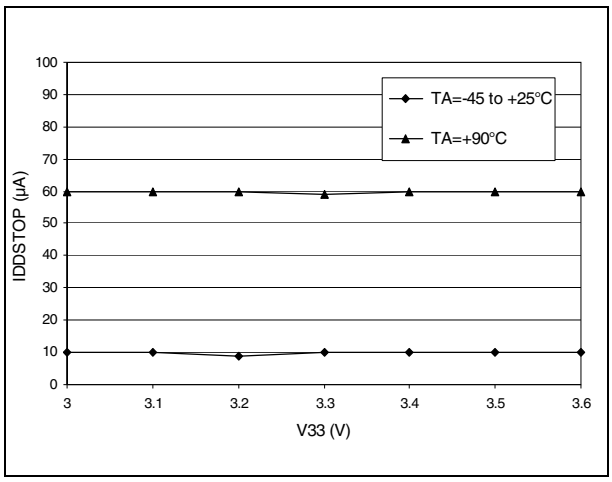


Figure 12. STANDBY I_{DD} vs. V_{33}

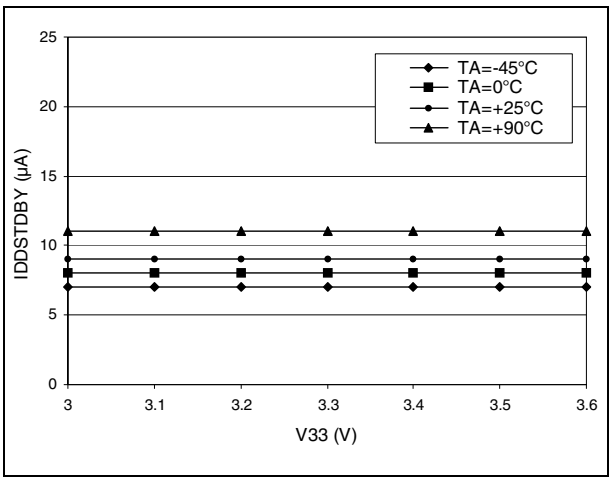


Figure 13. WFI I_{DD} vs. V_{33}

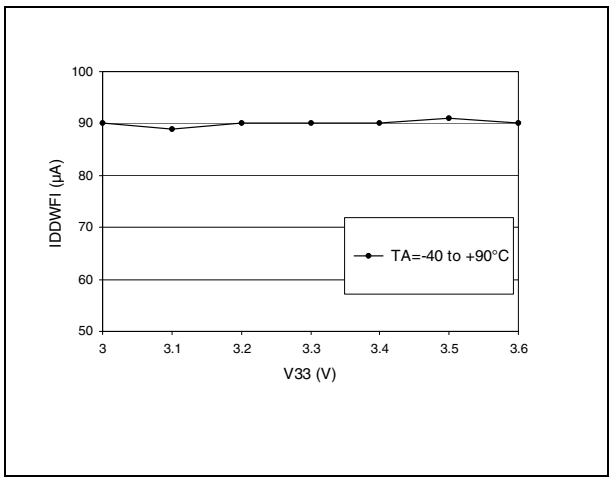


Table 17. RTCXT1 external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RTCXT1}	External clock source frequency		0		500	kHz
$V_{RTCXT1H}$	RTCXT1 input pin high level voltage		$0.7xV_{33}$		V_{33}	V
$V_{RTCXT1L}$	RTCXT1 input pin low level voltage		V_{SS}		$0.3xV_{33}$	
$t_{w(RTCXT1)}$ $t_{w(RTCXT1)}$	RTCXT1 high or low time [1]		100			ns
$t_{r(RTCXT1)}$ $t_{f(RTCXT1)}$	RTCXT1 rise or fall time [1]				5	
$C_{IN(RTCXT1)}$	RTCXT1 input capacitance[1]			5		pF
DuCy(RTCXT1)	Duty cycle		30		70	%
I_L	RTCXT1 Input leakage current	$V_{SS} \le V_{IN} \le V_{33}$			±1	µA

Notes:

1. Data based on design simulation and/or technology characteristics, not tested in production.

Table 25. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value [1]	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25°C	2000	V
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)		200	
$V_{ESD(CDM)}$	Electro-static discharge voltage (Charge Device Model)		750 on corner pins, 500 on others	

Notes:

1. Data based on characterization results, not tested in production.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Electrical sensitivities

Table 26. Static and dynamic latch-up

Symbol	Parameter	Conditions	Class[1]
LU	Static latch-up class	T_A=+25°C T_A=+85°C T_A=+105°C	A A A
DLU	Dynamic latch-up class	V_{DD}=3.3 V, f_{OSC4M}=4 MHz, f_{MCLK}=32 MHz, T_A=+25°C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

Figure 17. R_{PU} vs. V_{33} with $V_{IN}=V_{SS}$

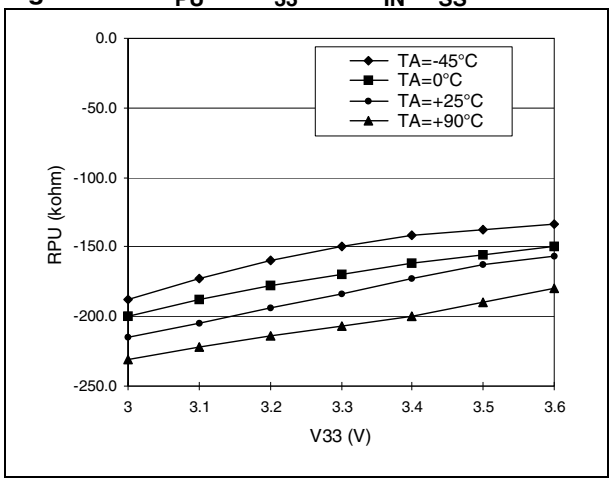


Figure 18. I_{PU} vs. V_{33} with $V_{IN}=V_{SS}$

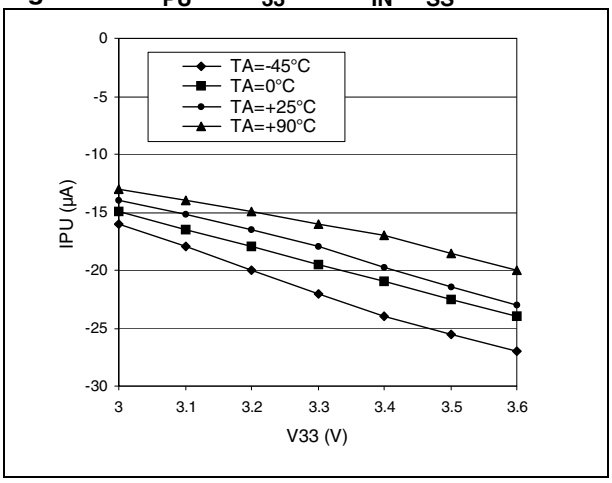


Figure 19. R_{PD} vs. V_{33} with $V_{IN}=V_{33}$

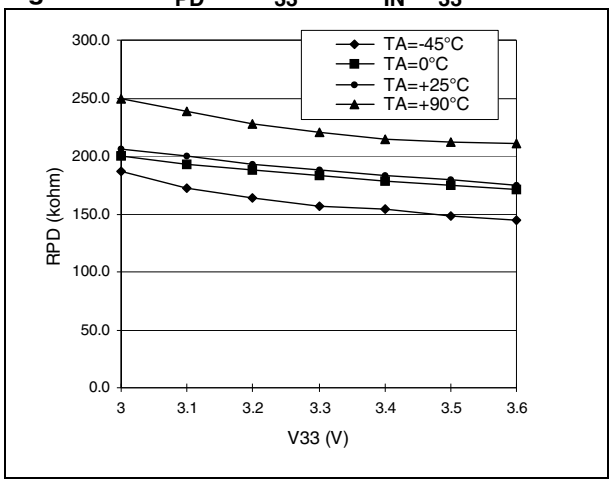
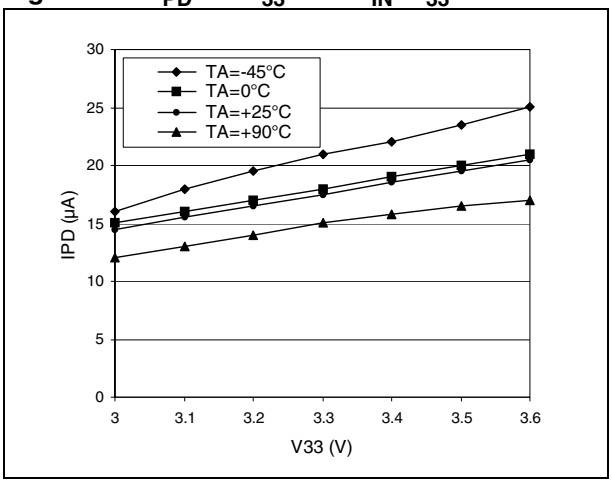


Figure 20. I_{PD} vs. V_{33} with $V_{IN}=V_{33}$



$\overline{\text{RSTIN}}$ pin

The $\overline{\text{RSTIN}}$ pin input driver is CMOS. A permanent pull-up is present which is the same as as R_{PU} (see *Table 27 on page 51*)

Subject to general operating conditions for V_{33} and T_A unless otherwise specified.

Table 29. $\overline{\text{RESET}}$ pin characteristics

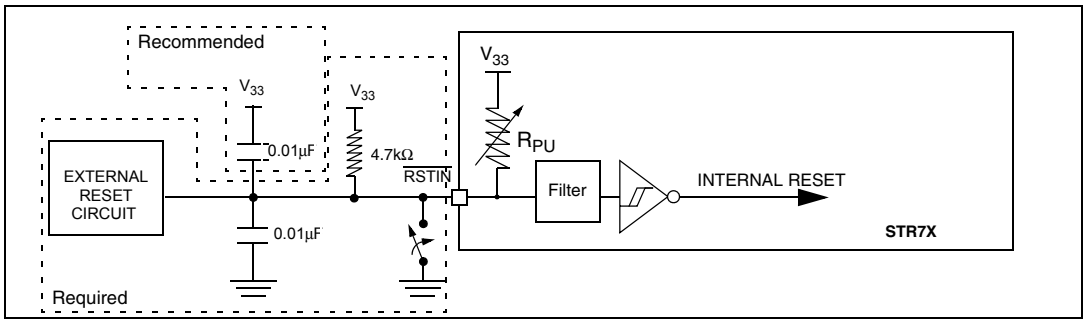
Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$V_{IL(RSTINn)}$	$\overline{\text{RSTIN}}$ Input low level voltage [1]				0.8	V
$V_{IH(RSTINn)}$	$\overline{\text{RSTIN}}$ Input high level voltage [1]		2			
$V_{F(RSTINn)}$	$\overline{\text{RSTIN}}$ Input filtered pulse[2]				500	ns
$V_{NF(RSTINn)}$	$\overline{\text{RSTIN}}$ Input not filtered pulse[2]		1.2			µs

Notes:

1. Data based on characterization results, not tested in production.

2) Data guaranteed by design, not tested in production.

Figure 24. Recommended $\overline{\text{RSTIN}}$ pin protection.[1]



Notes:

1. The R_{PU} pull-up equivalent resistor is based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 18*).
2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the $\overline{\text{RSTIN}}$ pin can go below the $V_{IL(RSTINn)}$ max. level specified in *Table 29*. Otherwise the reset will not be taken into account internally.

4.3.6 TIM timer characteristics

Subject to general operating conditions for V_{33}, f_{MCLK}, and T_A unless otherwise specified.

Refer to *Section 4.3.5: I/O port pin characteristics on page 51* for more details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output...).

Table 30. TIM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time		2			t_{CK_TIM}
$t_{res(TIM)}$	Timer resolution time		1			t_{PCLK2}
		f_{PCLK2} = 30 MHz	33.3			ns
f_{EXT}	Timer external clock frequency	$f_{CK\_TIM(MAX)} = f_{MCLK}$	0		$f_{CK\_TIM}/4$	MHz
		$f_{CK\_TIM} = f_{MCLK}$ = 60 MHz	0		15	MHz
Res_{TIM}	Timer resolution				16	bit
$t_{COUNTER}$	16-bit Counter clock period when internal clock is selected		1		65536	t_{PCLK2}
		f_{PCLK2} = 30 MHz	0.033		2184	µs
T_{MAX_COUNT}	Maximum Possible Count				65536x 65536	t_{PCLK}
		f_{PCLK2} = 30 MHz			143.1	s

4.3.7 EMI - external memory interface

Subject to general operating conditions for V_{DD}, f_{HCLK}, and T_A unless otherwise specified.

The tables below use a variable which is derived from the EMI_BCONn registers (described in the STR71x Reference Manual) and represents the special characteristics of the programmed memory cycle.

Table 31. EMI general characteristics

Symbol	Parameter	Value
t_{MCLK}	CPU clock period	1 / f_{MCLK}
t_C	Memory cycle time wait states	t_{MCLK} x (1 + [C_LENGTH])

Figure 31. Write cycle timing: 16-bit write on 8-bit memory

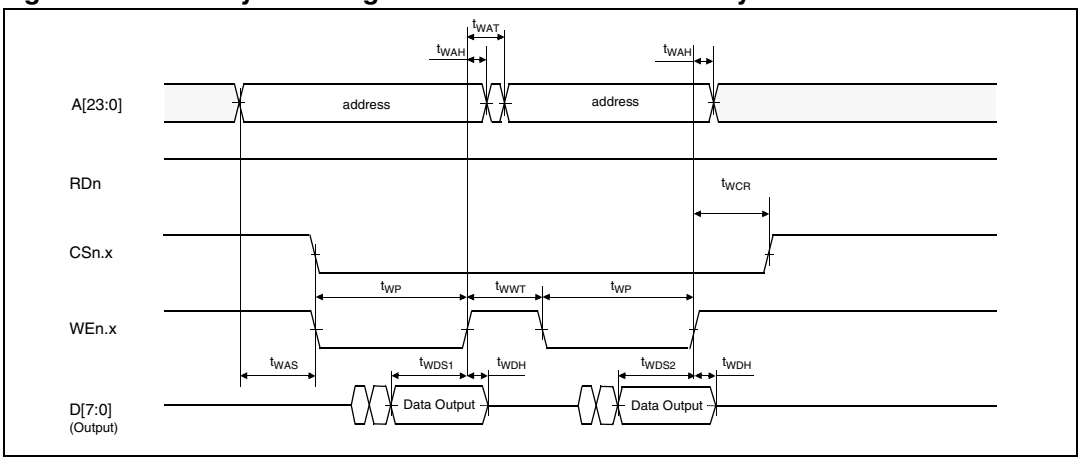
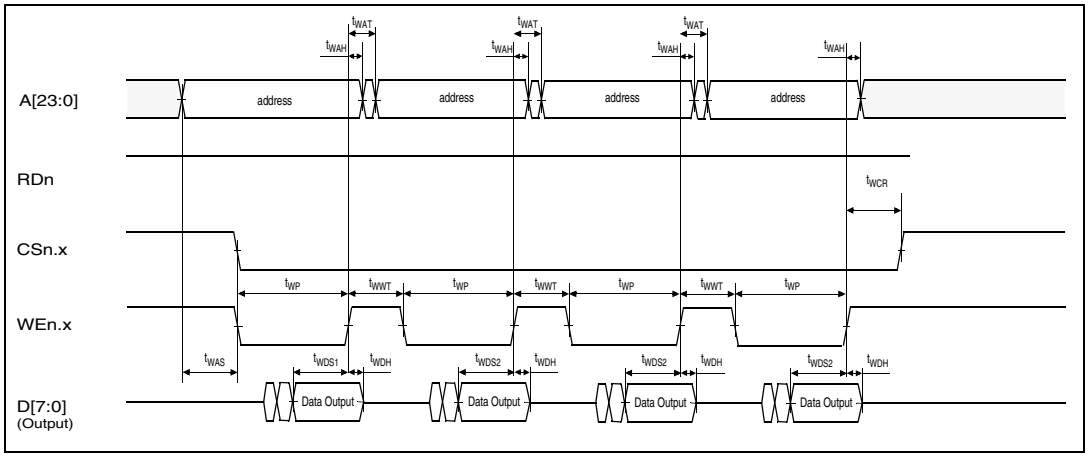


Figure 32. Write cycle timing: 32-bit write on 8-bit memory



See *Table 33* for write timing data.

4.3.8 I²C - inter IC control interface

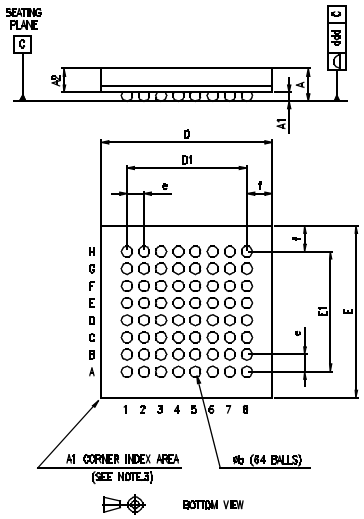
Subject to general operating conditions for V_{33}, f_{PCLK1}, and T_A unless otherwise specified.

The STR7 I²C interface meets the requirements of the Standard I²C communications protocol described in the following table with the restriction mentioned below:

Note: ***Restriction:*** *The I/O pins which SDA and SCL are mapped to are not "True" Open-Drain: when configured as open-drain, the PMOS connected between the I/O pin and V_{33} is disabled, but it is still present. Also, there is a protection diode between the I/O pin and V_{33}. Consequently, when using this I²C in a multi-master network, it is not possible to power off the STR7X while some another I²C master node remains powered on: otherwise, the STR7X will be powered by the protection diode.*

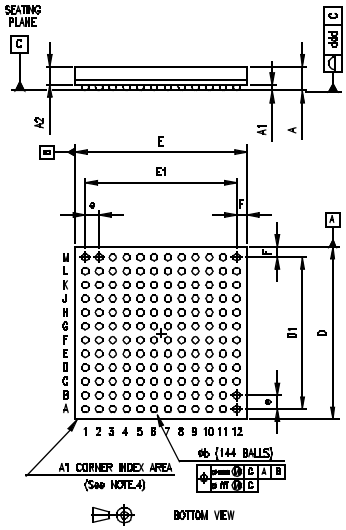
Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Figure 42. 64-Low profile fine pitch ball grid array package



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	1.210		1.700	0.048		0.067
A1	0.270			0.011		
A2		1.120			0.044	
b	0.450	0.500	0.550	0.018	0.020	0.022
D	7.750	8.000	8.150	0.305	0.315	0.321
D1		5.600			0.220	
E	7.750	8.000	8.150	0.305	0.315	0.321
E1		5.600			0.220	
e	0.720	0.800	0.880	0.028	0.031	0.035
f	1.050	1.200	1.350	0.041	0.047	0.053
ddd			0.120			0.005
	Number of Pins					
N	64					

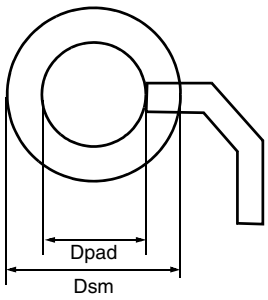
Figure 43. 144-low profile fine pitch ball grid array package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	1.21		1.70	0.0476		0.0669
A1	0.21			0.0083		
A2		1.085			0.0427	
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
D	9.85	10.00	10.15	0.3878	0.3937	0.3996
D1		8.80			0.3465	
E	9.85	10.00	10.15	0.3878	0.3937	0.3996
E1		8.80			0.3465	
e		0.80			0.0315	
F		0.60			0.0236	
ddd			0.10			0.0039
eee			0.15			0.0059
fff			0.08			0.0031
	Number of Pins					
N	144					

[1]Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. Recommended PCB design rules (0.80/0.75mm pitch BGA)



Dpad	0.37 mm
Dsm	0.52 mm typ. (depends on solder mask registration tolerance
Solder paste	0.37 mm aperture diameter
– Non solder mask defined pads are recommended – 4 to 6 mils screen print	

Figure 47. BGA144 STR710 version “Z”

Figure 48. BGA64 STR711 version “X”

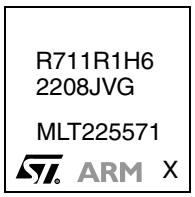


Table 43. A, Z and X version differences

Feature	A version	Z version	X version
ARM7TDMI core device Identification (ID) code register (see ARM7TDMI Technical Reference Manual)	Version bits [31:28] = 0001	Version bits [31:28] = 0010	Version bits [31:28] = 0010
Low power mode consumption in STOP mode at 25 °C	Not guaranteed Typical 49 µA	50 µA maximum at 25°C. Less than 30 µA at 25 °C for 99.730020% of parts	Same as Z.
SC.DATA pin	Not TRUE open drain When addressing 5V cards, the SCDATA Line must be connected to an open drain buffer.		Pin P0.10/U1.RX/U1.TX/SC.DATA has been modified to offer TRUE OPEN DRAIN functionality when in Smartcard mode. When addressing 5V cards, the SCDATA line can now be connected directly to the card I/O. This modification is backward compatible with previous designs, and no board modification is required.

8 Known limitations

Description

If an IRQ or FIQ interrupt is pending and the Interrupt vector register (EIC_IVR) is not yet read, the HALT bit in the RCCU_SMR register can not be written. Therefore a software reset can not be generated.

Workaround

To generate a software reset when an IRQ or FIQ line is pending, either:

- reset the EIC peripheral by setting bit 14 in the APB2_SWRES register, or
- read the EIC_IVR register prior to generating a software reset.

Table 44. Document revision history (continued)

Date	Revision	Changes
22-May-2006	8	Added Flashless device. Changed reset state of pins P1.10 and P1.13 from pu to pd, P0.15 from pu to floating and removed x in interrupt column for P1.15 and P1.12 in *Table 4* and *Table 5* Added notes under *Table 4* on EMI pin reset state. Corrected inch value for d3 in *Figure 40* Added footprint diagrams in *Figure 40* and *Figure 43* Updated *Section 4: Electrical parameters*
01-Aug-2006	9	Flash data retention changed to 20 years at 85° C. Changed note 8 on page 19 Changed note 1 on page 45
06-Nov-2006	10	Added STR715FR0T1 in *Table 42: Order codes* P0.12 corrected in *Table 5 on page 25*
20-Mar-2007	11	Added characteristics of *BSPI - buffered serial peripheral interface on page 63* Updated *Table 21: Low-power mode wakeup timing on page 46*
13-Feb-2008	12	Updated ordering information Updated USB characteristics Updated external clock characteristics
03-Apr-2013	13	Updated title (to be in line with the “device summary” table) Updated ST Logo and Disclaimer Added *Section 8: Known limitations*