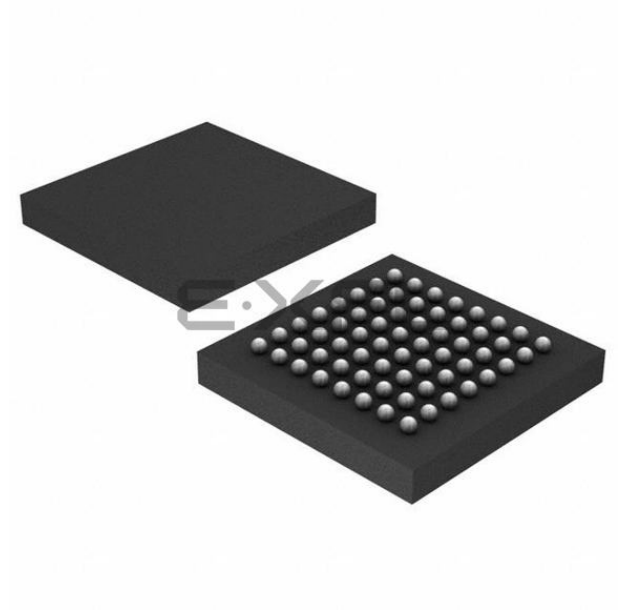

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, HDLC, I²C, SmartCard, SPI, UART/USART, USB
Peripherals	PWM, WDT
Number of I/O	48
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str710rzh6

List of tables

Figure 1. STR71x block diagram

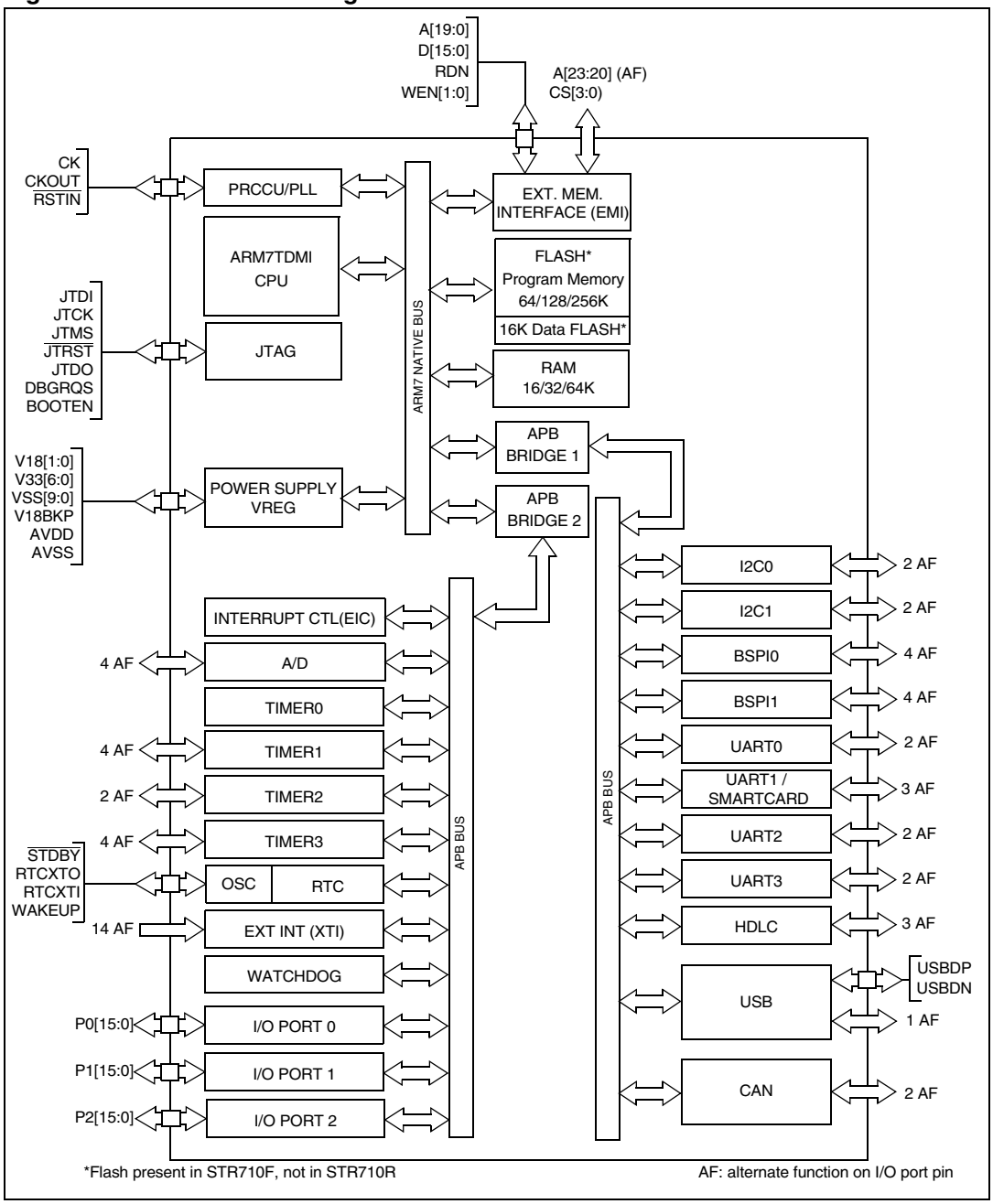


Table 3. STR710 BGA ball connections

	A	B	C	D	E	F	G	H	J	K	L	M
1	P0.10	P2.0	P2.1	VSS	P2.2	P2.6	BOOT EN	P2.12	P2.13	P2.15	JTDI	N.C.
2	VSS	RDn	P0.11	V33	P2.3	P2.8	P2.9	JTMS	JTRSTn	TEST	TEST	N.C.
3	V33	P0.9	P0.12	P0.13	P2.4	N.C.	P2.10	JTCK	NU	V33	N.C.	DBG RQS
4	P0.6	P0.7	P0.8	P0.14	P2.5	N.C.	P2.11	JTDO	CK	CKOUT	VSSIO-PLL	N.C.
5	A.19	WEn.1	WEn.0	P0.5	P2.7	VSS	P2.14	N.C.	RTCX-TO	RTCXTI	N.C.	P0.15
6	P0.3	A.15	A.16	A.17	A.18	V33	V18	N.C.	N.C.	V18BKP	VSS BKP	$\overline{\text{STDBY}}$
7	P0.2	P0.1	P0.4	VSS18	V18	A.14	D.12	D.1	D.0	nc	VSS18	$\overline{\text{RSTIN}}$
8	A.9	A.10	A.11	A.13	P0.0	A.0	D.11	P1.12/ CANTX	N.C.	AVSS	D.3	D.2
9	VSS	V33	A.5	A.6	V33	D.15	D.10	P1.8	D.9	P1.0	N.C.	N.C.
10	A.8	N.C.	P1.15	P1.13	VSS	D.14	USBDN	P1.7	D.8	P1.5	P1.1	D.4
11	A.7	N.C.	P1.14	P1.10	A.2	D.13	USBDP	VSS	D.5	P1.4	P1.3	AVDD
12	A.12	A.4	A.3	P1.9	A.1	P1.11/ CANRX	N.C.	V33IO-PLL	P1.6	D.7	D.6	P1.2

Legend / abbreviations for *Table 4*:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: C = CMOS $0.3V_{DD}/0.7V_{DD}$
C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger
T_T= TTL 0.8 V/2 V with input trigger
C/T = Programmable levels: CMOS $0.3V_{DD}/0.7V_{DD}$ or TTL 0.8 V / 2 V

Port and control configuration:

Input: pu/pd= software enabled internal pull-up or pull down
pu= in reset state, the internal 100kΩ weak pull-up is enabled.
pd = in reset state, the internal 100kΩ weak pull-down is enabled.

Output: OD = open drain (logic level)
PP = push-pull
T = true OD, (P-Buffer and protection diode to V_{DD} not implemented), 5 V tolerant.

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
1	A1	P0.10/U1.RX/ U1.TX/ SC.DATA	I/O	pd	C_T	X	4mA	T			Port 0.10	UART1: Receive Data input	UART1: Transmit data output.
												Note: This pin may be used for Smartcard DataIn/DataOut or single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress	
2	B2	$\overline{RD}$	O	5)					X		External Memory Interface: Active low read signal for external memory. It maps to the OE_N input of the external components.		
3	C2	P0.11/BOOT.1 /U1.TX	I/O	pd	C_T		4mA	X	X		Port 0.11	Select Boot Configuration input	UART1: Transmit data output.
4	C3	P0.12/SC.CLK	I/O	pd	C_T		4mA	X	X		Port 0.12	Smartcard reference clock output	
5	D1	V_{SS}	S								Ground voltage for digital I/Os[4]		
6	D2	V_{33}	S								Supply voltage for digital I/Os[4]		
7	B1	P2.0/$\overline{CS}$.0	I/O	8)	C_T		8mA	X	X		Port 2.0	External Memory Interface: Select Memory Bank 0 output **Note:** This pin is forced to output push-pull 1 mode at reset to allow boot from external memory	
8	C1	P2.1/$\overline{CS}$.1	I/O	pu 2)	C_T		8mA	X	X		Port 2.1	External Memory Interface: Select Memory Bank 1 output	
9	D3	P0.13/U2.RX/ T2.OCMPA	I/O	pu	C_T	X	4mA	X	X		Port 0.13	UART2: Receive Data input	Timer2: Output Compare A output
10	D4	P0.14/U2.TX/ T2.ICAPA	I/O	pu	C_T		4mA	X	X		Port 0.14	UART2: Transmit data output	Timer2: Input Capture A input
11	E1	P2.2/$\overline{CS}$.2	I/O	pu 2)	C_T		8mA	X	X		Port 2.2	External Memory Interface: Select Memory Bank 2 output	
12	E2	P2.3/$\overline{CS}$.3	I/O	pu 2)	C_T		8mA	X	X		Port 2.3	External Memory Interface: Select Memory Bank 3 output	

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
143	C4	P0.8/U0.RX/ U0.TX	I/O	pd	C_T	X	4mA	T			Port 0.8	UART0: Receive Data input	UART0: Transmit data output.
											Note: This pin may be used for single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress		
144	B3	P0.9/U0.TX/ BOOT.0	I/O	pd	C_T		4mA	X	X		Port 0.9	Select Boot Configuration input	UART0: Transmit data output

1. The Reset configuration of the I/O Ports is IPUPD (input pull-up/pull down). Refer to *Table 6 on page 30*. The Port bit configuration at reset is PC0=1, PC1=1, PC2=0. The port data register bit (PD) value depends on the pu/pd column which specifies whether the pull-up or pull-down is enabled at reset
2. In reset state, these pins configured as Input PU/PD with weak pull-up enabled. They must be configured by software as Alternate Function (see *Table 6: Port bit configuration table on page 30*) to be used by the External Memory Interface.
3. In reset state, these pins configured as Input PU/PD with weak pull-down enabled to output Address 0x0000 0000 using the External Memory Interface. To access memory banks greater than 1Mbyte, they need to be configured by software as Alternate Function (see *Table 6: Port bit configuration table on page 30*).
4. $V_{33IO\text{-}PLL}$ and V_{33} are internally connected. $V_{SSIO\text{-}PLL}$ and V_{SS} are internally connected.
5. During the reset phase, these pins are in input pull-up state. When reset is released, they are configured as Output Push-Pull.
6. During the reset phase, these pins are in input pull-up state. When reset is released, they are configured as Hi-Z.
7. During the reset phase, these pins are in input pull-down state. When reset is released, they are configured as Output Push-Pull.
8. During the reset phase, this pin is in input floating state. When reset is released, it is configured as Output Push-Pull.

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1)]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
20	P0.15/ WAKEUP	I		T_T	X				X	Port 0.15	Wakeup from Standby mode input.	
										Note: This port is input only.		
21	RTCXTI									Realtime Clock input and input of 32 kHz oscillator amplifier circuit		
22	RTCXTO									Output of 32 kHz oscillator amplifier circuit		
23	$\overline{STDBY}$	I/O		C_T		4mA	X		X	Input: Hardware Standby mode entry input active low. **Caution:** External pull-up to V_{33} required to select normal mode. Output: Standby mode active low output following Software Standby mode entry. **Note**: In Standby mode all pins are in high impedance except those marked Active in Stdby.		
24	$\overline{RSTIN}$	I		C_T					X	Reset input		
25	V_{SSBKP}			S					X	Stabilization for low power voltage regulator.		
26	V_{18BKP}			S					X	Stabilization for low power voltage regulator. Requires external capacitors of at least 1µF between V_{18BKP} and $V_{SS18BKP}$. See *Figure 5*. **Note:** If the low power voltage regulator is bypassed, this pin can be connected to an external 1.8V supply.		
27	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
28	V_{SS18}	S								Stabilization for main voltage regulator.		
29	V_{DDA}	S								Supply voltage for A/D Converter		
30	V_{SSA}	S								Ground voltage for A/D Converter		
31	P1.0/T3.OCMPB/AIN.0	I/O	pu	C_T		4mA	X	X		Port 1.0	Timer 3: Output Compare B	ADC: Analog input 0
32	P1.1/T3.ICAPA/T3.EXTCLK/AIN.1	I/O	pu	C_T		4mA	X	X		Port 1.1	Timer 3: Input Capture A or External Clock input	ADC: Analog input 1
33	P1.2/T3.OCMPA/AIN.2	I/O	pu	C_T		4mA	X	X		Port 1.2	Timer 3: Output Compare A	ADC: Analog input 2
34	P1.3/T3.ICAPB/AIN.3	I/O	pu	C_T		4mA	X	X		Port 1.3	Timer 3: Input Capture B	ADC: Analog input 3
35	P1.4/T1.ICAPA/T1.EXTCLK	I/O	pu	C_T		4mA	X	X		Port 1.4	Timer 1: Input Capture A	Timer 1: External Clock input

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
36	P1.5/T1.ICAPB	I/O	pu	C_T		4mA	X	X		Port 1.5	Timer 1: Input Capture B	
37	P1.6/T1.OCMPB	I/O	pu	C_T		4mA	X	X		Port 1.6	Timer 1: Output Compare B	
38	$V_{33IO-PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference[2]		
39	$V_{SSIO-PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[2]		
40	P1.7/T1.OCMPA	I/O	pu	C_T		4mA	X	X		Port 1.7	Timer 1: Output Compare A	
41	P1.8	I/O	pd	C_T		4mA	X	X		Port 1.8		
42	P1.11/CANRX	I/O	pu	C_T	X	4mA	X	X		Port 1.11	CAN: receive data input **Note:** On STR710 and STR712 only	
43	P1.12/CANTX	I/O	pu	C_T		4mA	X	X		Port 1.12	CAN: Transmit data output **Note:** On STR710 and STR712 only	
42	USBDP	I/O		C_T						USB bidirectional data (data +). Reset state = HiZ **Note:** On STR710 and STR711 only This pin requires an external pull-up to V_{33} to maintain a high level.		
43	USBDN	I/O		C_T						USB bidirectional data (data -). Reset state = HiZ **Note:** On STR710 and STR711 only.		
44	V_{SS}	S								Ground voltage for digital I/O circuitry[2]		
45	P1.9	I/O	pd	C_T		4mA	X	X		Port 1.9		
46	P1.10/USBCLK	I/O	pd	C/T		4mA	X	X		Port 1.10	USB: 48 MHZ clock input	
47	P1.13/HCLK/I0.SCL	I/O	pd	C_T	X	4mA	X	X		Port 1.13	HDLC: reference clock input	I2C clock
48	P1.14/HRXD/I0.SDA	I/O	pu	C_T	X	4mA	X	X		Port 1.14	HDLC: Receive data input	I2C serial data
49	P1.15/HTXD	I/O	pu	C_T		4mA	X	X		Port 1.15	HDLC: Transmit data output	
50	V_{SS}	S								Ground voltage for digital I/O circuitry[2]		
51	V_{33}	S								Supply voltage for digital I/O circuitry[2]		

Figure 7. Mapping of Flash memory versions

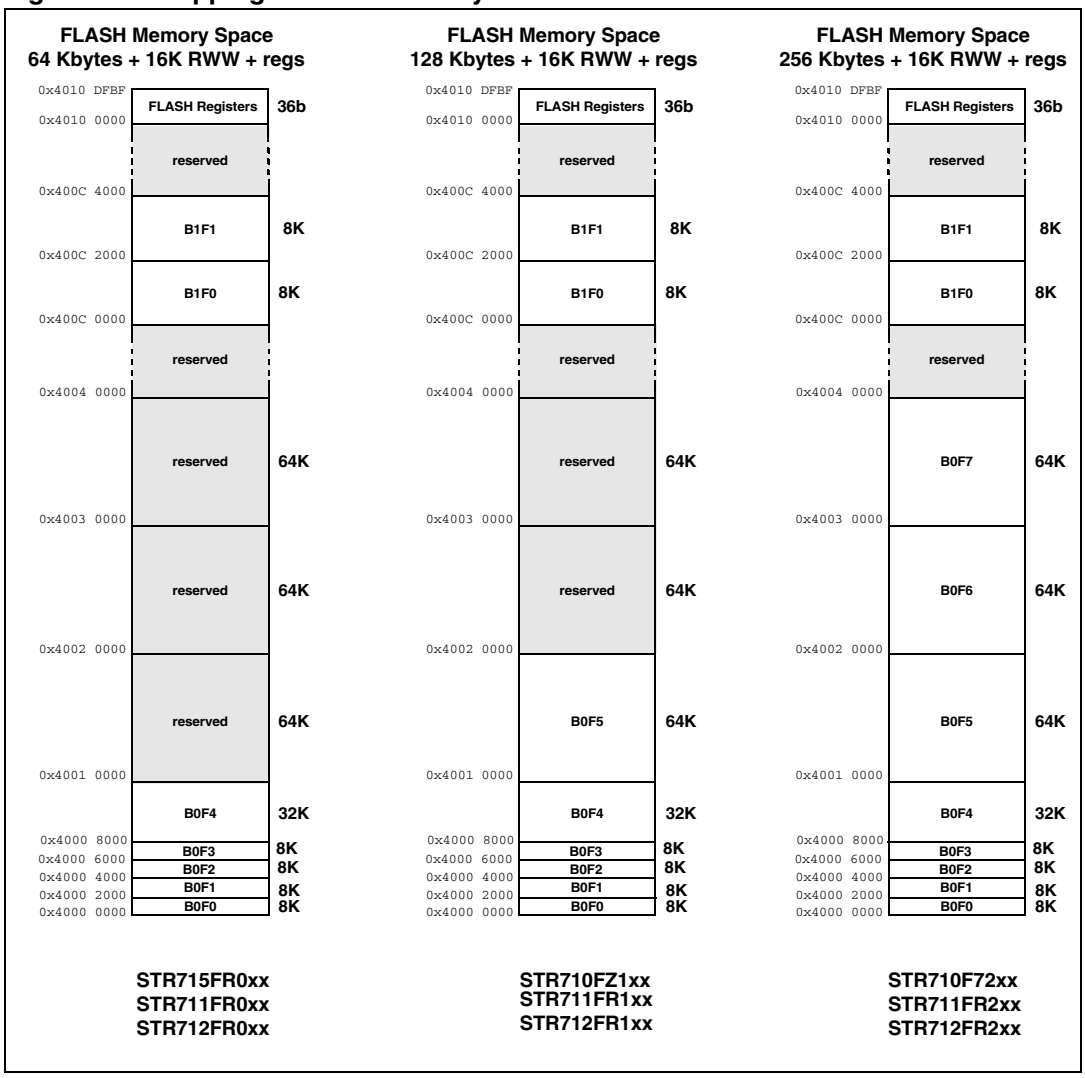


Table 7. RAM memory mapping

Part number	RAM size	Start address	End address
STR715FR0xx STR711FR0xx STR712FR0xx	16 Kbytes	0x2000 0000	0x2000 3FFF
STR710FZ1xx STR711FR1xx STR712FR1xx	32 Kbytes	0x2000 0000	0x2000 7FFF
STR710FR2xx STR710Rxx STR711FR2xx STR712FR2xx	64 Kbytes	0x2000 0000	0x2000 FFFF

4.3 Operating conditions

Subject to general operating conditions for V_{33}, and T_A.

Table 11. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	Internal CPU Clock frequency	Accessing SRAM or external memory with 0 wait states	0	66	MHz
		Accessing FLASH in burst mode	0	50	
		Executing from FLASH with RWW	0	45 [1)]	
		Accessing FLASH with 0 wait states	0	33	
f_{PCLK}	Internal APB Clock frequency		0	33	MHz
V_{33}	Standard Operating Voltage (includes V_{33I0_PLL})		3.0	3.6	V
V_{18BKP}	Backup Operating Voltage		1.4	1.8	V
T_A	Ambient temperature range	6 Partnumber Suffix	-40	85	°C

1. Data guaranteed by characterization, not tested in production

Table 12. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{V33}	V_{33} rise time rate	Subject to general operating conditions for T_A.	20			µs/V
					20	ms/V

Figure 11. STOP I_{DD} vs. V_{33}

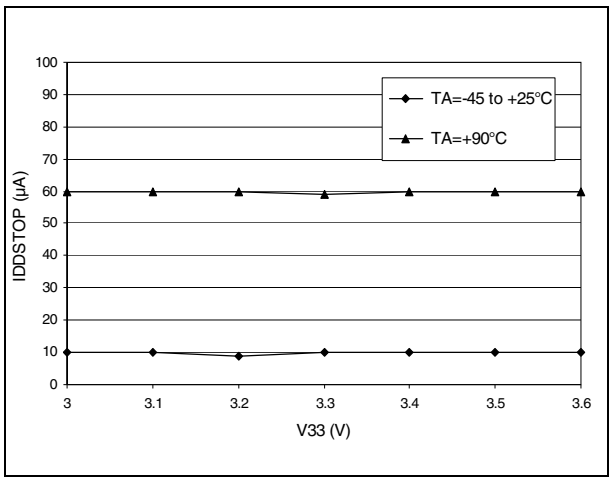


Figure 12. STANDBY I_{DD} vs. V_{33}

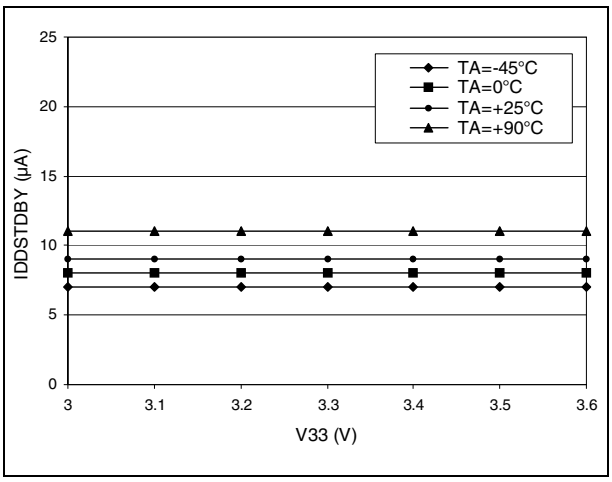
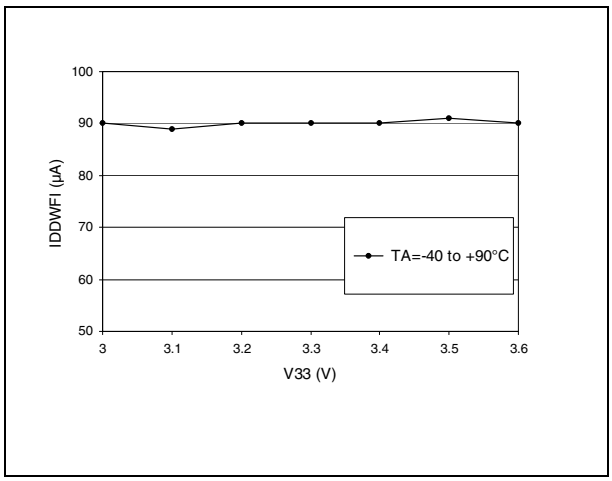


Figure 13. WFI I_{DD} vs. V_{33}



4.3.2 Clock and timing characteristics

External clock sources

Subject to general operating conditions for V_{33}, and T_A.

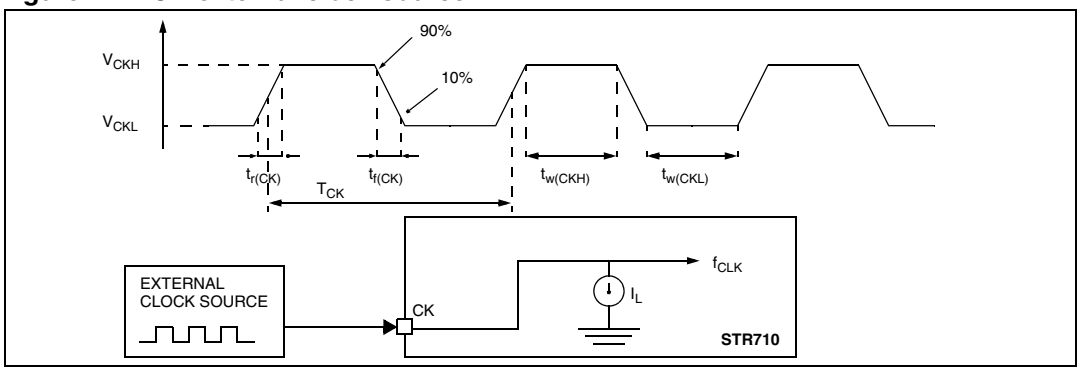
Table 16. CK external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	External clock source frequency		0		16.5	MHz
V_{CKH}	CK input pin high level voltage		$0.7xV_{33}$		V_{33}	V
V_{CKL}	CK input pin low level voltage		V_{SS}		$0.3xV_{33}$	
$t_{w(CK)}$ $t_{w(CK)}$	CK high or low time 1)		25			ns
$t_{r(CK)}$ $t_{f(CK)}$	CK rise or fall time 1)				20	
$C_{IN(CK)}$	CK input capacitance 1)			5		pF
DuCy(XT1)	Duty cycle		40		60	%
I_L	CK Input leakage current	$V_{SS} \leq V_{IN} \leq V_{33}$			±1	µA

Notes:

1. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 14. CK external clock source



OSC32K crystal / ceramic resonator oscillator

The STR7 RTC clock can be supplied with a 32 kHz Crystal/Ceramic resonator oscillators. All the information given in this paragraph are based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 18. 32K oscillator characteristics ($f_{OSC32K=}$ 32.768 kHz)

Symbol	Parameter	Conditions	Typ	Unit
R_F	Feedback resistor		2.7	MΩ
C_{L1} C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)[1)]	R_S=40K Ω	12.5	pF
i_2	RTCXT2 driving current	V_{33}=3.3 V V_{IN}=V_{SS}	3.2	µA
g_m	Oscillator Transconductance		8	µA/V
$t_{SU(OSC32KHZ)}$[2)]	Startup time	V_{33} is stabilized	5	s

Notes:

1. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details
2. $t_{SU(OSC32KHZ)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 32 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 15. Typical application with a 32 kHz crystal

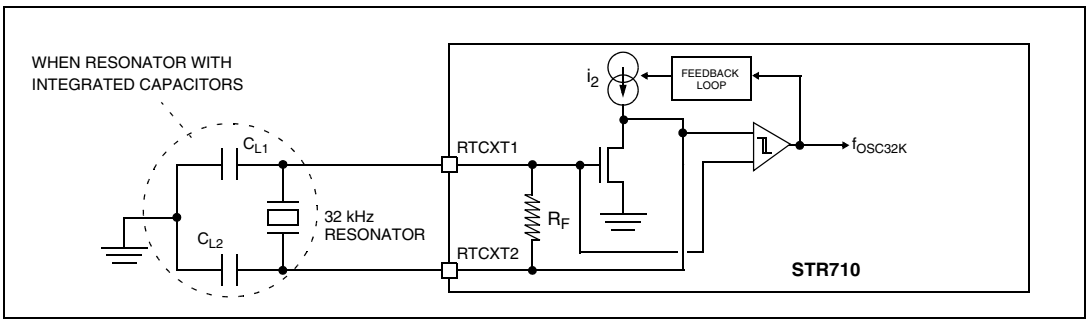


Table 19. PLL1 characteristics (continued)

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$\Delta t_{JITTER1}$	PLL jitter (peak to peak)	t_{PLL} = 4 MHz, MX[1:0]='11' Global Output division = 32 (Output Clock = 2 MHz)		0.7	2	ns

Table 20. PLL2 characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$f_{PLLCLK2}$	PLL multiplier output clock				140	MHz
f_{PLL2}	PLL input clock	FREF_RANGE = 0	1.5		3.0	MHz
		FREF_RANGE = 1	3.0		5	MHz
t_{LOCK2}	PLL lock time	FREF_RANGE = 0 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			300	µs
		FREF_RANGE = 1 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			600	µs
$\Delta t_{JITTER2}$	PLL jitter (peak to peak)	t_{PLL} = 4 MHz, MX[1:0]='11' Global Output division = 32 (Output Clock = 2 MHz)		0.7	2	ns

Table 21. Low-power mode wakeup timing

Symbol	Parameter	Typ	Unit
$t_{WULPWFI}$	Wakeup from LPWFI mode	26(1)	µs
t_{WUSTOP}	Wakeup from STOP mode	2048	CLK Cycles (2)
t_{WUSTBY}	Wakeup from STANDBY mode	2048 CLK Cycles + 8 CLK2 Cycles(3)	Cycles

1. Clock selected is CK2_16, Main VReg OFF and Flash in power-down
2. The CLK clock is derived from the external oscillator.
3. Refer to Figure 7. Reset General Timing in the STR71xF Reference Manual (UM0084)

Figure 22. Typical V_{OL} vs. V_{33}

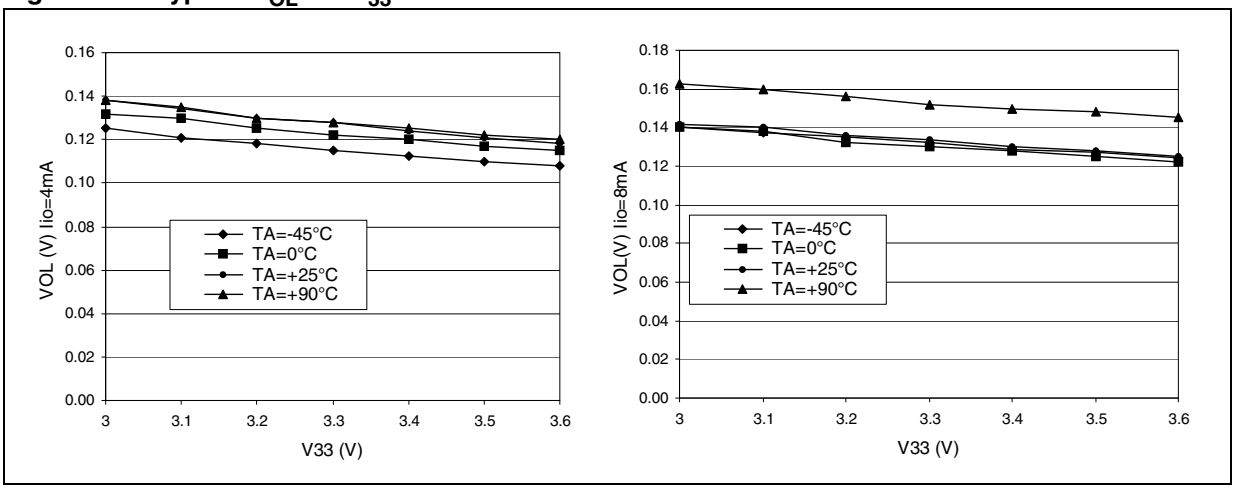


Figure 23. Typical V_{OH} vs. V_{33}

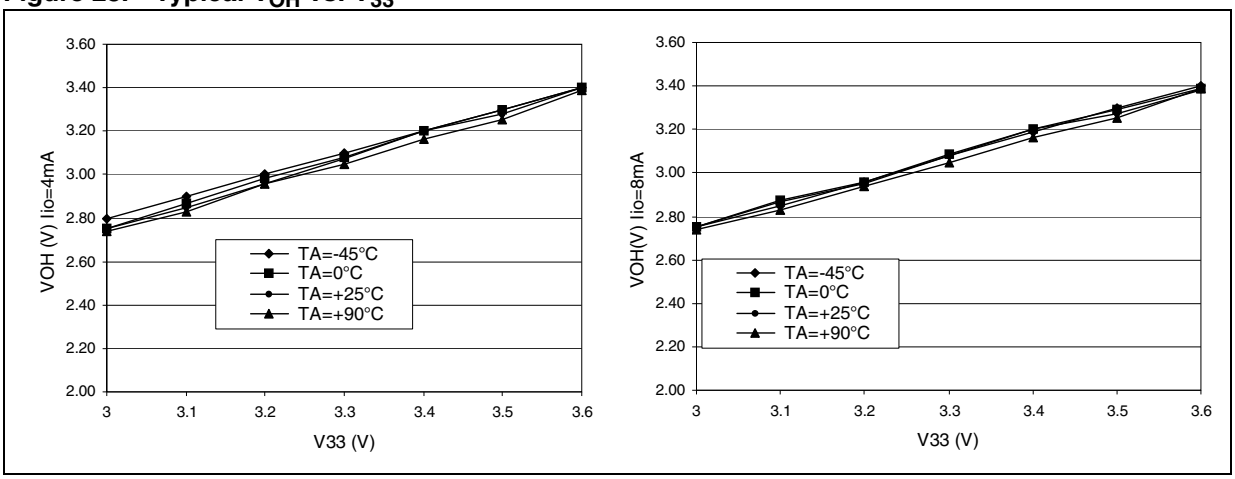


Table 34. I2C characteristics

Symbol	Parameter	Standard mode I^2C		Fast mode I^2C[5]		Unit
		Min [1]	Max [1]	Min [1]	Max [1]	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0 [3]		0 [2]	900 [3]	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	20+0.1C_b	300	
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

Notes:

1. Data based on standard I^2C protocol requirement, not tested in production.
2. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
3. The maximum hold time $t_{h(SDA)}$ is not applicable.
4. Measurement points are done at CMOS levels: $0.3xV_{DD}$ and $0.7xV_{DD}$.
5. f_{PCLK1}, must be at least 8 MHz to achieve max fast I^2C speed (400 kHz).
6. The following table gives the values to be written in the I2CCCR register to obtain the required I^2C SCL line frequency.

4.3.10 USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 37. USB startup time

Symbol	Parameter	Conditions	Max	Unit
$t_{STARTUP}$	USB transceiver startup time		1	µs

Table 38. USB DC characteristics

Symbol	Parameter	Conditions	Min.(1)(2)	Max.(1)(2)	Unit
Input Levels					
V_{DI}	Differential Input Sensitivity	I(DP, DM)	0.2		V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8	2.5	
V_{SE}	Single Ended Receiver Threshold		1.3	2.0	
Output Levels					
V_{OL}	Static Output Level Low	R_L of 1.5 kΩ to 3.6V(3)		0.3	V
V_{OH}	Static Output Level High	R_L of 15 kΩ to V_{SS}(3)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. It is important to be aware that the DP/DM pins are not 5 V tolerant. As a consequence, in case of a a shortcut with Vbus (typ: 5.0V), the protection diodes of the DP/DM pins will be direct biased . This will not damage the device if not more than 50 mA is sunk for longer than 24 hours but the reliability may be affected.
3. R_L is the load connected on the USB drivers

Figure 37. USB: data signal rise and fall time

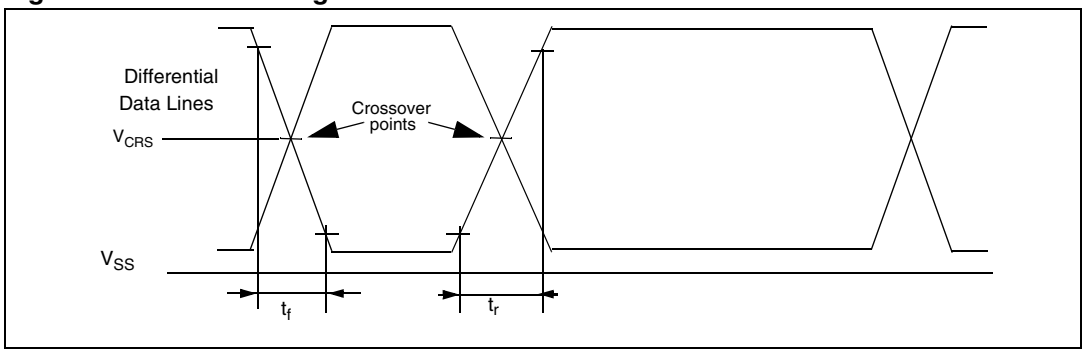


Table 39. USB: Full speed driver electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time(1)	C_L=50 pF	4	20	ns
t_f	Fall Time1)	C_L=50 pF	4	20	ns
t_{rfm}	Rise/ Fall Time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal Crossover Voltage		1.3	2.0	V

1. Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification - Chapter 7 (version 2.0).

Table 41. ADC accuracy with f_{PCLK2} = 20 MHz, f_{ADC}=10 MHz, AV_{DD}=3.3 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ADC_DATA(0V)	Converted code when AIN=0V 1)		2370		2565	Decimal code
ADC_DATA(2.5V)	Converted code when AIN=2.5V 1)		1480		1680	
VCM	Center voltage of Sigma-Delta Modulator1)		1.23	1.25	1.30	V
TUE	Total unadjusted error	In this type of ADC, calibration is necessary to correct gain error and offset errors. Once calibrated, the TUE is limited to the ILE.				
$\lvert E_D \rvert$	Differential linearity error1)			1.96	2.19	LSB
$\lvert E_L \rvert$	Integral linearity error 1)			2.36	3.95	

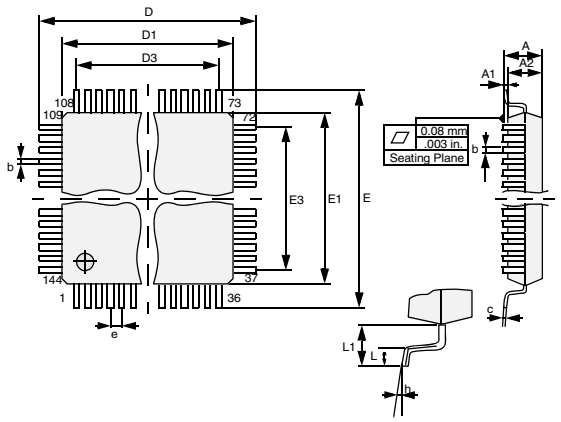
Data are based on characterisation and are not tested in production.

ADC Accuracy vs. Negative Injection Current

Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. The effect of negative injection current on robust pins is specified in *Section 4.3.5*.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 4.3.5* does not affect the ADC accuracy.

Figure 41. 144-Pin low profile quad flat package

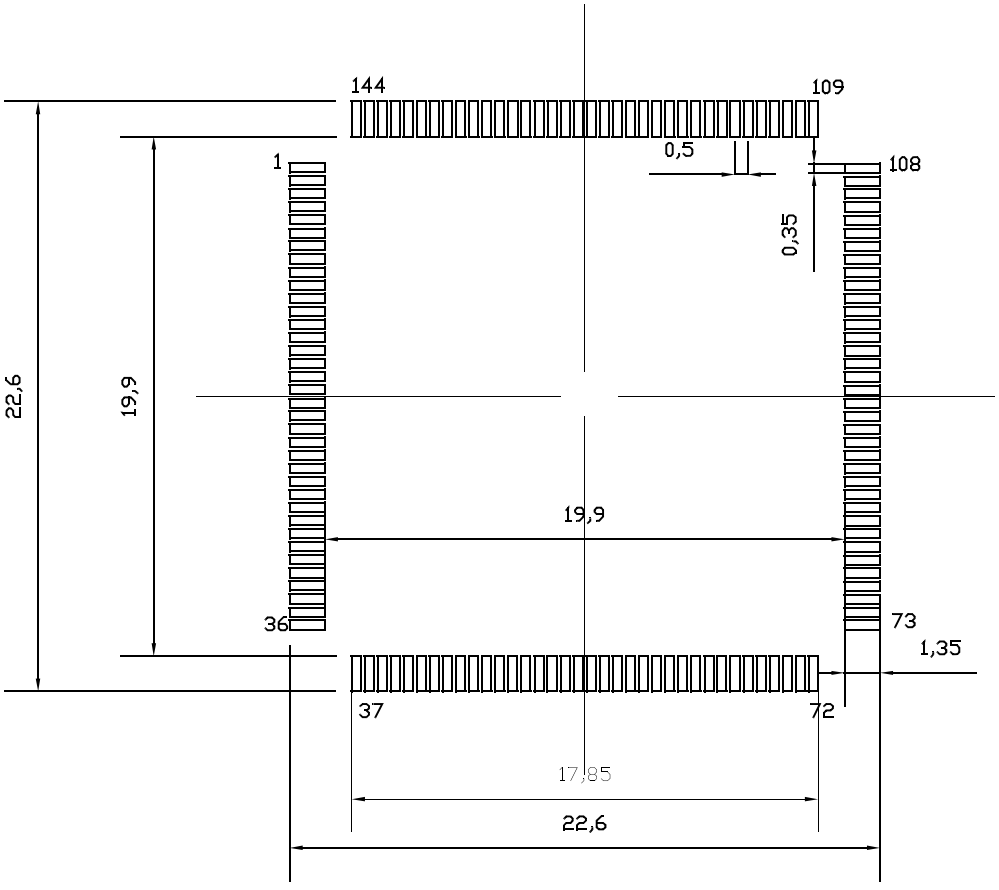


Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053		0.057
b	0.17	0.22	0.27	0.007		0.011
c	0.09		0.20	0.004		0.008
D	21.80	22.00	22.20	0.858	0.867	0.874
D1	19.80	20.00	20.20	0.780	0.787	0.795
D3		17.50			0.689	
E	21.80	22.00	22.20	0.858	0.867	0.874
E1	19.80	20.00	20.20	0.780	0.787	0.795
E3		17.50			0.689	
e		0.50			0.020	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	144					

Jedec Ref. MS-026-BFB

1.Values in inches are converted from mm and rounded to 3 decimal digits.

Recommended footprint (dimensions in mm)



5.2 Thermal characteristics

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

- T_A is the Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the Chip Internal Power.

$P_{I/O}$ represents the Power Dissipation on Input and Output Pins;

Most of the time for the application $P_{I/O} < P_{INT}$ and can be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273°C) \quad (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

where:

K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 42. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal Resistance Junction-Ambient LQFP 144 - 20 x 20 mm / 0.5 mm pitch	42	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LFBGA 144 - 10 x 10 x 1.7mm	50	°C/W

Figure 47. BGA144 STR710 version “Z”

Figure 48. BGA64 STR711 version “X”

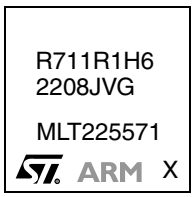


Table 43. A, Z and X version differences

Feature	A version	Z version	X version
ARM7TDMI core device Identification (ID) code register (see ARM7TDMI Technical Reference Manual)	Version bits [31:28] = 0001	Version bits [31:28] = 0010	Version bits [31:28] = 0010
Low power mode consumption in STOP mode at 25 °C	Not guaranteed Typical 49 µA	50 µA maximum at 25°C. Less than 30 µA at 25 °C for 99.730020% of parts	Same as Z.
SC.DATA pin	Not TRUE open drain When addressing 5V cards, the SCDATA Line must be connected to an open drain buffer.		Pin P0.10/U1.RX/U1.TX/SC.DATA has been modified to offer TRUE OPEN DRAIN functionality when in Smartcard mode. When addressing 5V cards, the SCDATA line can now be connected directly to the card I/O. This modification is backward compatible with previous designs, and no board modification is required.