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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, HDLC, I²C, SmartCard, SPI, UART/USART, USB
Peripherals	PWM, WDT
Number of I/O	48
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str710rzt6

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Flexible power management

To minimize power consumption, you can program the STR71x to switch to SLOW, WAIT, LPWAIT (low power wait), STOP or STANDBY mode depending on the current system activity in the application.

Flexible clock control

Two external clock sources can be used, a main clock and a 32 kHz backup clock. The embedded PLL allows the internal system clock (up to 66 MHz) to be generated from a main clock frequency of 16 MHz or less. The PLL output frequency can be programmed using a wide selection of multipliers and dividers. The microcontroller core, APB1 and APB2 peripherals are in separate clock domains and can be programmed to run at different frequencies during application runtime. The clock to each peripheral is gated with an individual control bit to optimize power usage by turning off peripherals any time they are not required.

Voltage regulators

The STR71x requires an external 3.0-3.6V power supply. There are two internal Voltage Regulators for generating the 1.8V power supply for the core and peripherals. The main VR is switched off during low power operation.

Low voltage detectors

Both the Main Voltage Regulator and the Low Power Voltage Regulator contain each a low voltage detection circuitry which keep the device under reset when the corresponding controlled voltage value (V_{18} or V_{18BKP}) falls below 1.35V (+/- 10%). This enhances the security of the system by preventing the MCU from going into an unpredictable state.

An external reset circuit must be used to provide the RESET at V_{33} power-up. It is not sufficient to rely on the RESET generated by the LVD in this case. This is because LVD operation is guaranteed only when V_{33} is within the specification.

3.1 On-chip peripherals

CAN interface (STR710 and STR712)

The CAN module is compliant with the CAN specification V2.0 part B (active). The bit rate can be programmed up to 1 MBaud.

USB interface (STR710 and STR711)

The full-speed USB interface is USB V2.0 compliant and provides up to 16 bidirectional/32 unidirectional endpoints, up to 12 Mb/s (full-speed), support for bulk transfer, isochronous transfers and USB Suspend/Resume functions.

Standard timers

Each of the four timers have a 16-bit free-running counter with 7-bit prescaler

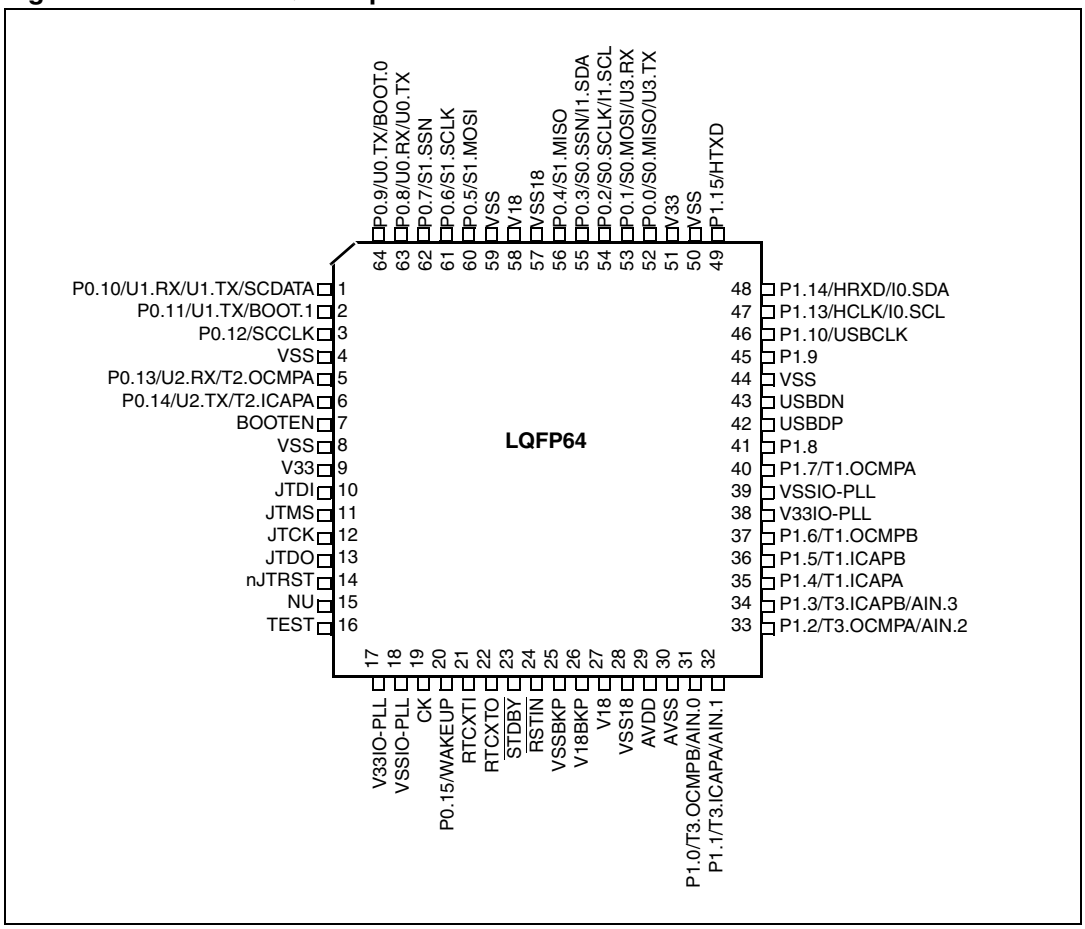
Three timers each provide up to two input capture/output compare functions, a pulse counter function, and a PWM channel with selectable frequency.

The fourth timer is not connected to the I/O ports. It can be used by the application software for general timing functions.

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
107	D10	P1.13/HCLK/ I0.SCL	I/O	pd	C_T	X	4mA	X	X		Port 1.13	HDLC: reference clock input	I2C clock
108	C11	P1.14/HRXD/ I0.SDA	I/O	pu	C_T	X	4mA	X	X		Port 1.14	HDLC: Receive data input	I2C serial data
109	B11	N.C.									Not connected (not bonded)		
110	B10	N.C.									Not connected (not bonded)		
111	C10	P1.15/HTXD	I/O	pu	C_T		4mA	X	X		Port 1.15	HDLC: Transmit data output	
112	A9	V_{SS}	S								Ground voltage for digital I/O circuitry[4]		
113	B9	V_{33}	S								Supply voltage for digital I/O circuitry[4]		
114	C9	A.5	O	[7]			8mA		X		External Memory Interface: address bus		
115	D9	A.6	O	[7]			8mA		X				
116	A11	A.7	O	[7]			8mA		X				
117	A10	A.8	O	[7]			8mA		X				
118	A8	A.9	O	[7]			8mA		X				
119	B8	A.10	O	[7]			8mA		X				
120	C8	A.11	O	[7]			8mA		X				
121	A12	A.12	O	[7]			8mA		X				
122	D8	A.13	O	[7]			8mA		X				
123	E8	P0.0/S0.MISO /U3.TX	I/O	pu	C_T		4mA	X	X		Port 0.0	SPI0 Master in/Slave out data	UART3 Transmit data output
												Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
124	B7	P0.1/S0.MOSI /U3.RX	I/O	pu	C_T	X	4mA	X	X		Port 0.1	BSPI0: Master out/Slave in data	UART3: Receive Data input
												Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	

Figure 4. STR711 LQFP64 pinout



Legend / abbreviations for *Table 5*:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: C = CMOS $0.3V_{DD}/0.7V_{DD}$
C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger
T_T= TTL 0.8V / 2V with input trigger
C/T = Programmable levels: CMOS $0.3V_{DD}/0.7V_{DD}$ or TTL 0.8V / 2V

Port and control configuration:

Input: pu/pd= software enabled internal pull-up or pull down
pu= in reset state, the internal 100kΩ weak pull-up is enabled.
pd = in reset state, the internal 100kΩ weak pull-down is enabled.

Output: OD = open drain (logic level)
PP = push-pull
T = true OD, (P-Buffer and protection diode to V_{DD} not implemented), 5V tolerant.

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n° LQFP64	Pin name	Type	Reset state[1]	Input: Input level	Input: interrupt	Output: Capability	Output: OD	Output: PP	Active in Stdby	Main function (after reset)	Alternate function	
63	P0.8/U0.RX/U0.TX	I/O	pd	C_T	X	4mA	T			Port 0.8	UART0: Receive Data input	UART0: Transmit data output.
										Note: This pin may be used for single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress		
64	P0.9/U0.TX/BOOT.0	I/O	pd	C_T		4mA	X	X		Port 0.9	Select Boot Configuration input	UART0: Transmit data output

1. The Reset configuration of the I/O Ports is IPUPD (input pull-up/pull down). Refer to *Table 6 on page 30*. The Port bit configuration at reset is PC0=1, PC1=1, PC2=0. The port data register bit (PD) value depends on the pu/pd column which specifies whether the pull-up or pull-down is enabled at reset
2. $V_{33IO\text{-}PLL}$ and V_{33} are internally connected. $V_{SSIO\text{-}PLL}$ and V_{SS} are internally connected.

3.5 External connections

Figure 5. Recommended external connection of V_{18} and V_{18BKP} pins

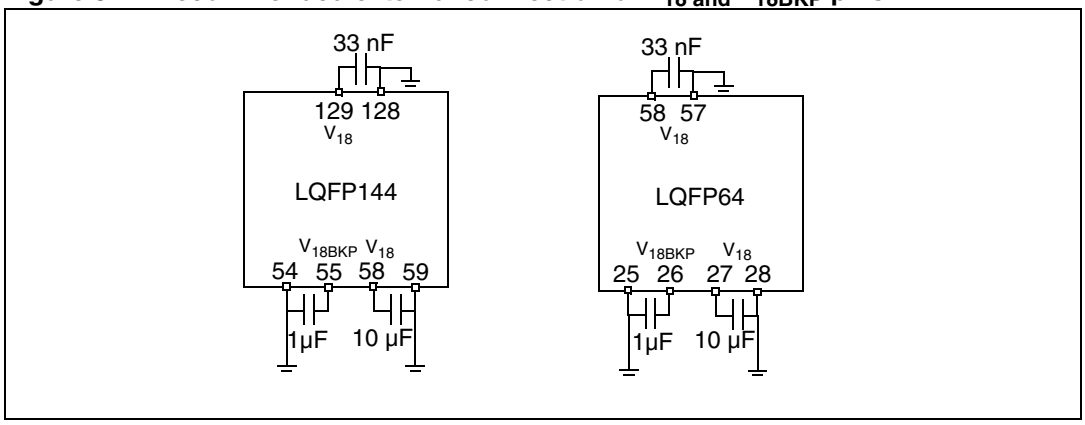
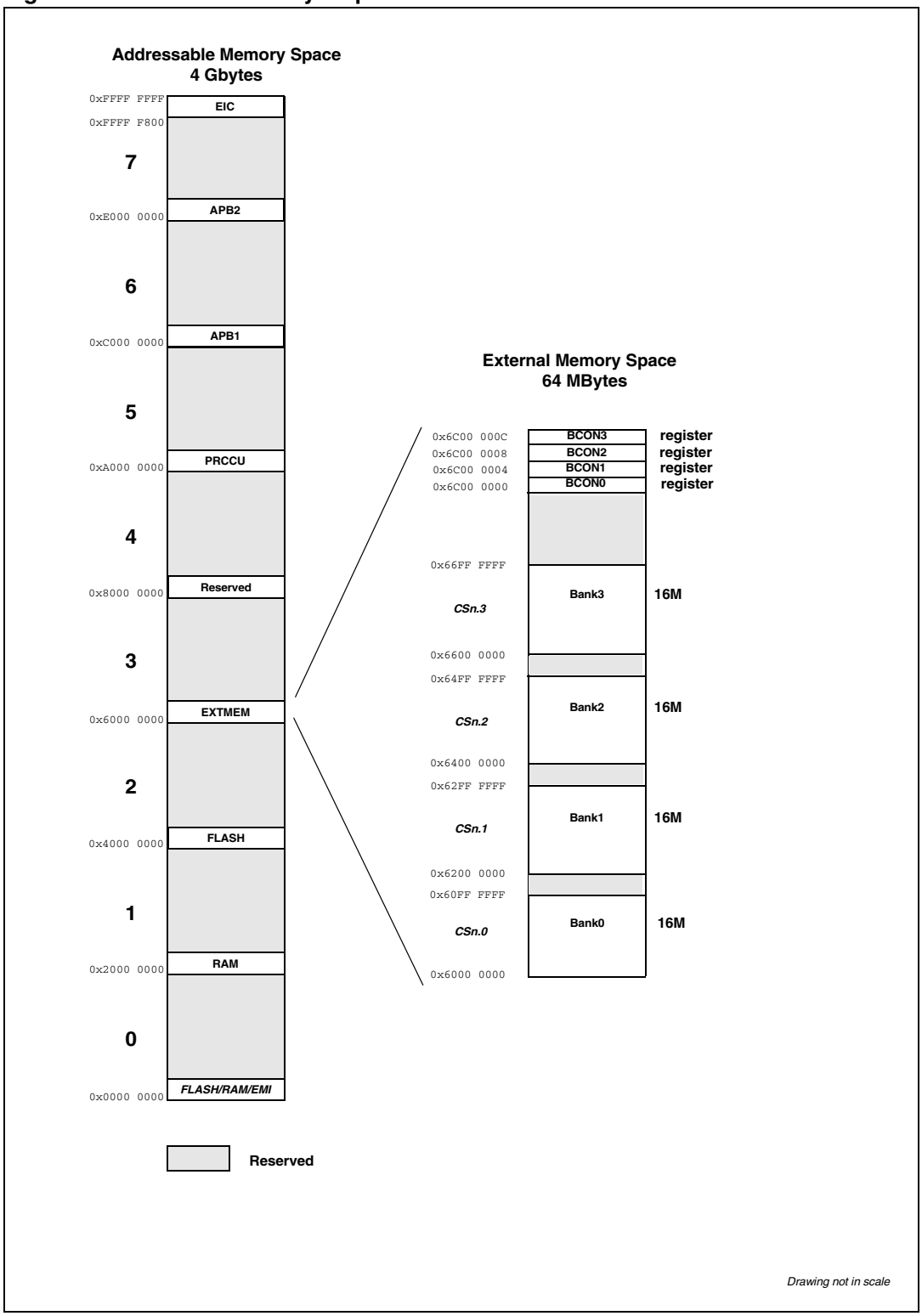


Figure 8. External memory map



4.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{33}- V_{SS}	External 3.3V Supply voltage (including AV_{DD} and $V_{33IO-PLL}$)[2]	-0.3	4.0	V
V_{18BKP} - V_{SSBKP}	Digital 1.8V Supply voltage on V_{18BKP} backup supply [2]	-0.3	2.0	
V_{IN}	Input voltage on true open drain pin (P0.10) [1]	V_{SS}-0.3	+5.5	
	Input voltage on any other pin [1]	V_{SS}-0.3	V_{33}+0.3	
$\|\Delta V_{33x}\|$	Variations between different 3.3V power pins	50	50	mV
$\|\Delta V_{18x}\|$	Variations between different 1.8V power pins [5]	25	25	
$\|V_{SSX}$ - $V_{SS}\|$	Variations between all the different ground pins	50	50	
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	see *: Absolute maximum ratings (electrical sensitivity) on page 49*		
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)			

Table 9. Current characteristics

Symbol	Ratings	Max.	Unit
I_{V33}	Total current into $V_{33}/V_{33IO-PLL}$ power lines (source) [2]	150	mA
I_{VSS}	Total current out of $V_{SS}/V_{SSIO-PLL}$ ground lines (sink) [2]	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$ [1] [3]	Injected current on $\overline{RSTIN}$ pin	± 5	
	Injected current on CK pin	± 5	
	Injected current on any other pin [4]	± 5	
$\Sigma I_{INJ(PIN)}$ [1]	Total injected current (sum of all I/O and control pins) [4]	± 25	

The $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{33}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected. Data based on T_A = 25 °C.

All 3.3V power (V_{33}, AV_{DD}, $V_{33IO-PLL}$) and ground (V_{SS}, AV_{SS}, $V_{SSIO-PLL}$) pins must always be connected to the external 3.3V supply.

Negative injection disturbs the analog performance of the device. See note in *Section 4.3.11: ADC characteristics on page 66*.

When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Only when using external 1.8V power supply. All the power (V_{18}, V_{18BKP}) and ground (V_{SS18}, V_{SSBKP}) pins must always be connected to the external 1.8V supply.

Table 10. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature (see *Section 5.2: Thermal characteristics on page 73*)		

4.3 Operating conditions

Subject to general operating conditions for V_{33}, and T_A.

Table 11. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	Internal CPU Clock frequency	Accessing SRAM or external memory with 0 wait states	0	66	MHz
		Accessing FLASH in burst mode	0	50	
		Executing from FLASH with RWW	0	45 [1)]	
		Accessing FLASH with 0 wait states	0	33	
f_{PCLK}	Internal APB Clock frequency		0	33	MHz
V_{33}	Standard Operating Voltage (includes V_{33I0_PLL})		3.0	3.6	V
V_{18BKP}	Backup Operating Voltage		1.4	1.8	V
T_A	Ambient temperature range	6 Partnumber Suffix	-40	85	°C

1. Data guaranteed by characterization, not tested in production

Table 12. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{V33}	V_{33} rise time rate	Subject to general operating conditions for T_A.	20			µs/V
					20	ms/V

Table 14. Typical power consumption data

Symbol	Parameter		Conditions	Typical current on V33	Unit
I_{DDRUN}	RUN mode current from RAM	All periphs ON	MCLK = 16 MHz, PCLK1 = PCLK2 = 16 MHz	23	mA
			MCLK = 32 MHz, PCLK1 = PCLK2 = 32 MHz	40	
			MCLK = 48 MHz, PCLK1 = PCLK2 = 24 MHz	50	
			MCLK = 64 MHz, PCLK1 = PCLK2 = 32 MHz	63	
		All periphs OFF	MCLK = 16 MHz	16	
			MCLK = 32 MHz	26	
			MCLK = 48 MHz	39	
			MCLK = 64 MHz	48	
	RUN mode current from FLASH	All periphs ON	MCLK = 16 MHz, PCLK1 = PCLK2 = 16 MHz	27	
			MCLK = 32 MHz, PCLK1 = PCLK2 = 32 MHz	47	
			MCLK = 48 MHz, PCLK1 = PCLK2 = 24 MHz	62	
		All periphs OFF	MCLK = 16 MHz	21	
			MCLK = 32 MHz	36	
			MCLK = 48 MHz	53	
I_{DDSLOW}	SLOW mode current		MCLK = CK_AF (32 kHz), MVR off	1.7	
I_{DDWAIT}	WAIT mode current (all periphs ON)		PCLK1 = PCLK2 = 1 MHz	13	
$I_{DDLPWAIT}$	LPWAIT mode current		CK_AF (32 kHz), Main VReg off, FLASH in power-down	37	µA
I_{DDSTOP}	STOP mode current		Main VReg off, FLASH in power down, RTC on	18	
			Main VReg off, FLASH in power down, RTC off	10	
I_{DDSB}	STANDBY mode current		LP VReg on, LVD on, RTC on	10	
			LP VReg off (ext 1.8V on V18BKP), LVD on, RTC on	9	
			LP VReg off (ext1.8V on V18BKP), LVD off, RTC on	5	
			LP VReg off (ext 1.8V on V18BKP), LVD off, RTC off	1	

Figure 11. STOP I_{DD} vs. V_{33}

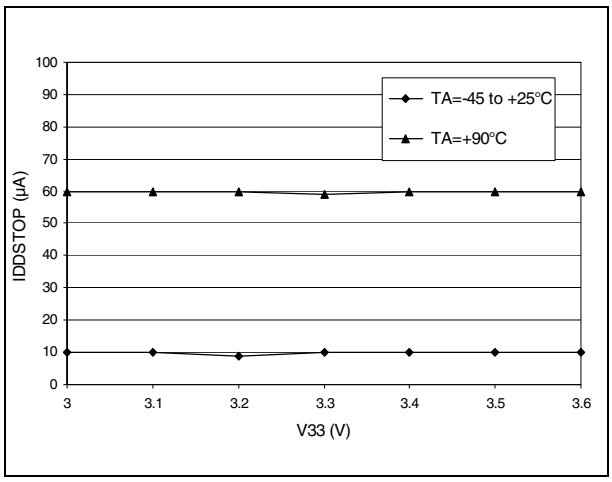


Figure 12. STANDBY I_{DD} vs. V_{33}

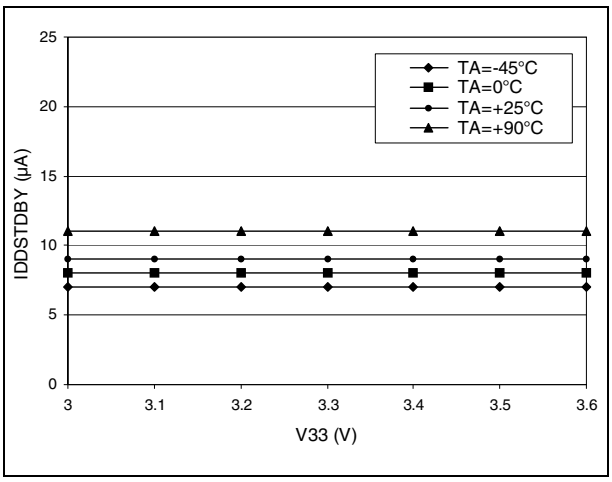
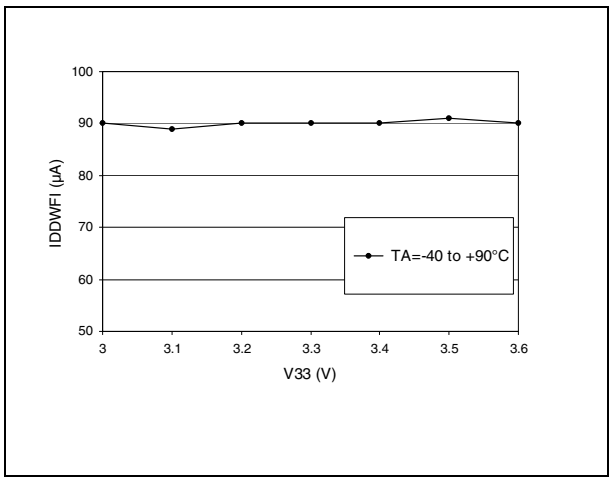


Figure 13. WFI I_{DD} vs. V_{33}



On-chip peripherals

Table 15. Peripheral current consumption

Symbol	Parameter	Conditions	Typ	Unit
$I_{DD(PLL1)}$	PLL1 supply current	T_A= 25°C	3.42	mA
$I_{DD(PLL2)}$	PLL2 supply current		5.81	
$I_{DD(TIM)}$	TIM Timer supply current [1]	T_A= 25°C, f_{PCLK1}= f_{PCLK2}=33 MHz	0.88	
$I_{DD(BSPI)}$	BSPI supply current [2]		1.1	
$I_{DD(UART)}$	UART supply current [2]		1.05	
$I_{DD(I2C)}$	I2C supply current [2]		0.45	
$I_{DD(ADC)}$	ADC supply current when converting [5]		1.89	
$I_{DD(HDLC)}$	HDLC supply current [2]		1.82	
$I_{DD(USB)}$	USB supply current [2]		2.08	
$I_{DD(CAN)}$	CAN supply current [2]		1.11	

Notes:

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16MHz. No IC/OC programmed (no I/O pads toggling).
2. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

4.3.4 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electro magnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

In the case of an ARM7 CPU, in order to write robust code that can withstand all kinds of stress, such as very strong electromagnetic disturbance, it is mandatory that the Data Abort, Prefetch Abort and Undefined Instruction exceptions are managed by the application software. This will prevent the code going into an undefined state or performing any unexpected operation.

Table 23. EMS data

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{33}=3.3 V, T_A=+25°C, f_{MCLK}=32 MHz conforms to IEC 1000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{33}=3.3 V, T_A=+25°C, f_{MCLK}=32 MHz conforms to IEC 1000-4-4	4A

Electro magnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 24. EMI data

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{OSC4M}/f_{HCLK}]		Unit
				16/ 48 MHz	16/8 MHz	
S_{EMI}	Peak level	V_{33}=3.3 V, T_A=+25°C, LQFP64 package conforming to SAE J 1752/3	0.1 MHz to 30 MHz	17	19	dBµV
			30 MHz to 130 MHz	17	16	
			130 MHz to 1 GHz	11	11	
			SAE EMI Level	4	3	-

Notes:

1. Not tested in production.
2. BGA and LQFP devices have similar EMI characteristics.

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electro-static discharge (ESD)

Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard.

Output driving current

Subject to general operating conditions for V_{33} and T_A unless otherwise specified.

Table 28. Output driving current

I/O type	Symbol	Parameter	Conditions	Min	Max	Unit
Standard	V_{OL} 1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO}=+4mA		0.4	V
	V_{OH} 2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-4mA	V_{33}-0.8		
High Current	V_{OL} 1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO}=+8mA		0.4	
	V_{OH} 2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-8mA	V_{33}-0.8		

Notes:

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 9* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 9* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{V33}.

Figure 21. Typical V_{OL} and V_{OH} at V_{33}=3.3V (high current ports)

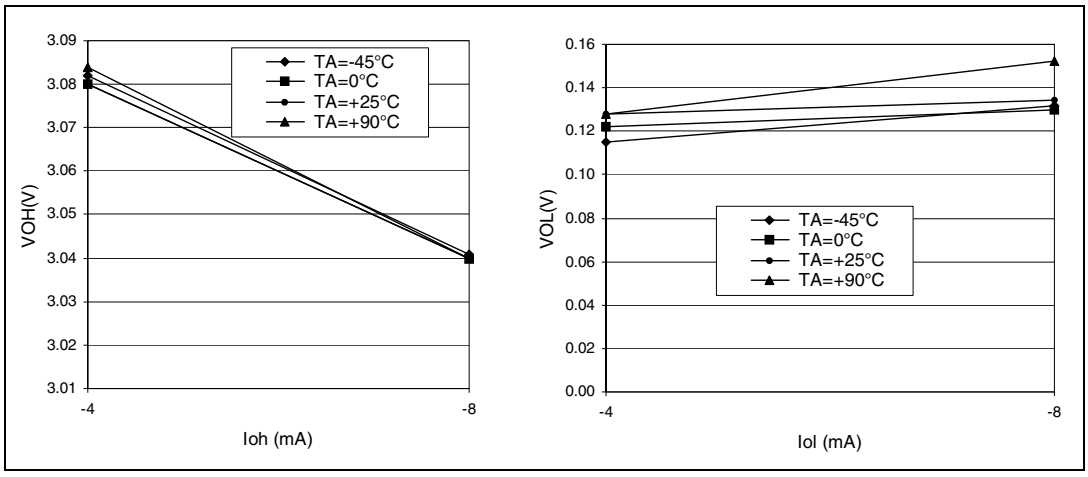
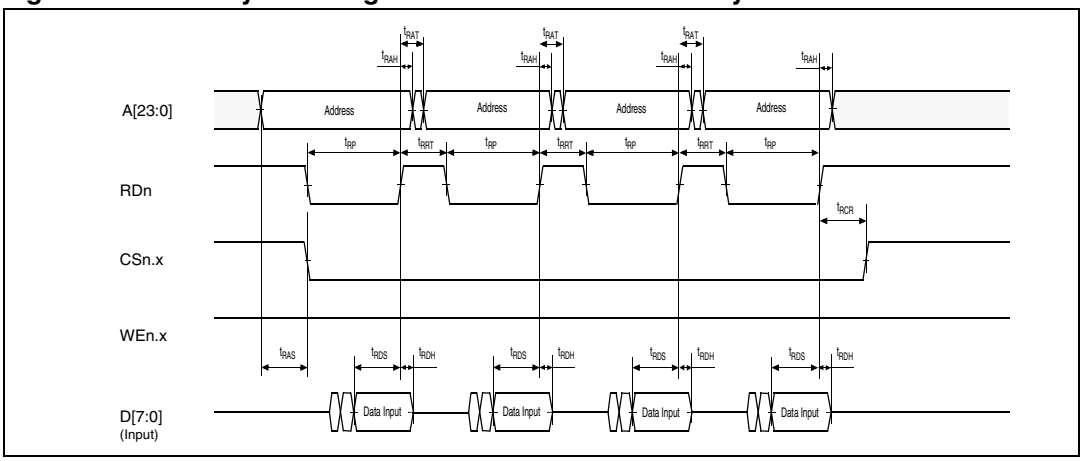


Figure 28. Read cycle timing: 32-bit read on 8-bit memory



See *Table 32* for read timing data.

Figure 29. Write cycle timing: 16-bit write on 16-bit memory

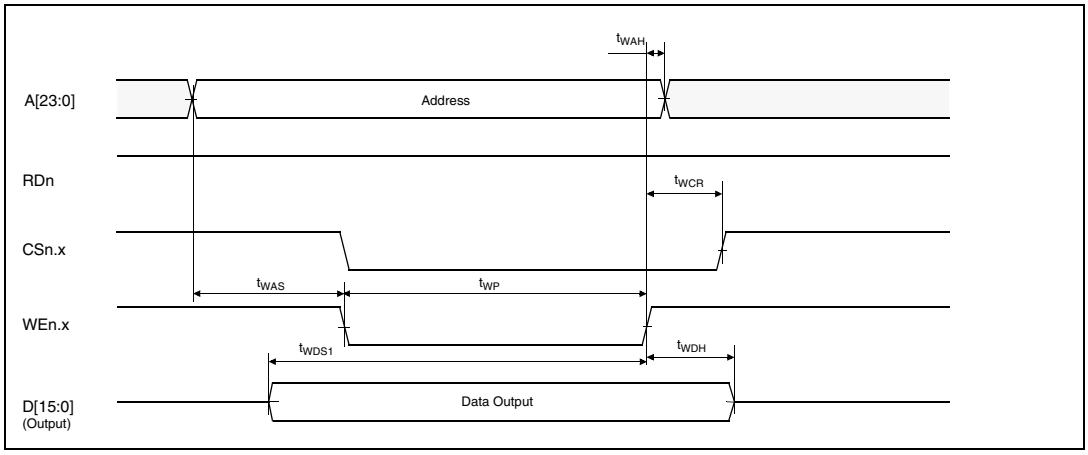
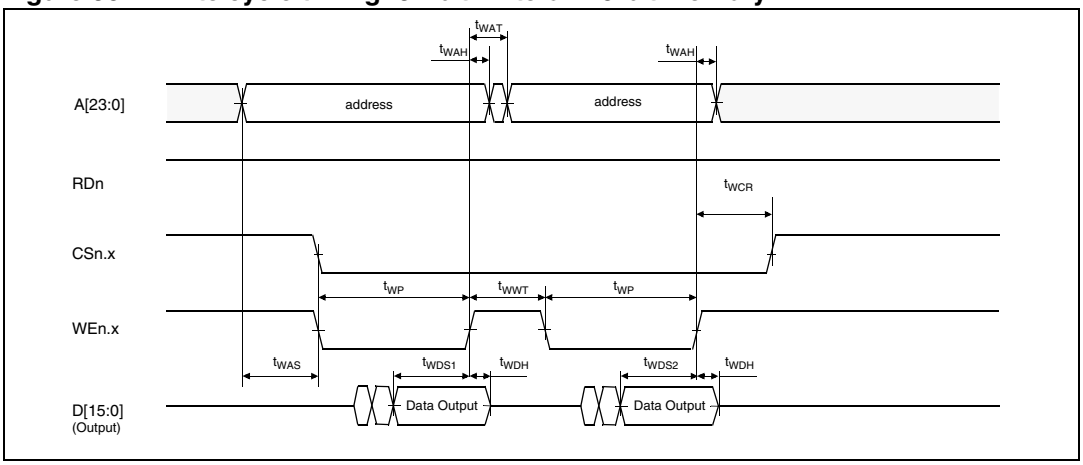


Figure 30. Write cycle timing: 32-bit write on 16-bit memory



See *Table 44* for write timing data.

Figure 33. Typical application with I²C bus and timing diagram

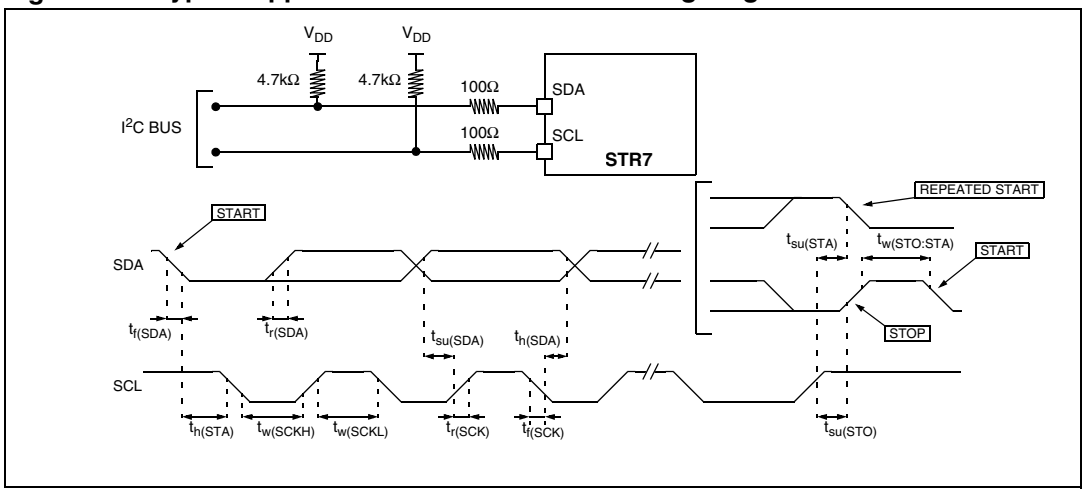


Table 35. SCL Frequency Table (f_{PCLK1}=8 MHz.,V_{33} = 3.3 V)

f_{SCL} (kHz)	I2CCCR Value
	R_P=4.7kΩ
400	83
300	85h
200	8Ah
100	24h
50	4Ch
20	C4h

Legend:

R_P = External pull-up resistance

f_{SCL} = I²C speed

NA = Not achievable

Note: For speeds around 200 kHz, achieved speed can have ± 5% tolerance

For other speed ranges, achieved speed can have ± 2% tolerance

The above variations depend on the accuracy of the external components used.

5.2 Thermal characteristics

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

- T_A is the Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the Chip Internal Power.

$P_{I/O}$ represents the Power Dissipation on Input and Output Pins;

Most of the time for the application $P_{I/O} < P_{INT}$ and can be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273°C) \quad (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

where:

K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 42. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal Resistance Junction-Ambient LQFP 144 - 20 x 20 mm / 0.5 mm pitch	42	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LFBGA 144 - 10 x 10 x 1.7mm	50	°C/W

9 Revision history

Table 44. Document revision history

Date	Revision	Changes
17-Mar-2004	1	First Release
05-Apr-2004	2	Updated “Electrical parameters” on page 34
08-Apr-2004	2.1	Corrected STR712F Pinout. Pins 43/42 swapped.
15-Apr-2004	2.2	PDF hyperlinks corrected.
7-Jul-2004	3	Corrected description of STDBY, V18, VSS18 V18BKP VSSBKP pins Added IDDrun typical data Updated BSPI max. baudrate. Updated “EMI - external memory interface” on page 56
29-Oct-2004	4	Corrected Flash sector B1F0/F1 address in *Figure 6: Memory map on page 31* Corrected *Table 5 on page 25* LQFP64 TEST pin is 16 instead of 17. Added to TQPFP64 column: pin 7 BOOTEN, pin 17 $V_{33IO-PLL}$ Changed description of JTCK from ‘External pull-down required’ to ‘External pull-up or pull down required’.
25-Jan-2005	5	Changed “Product Preview” to “Preliminary Data” on page 1 and 3 Renamed ‘PU/PD’ column to ‘Reset state’ in *Table 5 on page 25* Added reference to STR7 Flash Programming Reference Manual
19-Apr-2005	6	Added STR715F devices and modified RAM size of STR71xF1 devices Added BGA package in *Section 5* Updated ordering information in *Section 7*. Added PLL duty cycle min and max. in *PLL electrical characteristics on page 45*
13-Oct-2005	7	Updated feature description on page 1 Update overview *Section 1.1* Added OD/PP to P0.12 in *Table 5* Changed name of WFI mode to WAIT mode Changed Memory Map *Table 6*: Ext. Memory changed to 64 MB and flash register changed to 36 bytes. Added Power Consumption *Table 13* Modified BGA144 F3, F5, F12 and G12 in *Table 3* and *Table 4* Update EMI Timing *Table 24* and *Figure 29*