Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	HDLC, I²C, SmartCard, SPI, UART/USART, USB
Peripherals	PWM, WDT
Number of I/O	30
Program Memory Size	64KB (64K x 8 + 16K)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str711fr0t6

Realtime clock (RTC)

The RTC provides a set of continuously running counters driven by the 32 kHz external crystal. The RTC can be used as a general timebase or clock/calendar/alarm function. When the STR71x is in Standby mode the RTC can be kept running, powered by the low power voltage regulator and driven by the 32 kHz external crystal.

UARTs

The 4 UARTs allow full duplex, asynchronous, communications with external devices with independently programmable TX and RX baud rates up to 1.25 Mb/s.

Smartcard interface

UART1 is configurable to function either as a general purpose UART or as an asynchronous Smartcard interface as defined by ISO 7816-3. It includes Smartcard clock generation and provides support features for synchronous cards.

Buffered serial peripheral interfaces (BSPI)

Each of the two SPIs allow full duplex, synchronous communications with external devices, master or slave communication at up to 5.5 Mb/s in Master mode and 4 Mb/s in Slave mode.

I^2C interfaces

The two I^2C Interfaces provide multi-master and slave functions, support normal and fast I^2C mode (400 kHz) and 7 or 10-bit addressing modes.

One I^2C Interface is multiplexed with one SPI, so either 2xSPI+1x I^2C or 1xSPI+2x I^2C may be used at a time.

HDLC interface

The High Level Data Link Controller (HDLC) unit supports full duplex operation and NRZ, NRZI, FM0 or MANCHESTER protocols. It has an internal 8-bit baud rate generator.

A/D converter

The Analog to Digital Converter, converts in single channel or up to 4 channels in single-shot or round robin mode. Resolution is 12-bit with a sampling frequency of up to 1 kHz. The input voltage range is 0-2.5V.

Watchdog

The 16-bit Watchdog Timer protects the application against hardware or software failures and ensures recovery by generating a reset.

I/O ports

The 48 I/O ports are programmable as Inputs or Outputs.

External interrupts

Up to 14 external interrupts are available for application use or to wake up the application from STOP mode.

3.2 Related documentation

Available from www.arm.com:

ARM7TDMI Technical reference manual

Available from http://www.st.com:

STR71x Reference manual

STR7 Flash programming manual

AN1774 - STR71x Software development getting started

AN1775 - STR71x Hardware development getting started

AN1776 - STR71x Enhanced interrupt controller

AN1777 - STR71x memory mapping

AN1780 - Real time clock with STR71x

AN1781 - Four 7 segment display drive using the STR71x

The above is a selected list only, a full list STR71x application notes can be viewed at http://www.st.com.

3.3 Pin description for 144-pin packages

Figure 2. STR710 LQFP pinout

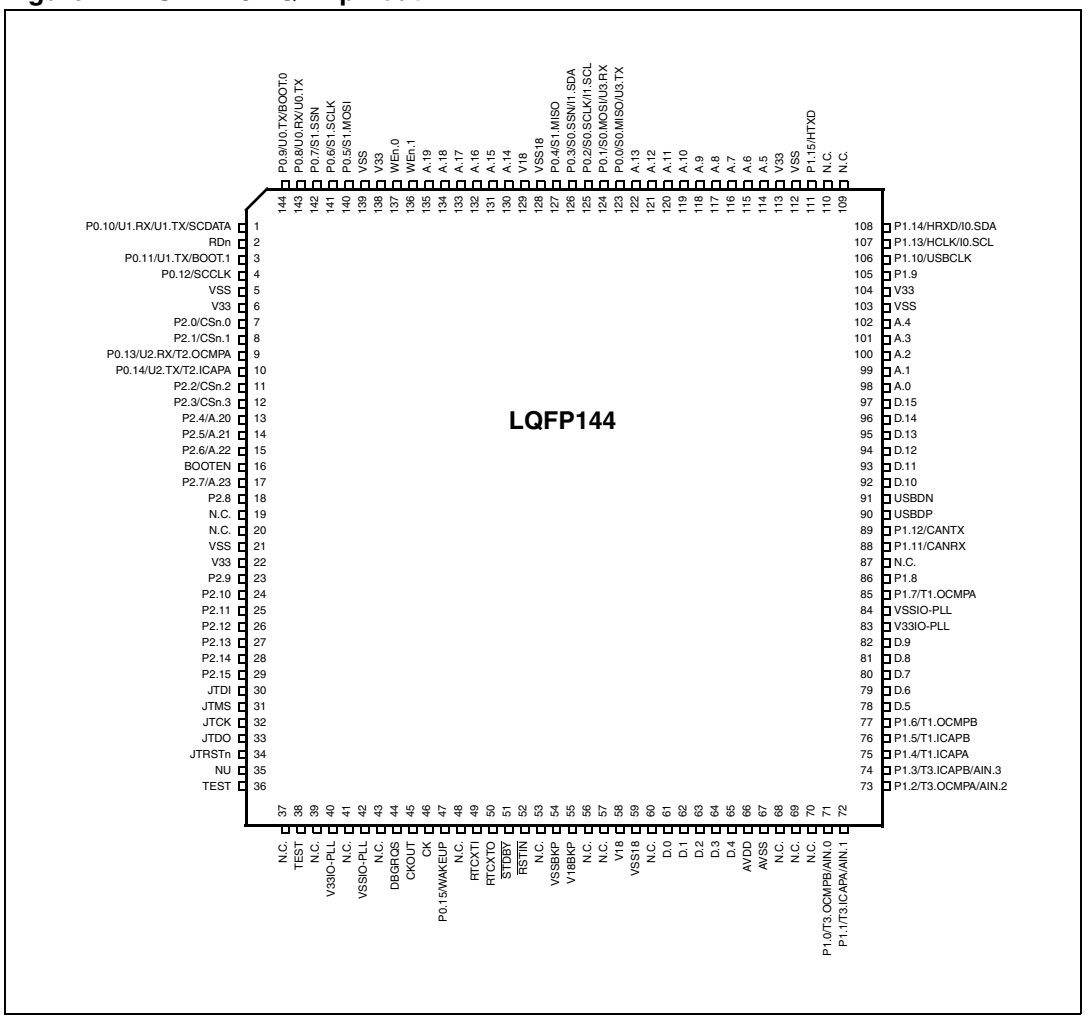


Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP			
13	E3	P2.4/A.20	I/O	pd[3]	C_T		8mA	X	X		Port 2.4	External Memory Interface: address bus
14	E4	P2.5/A.21	I/O	pd[3]	C_T		8mA	X	X		Port 2.5	
15	F1	P2.6/A.22	I/O	pd[3]	C_T		8mA	X	X		Port 2.6	
16	G1	BOOTEN	I		C_T						Boot control input. Enables sampling of BOOT[1:0] pins	
17	E5	P2.7/A.23	I/O	pd[3]	C_T		8mA	X	X		Port 2.7	External Memory Interface: address bus
18	F2	P2.8	I/O	pu	C_T	X	4mA	X	X		Port 2.8	External interrupt INT2
19	F3	N.C.									Not connected (not bonded)	
20	F4	N.C.									Not connected (not bonded)	
21	F5	V_{SS}	S								Ground voltage for digital I/Os[4]	
22	F6	V_{33}	S								Supply voltage for digital I/Os[4]	
23	G2	P2.9	I/O	pu	C_T	X	4mA	X	X		Port 2.9	External interrupt INT3
24	G3	P2.10	I/O	pu	C_T	X	4mA	X	X		Port 2.10	External interrupt INT4
25	G4	P2.11	I/O	pu	C_T	X	4mA	X	X		Port 2.11	External interrupt INT5
26	H1	P2.12	I/O	pu	C_T		4mA	X	X		Port 2.12	
27	J1	P2.13	I/O	pu	C_T		4mA	X	X		Port 2.13	
28	G5	P2.14	I/O	pu	C_T		4mA	X	X		Port 2.14	
29	K1	P2.15	I/O	pu	C_T		4mA	X	X		Port 2.15	
30	L1	JTDI	I		T_T						JTAG Data input. External pull-up required.	
31	H2	JTMS	I		T_T						JTAG Mode Selection Input. External pull-up required.	
32	H3	JTCK	I		C						JTAG Clock Input. External pull-up or pull-down required.	
33	H4	JTDO	O				8mA		X		JTAG Data output. **Note:** Reset state = HiZ.	
34	J2	JTRST	I		T_T						JTAG Reset Input. External pull-up required.	
35	J3	NU									Reserved, must be forced to ground.	
36	K2	TEST									Reserved, must be forced to ground.	
37	M1	N.C.									Not connected (not bonded)	
38	L2	TEST									Reserved, must be forced to ground.	
39	L3	N.C.									Not connected (not bonded)	

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP			
40	K3	$V_{33IO-PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference	
41	M4	N.C.									Not connected (not bonded)	
42	L4	$V_{SSIO-PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[4]	
43	M2	N.C.									Not connected (not bonded)	
44	M3	DBGRQS	I		C_T						Debug Mode request input (active high)	
45	K4	CKOUT	O				8mA		X		Clock output (f_{PCLK2}) **Note:** Enabled by CKDIS register in APB Bridge 2	
46	J4	CK	I		C						Reference clock input	
47	M5	P0.15/ WAKEUP	I		T_T	X				X	Port 0.15	Wakeup from Standby mode input. **Note:** This port is input only.
48	L5	N.C.									Not connected (not bonded)	
49	K5	RTCXTI									Realtime Clock input and input of 32 kHz oscillator amplifier circuit	
50	J5	RTCXTO									Output of 32 kHz oscillator amplifier circuit	
51	M6	$\overline{STDBY}$	I/O		C_T		4mA	X		X	Input: Hardware Standby mode entry input active low. **Caution:** External pull-up to V_{33} required to select normal mode. Output: Standby mode active low output following Software Standby mode entry. **Note**: In Standby mode all pins are in high impedance except those marked Active in Stdby	
52	M7	$\overline{RSTIN}$	I		C_T					X	Reset input	
53	H5	N.C.									Not connected (not bonded)	
54	L6	V_{SSBKP}			S					X	Stabilization for low power voltage regulator.	
55	K6	V_{18BKP}			S					X	Stabilization for low power voltage regulator. Requires external capacitors of at least 1µF between V_{18BKP} and $V_{SS18BKP}$. See *Figure 5*. **Note:** If the low power voltage regulator is bypassed, this pin can be connected to an external 1.8V supply.	
56	J6	N.C.									Not connected (not bonded)	
57	H6	N.C.									Not connected (not bonded)	
58	G6	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.	

Table 4. STR710 pin description

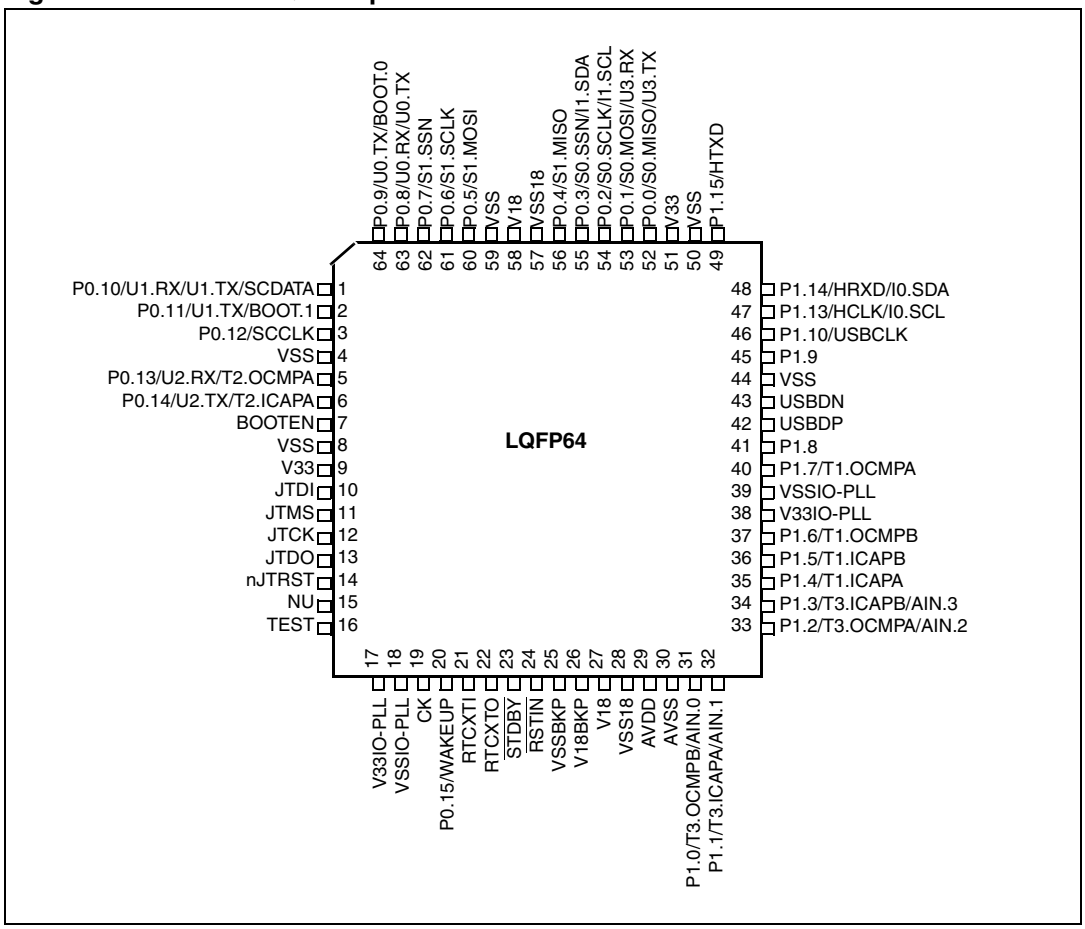
Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
107	D10	P1.13/HCLK/ I0.SCL	I/O	pd	C_T	X	4mA	X	X		Port 1.13	HDLC: reference clock input	I2C clock
108	C11	P1.14/HRXD/ I0.SDA	I/O	pu	C_T	X	4mA	X	X		Port 1.14	HDLC: Receive data input	I2C serial data
109	B11	N.C.									Not connected (not bonded)		
110	B10	N.C.									Not connected (not bonded)		
111	C10	P1.15/HTXD	I/O	pu	C_T		4mA	X	X		Port 1.15	HDLC: Transmit data output	
112	A9	V_{SS}	S								Ground voltage for digital I/O circuitry[4]		
113	B9	V_{33}	S								Supply voltage for digital I/O circuitry[4]		
114	C9	A.5	O	[7]			8mA		X		External Memory Interface: address bus		
115	D9	A.6	O	[7]			8mA		X				
116	A11	A.7	O	[7]			8mA		X				
117	A10	A.8	O	[7]			8mA		X				
118	A8	A.9	O	[7]			8mA		X				
119	B8	A.10	O	[7]			8mA		X				
120	C8	A.11	O	[7]			8mA		X				
121	A12	A.12	O	[7]			8mA		X				
122	D8	A.13	O	[7]			8mA		X				
123	E8	P0.0/S0.MISO /U3.TX	I/O	pu	C_T		4mA	X	X		Port 0.0	SPI0 Master in/Slave out data	UART3 Transmit data output
												Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
124	B7	P0.1/S0.MOSI /U3.RX	I/O	pu	C_T	X	4mA	X	X		Port 0.1	BSPI0: Master out/Slave in data	UART3: Receive Data input
												Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
143	C4	P0.8/U0.RX/ U0.TX	I/O	pd	C_T	X	4mA	T			Port 0.8	UART0: Receive Data input	UART0: Transmit data output.
											Note: This pin may be used for single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress		
144	B3	P0.9/U0.TX/ BOOT.0	I/O	pd	C_T		4mA	X	X		Port 0.9	Select Boot Configuration input	UART0: Transmit data output

1. The Reset configuration of the I/O Ports is IPUPD (input pull-up/pull down). Refer to *Table 6 on page 30*. The Port bit configuration at reset is PC0=1, PC1=1, PC2=0. The port data register bit (PD) value depends on the pu/pd column which specifies whether the pull-up or pull-down is enabled at reset
2. In reset state, these pins configured as Input PU/PD with weak pull-up enabled. They must be configured by software as Alternate Function (see *Table 6: Port bit configuration table on page 30*) to be used by the External Memory Interface.
3. In reset state, these pins configured as Input PU/PD with weak pull-down enabled to output Address 0x0000 0000 using the External Memory Interface. To access memory banks greater than 1Mbyte, they need to be configured by software as Alternate Function (see *Table 6: Port bit configuration table on page 30*).
4. $V_{33IO\text{-}PLL}$ and V_{33} are internally connected. $V_{SSIO\text{-}PLL}$ and V_{SS} are internally connected.
5. During the reset phase, these pins are in input pull-up state. When reset is released, they are configured as Output Push-Pull.
6. During the reset phase, these pins are in input pull-up state. When reset is released, they are configured as Hi-Z.
7. During the reset phase, these pins are in input pull-down state. When reset is released, they are configured as Output Push-Pull.
8. During the reset phase, this pin is in input floating state. When reset is released, it is configured as Output Push-Pull.

Figure 4. STR711 LQFP64 pinout



Legend / abbreviations for *Table 5*:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: C = CMOS $0.3V_{DD}/0.7V_{DD}$
C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger
T_T= TTL 0.8V / 2V with input trigger
C/T = Programmable levels: CMOS $0.3V_{DD}/0.7V_{DD}$ or TTL 0.8V / 2V

Port and control configuration:

Input: pu/pd= software enabled internal pull-up or pull down
pu= in reset state, the internal 100kΩ weak pull-up is enabled.
pd = in reset state, the internal 100kΩ weak pull-down is enabled.

Output: OD = open drain (logic level)
PP = push-pull
T = true OD, (P-Buffer and protection diode to V_{DD} not implemented), 5V tolerant.

4 Electrical parameters

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

4.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25°C and T_A=$T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

4.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25°C, V_{33}=3.3V (for the 3.0V≤V_{33}≤3.6V voltage range) and V_{18}=1.8V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

4.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

4.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

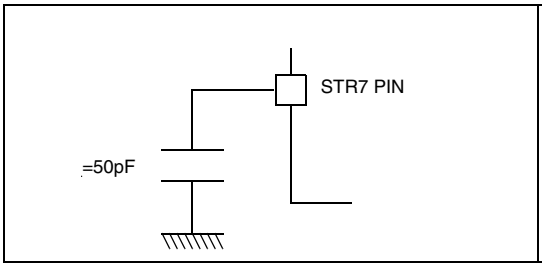
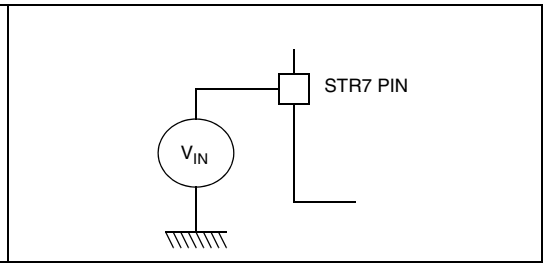


Figure 10. Pin input voltage



4.3.2 Clock and timing characteristics

External clock sources

Subject to general operating conditions for V_{33}, and T_A.

Table 16. CK external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	External clock source frequency		0		16.5	MHz
V_{CKH}	CK input pin high level voltage		$0.7xV_{33}$		V_{33}	V
V_{CKL}	CK input pin low level voltage		V_{SS}		$0.3xV_{33}$	
$t_{w(CK)}$ $t_{w(CK)}$	CK high or low time 1)		25			ns
$t_{r(CK)}$ $t_{f(CK)}$	CK rise or fall time 1)				20	
$C_{IN(CK)}$	CK input capacitance 1)			5		pF
DuCy(XT1)	Duty cycle		40		60	%
I_L	CK Input leakage current	$V_{SS} \leq V_{IN} \leq V_{33}$			±1	µA

Notes:

1. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 14. CK external clock source

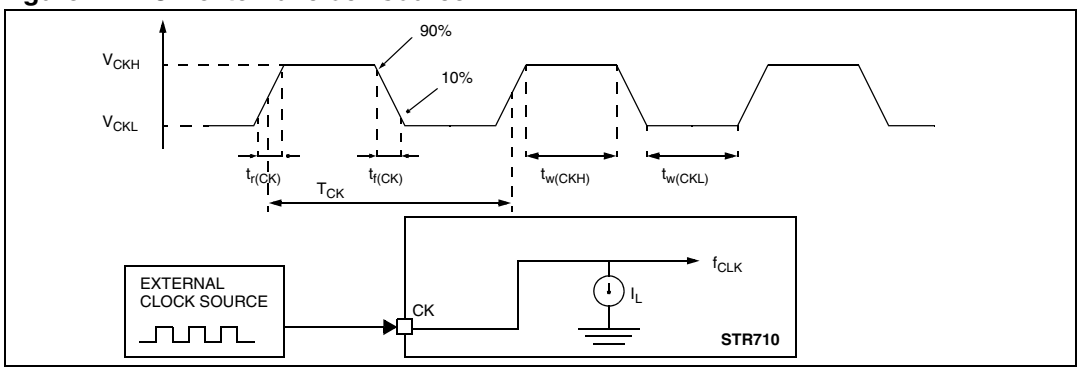
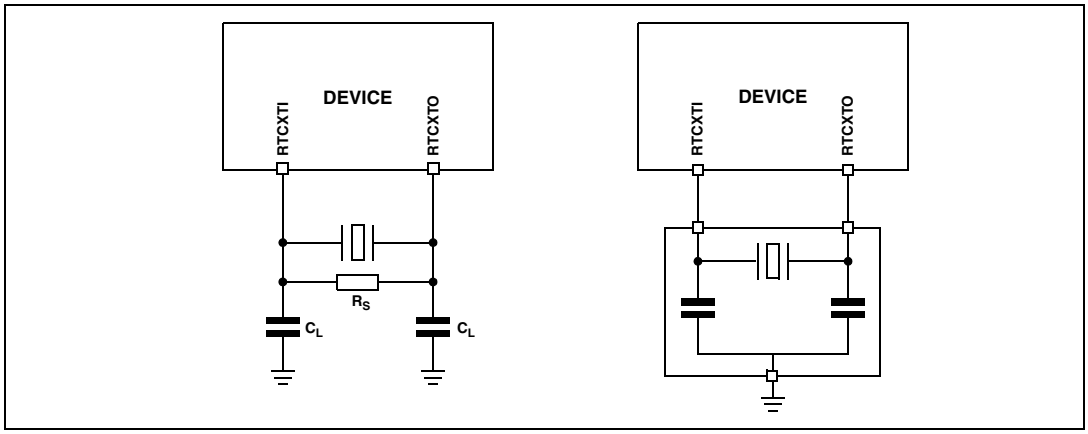


Figure 16. RTC crystal oscillator and resonator



PLL electrical characteristics

V_{33} = 3.0 to 3.6V, $V_{33IOPLL}$ = 3.0 to 3.6V, T_A = -40 / 85 °C unless otherwise specified.

Table 19. PLL1 characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$f_{PLLCLK1}$	PLL multiplier output clock				165	MHz
f_{PLL1}	PLL input clock	FREF_RANGE = 0	1.5		3.0	MHz
		FREF_RANGE = 1 MX[1:0]='00' or '01'	3.0		8.25	MHz
		FREF_RANGE = 1 MX[1:0]='10' or '11'	3.0		6	MHz
	PLL input clock duty cycle		25		75	%
f_{FREE1}	PLL free running frequency	FREF_RANGE = 0 MX[1:0]='01' or '11'		125		kHz
		FREF_RANGE = 0 MX[1:0]='00' or '10'		250		kHz
		FREF_RANGE = 1 MX[1:0]='01' or '11'		250		kHz
		FREF_RANGE = 1 MX[1:0]='00' or '10'		500		kHz
t_{LOCK1}	PLL lock time	FREF_RANGE = 0 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			300	µs
		FREF_RANGE = 1 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			600	µs

4.3.5 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{33} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 27. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage 1)	CMOS ports			$0.3V_{33}$	V
V_{IH}	Input high level voltage 1)		$0.7V_{33}$			
V_{hys}	Schmitt trigger voltage hysteresis 2)			0.8		V
V_{IL}	Input low level voltage 1)	P0.15 WAKEUP		0.9	0.8	V
V_{IH}	Input high level voltage 1)		2	1.35		
V_{hys}	Schmitt trigger voltage hysteresis 2)			0.4		V
V_{IL}	Input low level voltage 1)	TTL ports			0.8	V
V_{IH}	Input high level voltage 1)		2.0			
$I_{INJ(PIN)}$	Injected Current on any I/O pin				± 4	mA
$\Sigma I_{INJ(PIN)}$ 3)	Total injected current (sum of all I/O and control pins)				± 25	
I_{lkg}	Input leakage current 4)	$V_{SS} \le V_{IN} \le V_{33}$			±1	µA
R_{PU}	Weak pull-up equivalent resistor5)	$V_{IN}=V_{SS}$	110	150	700	kΩ
R_{PD}	Weak pull-down equivalent resistor5)	$V_{IN}=V_{33}$	110	150	700	kΩ
C_{IO}	I/O pin capacitance			5		pF

Notes:

1. Data based on characterization results, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
3. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{33}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Refer to *Section 4.2 on page 35* for more details.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. The R_{PU} pull-up and R_{PD} pull-down equivalent resistor are based on a resistive transistor (corresponding I_{PU} and I_{PD} current characteristics described in *Figure 18* to *Figure 19*).

$\overline{\text{RSTIN}}$ pin

The $\overline{\text{RSTIN}}$ pin input driver is CMOS. A permanent pull-up is present which is the same as as R_{PU} (see *Table 27 on page 51*)

Subject to general operating conditions for V_{33} and T_A unless otherwise specified.

Table 29. $\overline{\text{RESET}}$ pin characteristics

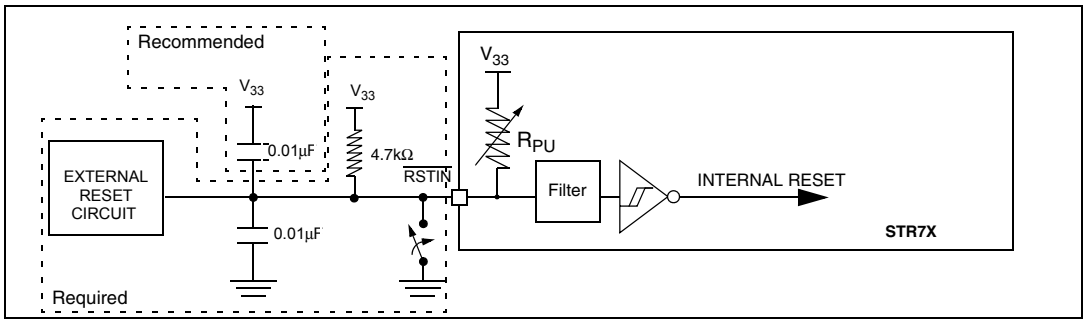
Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$V_{IL(RSTINn)}$	$\overline{\text{RSTIN}}$ Input low level voltage [1]				0.8	V
$V_{IH(RSTINn)}$	$\overline{\text{RSTIN}}$ Input high level voltage [1]		2			
$V_{F(RSTINn)}$	$\overline{\text{RSTIN}}$ Input filtered pulse[2]				500	ns
$V_{NF(RSTINn)}$	$\overline{\text{RSTIN}}$ Input not filtered pulse[2]		1.2			µs

Notes:

1. Data based on characterization results, not tested in production.

2) Data guaranteed by design, not tested in production.

Figure 24. Recommended $\overline{\text{RSTIN}}$ pin protection.[1]



Notes:

1. The R_{PU} pull-up equivalent resistor is based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 18*).
2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the $\overline{\text{RSTIN}}$ pin can go below the $V_{IL(RSTINn)}$ max. level specified in *Table 29*. Otherwise the reset will not be taken into account internally.

4.3.6 TIM timer characteristics

Subject to general operating conditions for V_{33}, f_{MCLK}, and T_A unless otherwise specified.

Refer to *Section 4.3.5: I/O port pin characteristics on page 51* for more details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output...).

Table 30. TIM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time		2			t_{CK_TIM}
$t_{res(TIM)}$	Timer resolution time		1			t_{PCLK2}
		f_{PCLK2} = 30 MHz	33.3			ns
f_{EXT}	Timer external clock frequency	$f_{CK\_TIM(MAX)} = f_{MCLK}$	0		$f_{CK\_TIM}/4$	MHz
		$f_{CK\_TIM} = f_{MCLK}$ = 60 MHz	0		15	MHz
Res_{TIM}	Timer resolution				16	bit
$t_{COUNTER}$	16-bit Counter clock period when internal clock is selected		1		65536	t_{PCLK2}
		f_{PCLK2} = 30 MHz	0.033		2184	µs
T_{MAX_COUNT}	Maximum Possible Count				65536x 65536	t_{PCLK}
		f_{PCLK2} = 30 MHz			143.1	s

4.3.7 EMI - external memory interface

Subject to general operating conditions for V_{DD}, f_{HCLK}, and T_A unless otherwise specified.

The tables below use a variable which is derived from the EMI_BCONn registers (described in the STR71x Reference Manual) and represents the special characteristics of the programmed memory cycle.

Table 31. EMI general characteristics

Symbol	Parameter	Value
t_{MCLK}	CPU clock period	1 / f_{MCLK}
t_C	Memory cycle time wait states	t_{MCLK} x (1 + [C_LENGTH])

Table 32. EMI read operation

Symbol	Parameter	Test Conditions	Value			Unit
			Min[1)]	Typ	Max[1)]	
t_{RCR}	Read to CSn Removal Time	MCLK=50 MHz 4 wait states 50 pf load on all pins	19	t_{MCLK}	21	ns
t_{RP}	Read Pulse Time		98	t_C	100	ns
t_{RDS}	Read Data Setup Time		22			ns
t_{RDH}	Read Data Hold Time		0			ns
t_{RAS}	Read Address Setup Time		27	$1.5*t_{MCLK}$	33	ns
t_{RAH}	Read Address Hold Time		0.65		2	ns
t_{RAT}	Read Address Turnaround Time		1.9		3.25	ns
t_{RRT}	RDn Turnaround Time		20	t_{MCLK}	21	ns

See *Figure 25*, *Figure 26*, *Figure 27* and *Figure 28* for related timing diagrams.

1. Data based on characterisation results, not tested in production.

Table 33. EMI write operation

Symbol	Parameter	Test conditions	Value			Unit
			Min[1)]	Typ	Max[1)]	
t_{WCR}	WEn to CSn Removal Time	MCLK=50 MHz 3 wait states 50 pf load on all pins	20	t_{MCLK}	22.5	ns
t_{WP}	Write Pulse Time		77.5	t_C	80	ns
t_{WDS1}	Write Data Setup Time 1		97	$t_C + t_{MCLK}$	100	ns
t_{WDS2}	Write Data Setup Time 2		77	t_C	80	ns
t_{WDH}	Write Data Hold Time		20	t_{MCLK}	23	ns
t_{WAS}	Write Address Setup Time		27	$1.5*t_{MCLK}$	33	ns
t_{WAH}	Write Address Hold Time		0.6		3	ns
t_{WAT}	Write Address Turnaround Time		1.75		4.1	ns
t_{WWT}	WEn Turnaround Time		20	t_{MCLK}	23	ns

See *Figure 29*, *Figure 30*, *Figure 31* and *Figure 32* for related timing diagrams.

1. Data based on characterisation results, not tested in production.

4.3.9 BSPI - buffered serial peripheral interface

Subject to general operating conditions for V_{DD}, T_A and f_{PCLK1} ,unless otherwise specified.

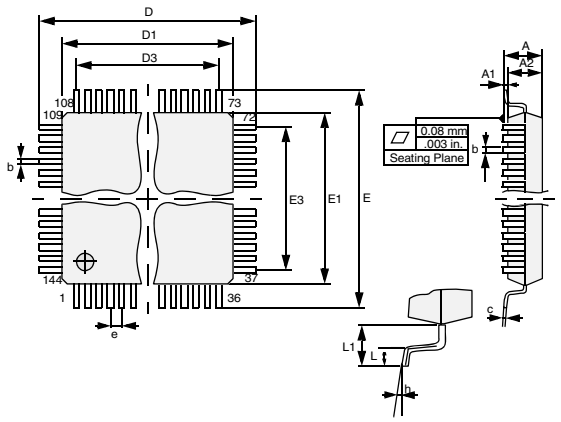
Refer to *I/O port pin characteristics on page 51* for more details on the input/output alternate function characteristics ($\overline{SS}$, SCK, MOSI, MISO).

Table 36. BSPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master	$f_{PCLK1}/254$	$f_{PCLK1}/6$ 5.5	MHz
		Slave	0	$f_{PCLK1}/8$ 3.3	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	capacitive charge C=50 pF		14	ns
$t_{su(\overline{SS})}$ (1)	$\overline{SS}$ setup time	Slave	0		
$t_{h(\overline{SS})}$ (1)	$\overline{SS}$ hold time	Slave	0		
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master f_{PCLK1}=33 MHz, presc = 6	73		
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master Slave	7 0		
$t_{h(MI)}$ 1)(2) $t_{h(SI)}$ 1)(2)	Data input hold time	Master Slave	$1xt_{PCLK1}$ $2xt_{PCLK1}$		
$t_{h(MI)}$ (1) $t_{h(SI)}$ (1)	Data input hold time	Master f_{PCLK1}=33 MHz Slave f_{PCLK1}=33 MHz	30 60		
$t_{a(SO)}$ 1)(3)	Data output access time	Slave	0	$1.5xt_{PCLK1}+42$	
		Slave f_{PCLK1}=33 MHz	0	87	
$t_{dis(SO)}$ (1)(4)	Data output disable time	Slave	0	42	
$t_{v(SO)}$ (1)(2)	Data output valid time	Slave (after enable edge)		$3xt_{PCLK1}+45$	
		f_{PCLK1}=33 MHz		135	
$t_{h(SO)}$ (1)	Data output hold time	Slave (after enable edge)	0		
$t_{v(MO)}$ (1)(2)	Data output valid time	Master (after enable edge)		$2xt_{PCLK1}+12$	
		f_{PCLK1}=33 MHz		72	
$t_{h(MO)}$ (1)	Data output hold time	Master (after enable edge)	0		

1. Data based on design simulation and/or characterisation results, not tested in production.
2. Depends on f_{PCLK1}. For example, if f_{PCLK1}=8 MHz, then t_{PCLK1} = $1/f_{PCLK1}$ =125 ns and $t_{v(MO)}$ = 255 ns.
3. Min. time is the minimum time to drive the output and the max. time is the maximum time to validate the data.
4. Min time is the minimun time to invalidate the output and the max time is the maximum time to put the data in Hi-Z.

Figure 41. 144-Pin low profile quad flat package

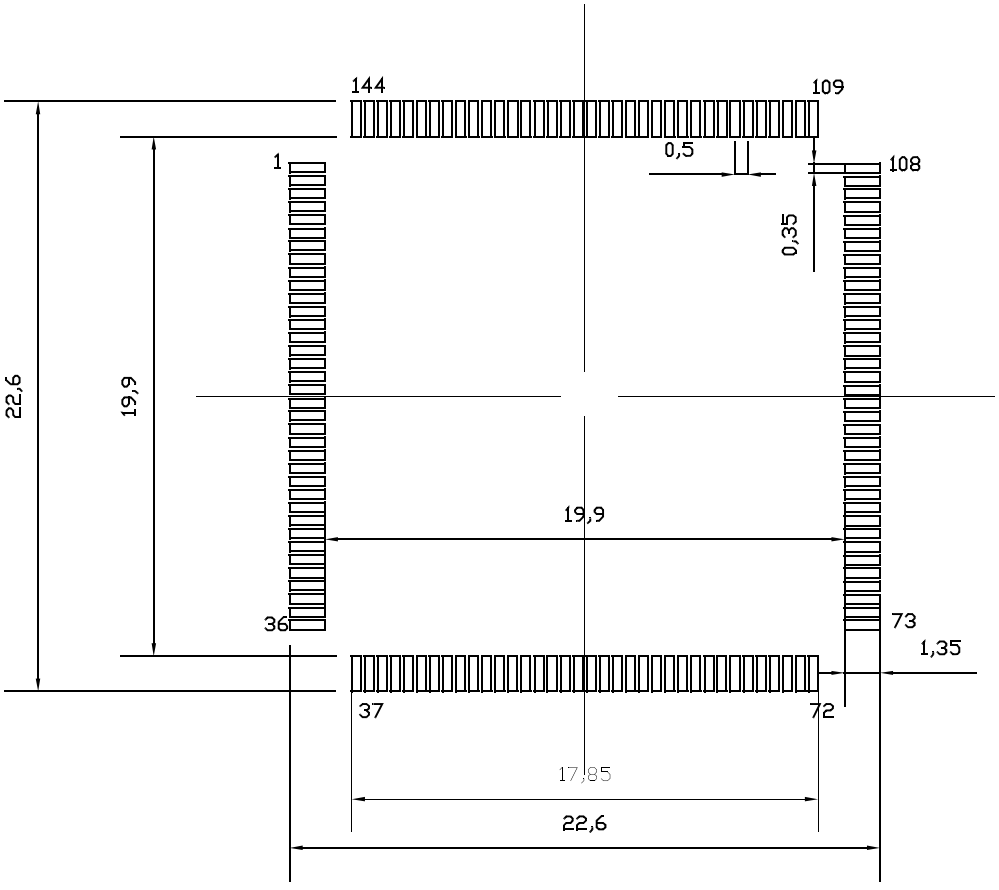


Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053		0.057
b	0.17	0.22	0.27	0.007		0.011
c	0.09		0.20	0.004		0.008
D	21.80	22.00	22.20	0.858	0.867	0.874
D1	19.80	20.00	20.20	0.780	0.787	0.795
D3		17.50			0.689	
E	21.80	22.00	22.20	0.858	0.867	0.874
E1	19.80	20.00	20.20	0.780	0.787	0.795
E3		17.50			0.689	
e		0.50			0.020	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	144					

Jedec Ref. MS-026-BFB

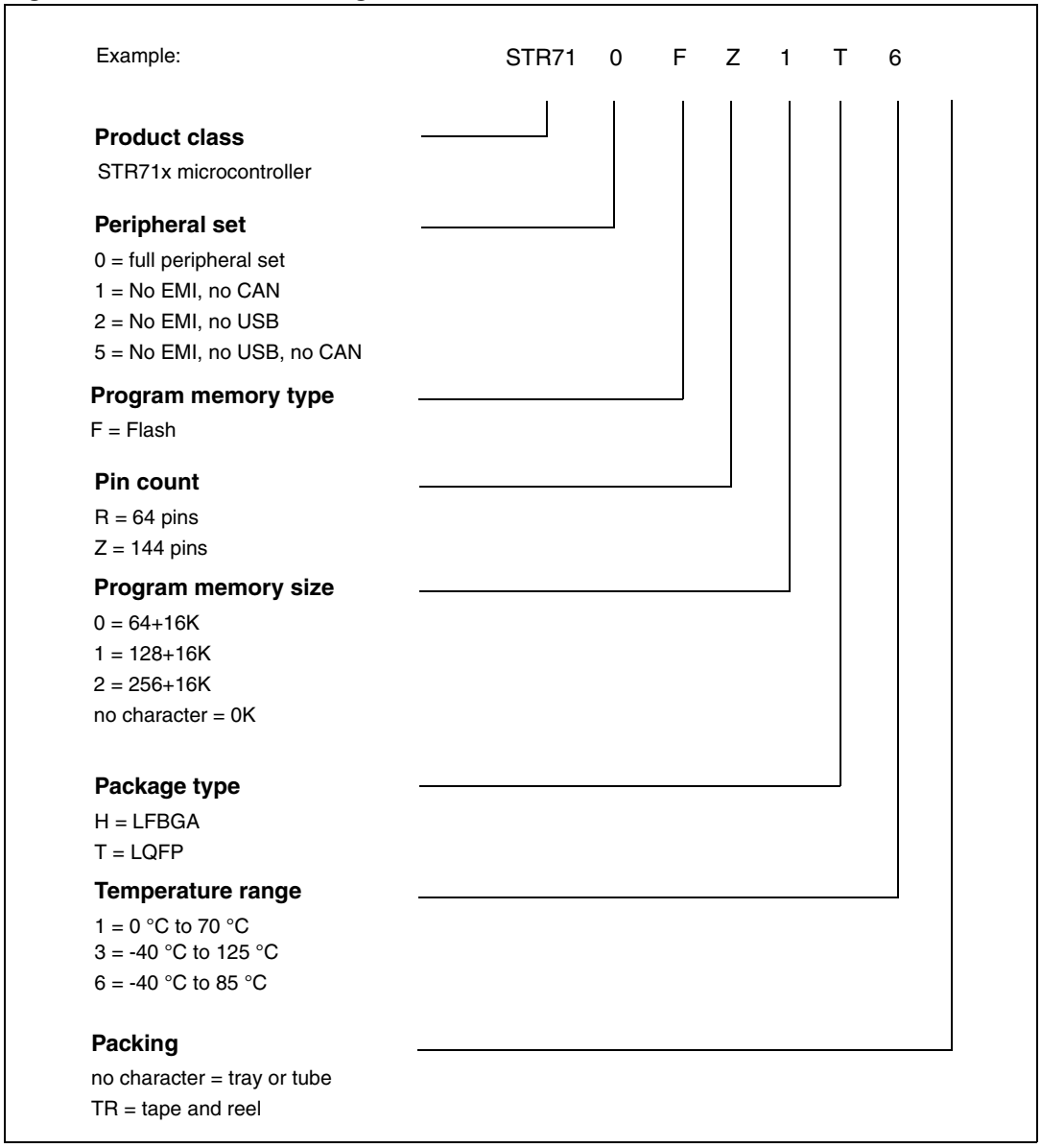
1.Values in inches are converted from mm and rounded to 3 decimal digits.

Recommended footprint (dimensions in mm)



7 Ordering information

Figure 49. STR71xF ordering information scheme



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to www.st.com or contact the ST Sales Office nearest to you.

Table 44. Document revision history (continued)

Date	Revision	Changes
22-May-2006	8	Added Flashless device. Changed reset state of pins P1.10 and P1.13 from pu to pd, P0.15 from pu to floating and removed x in interrupt column for P1.15 and P1.12 in *Table 4* and *Table 5* Added notes under *Table 4* on EMI pin reset state. Corrected inch value for d3 in *Figure 40* Added footprint diagrams in *Figure 40* and *Figure 43* Updated *Section 4: Electrical parameters*
01-Aug-2006	9	Flash data retention changed to 20 years at 85° C. Changed note 8 on page 19 Changed note 1 on page 45
06-Nov-2006	10	Added STR715FR0T1 in *Table 42: Order codes* P0.12 corrected in *Table 5 on page 25*
20-Mar-2007	11	Added characteristics of *BSPI - buffered serial peripheral interface on page 63* Updated *Table 21: Low-power mode wakeup timing on page 46*
13-Feb-2008	12	Updated ordering information Updated USB characteristics Updated external clock characteristics
03-Apr-2013	13	Updated title (to be in line with the “device summary” table) Updated ST Logo and Disclaimer Added *Section 8: Known limitations*

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT AUTHORIZED FOR USE IN WEAPONS. NOR ARE ST PRODUCTS DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com