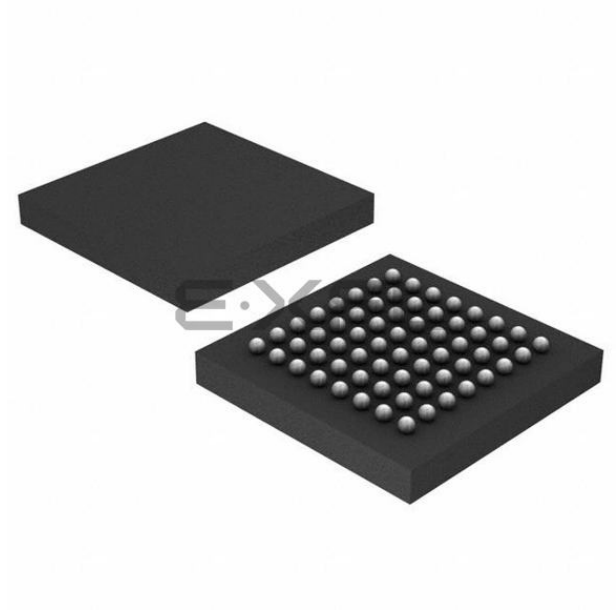


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	HDLC, I²C, SmartCard, SPI, UART/USART, USB
Peripherals	PWM, WDT
Number of I/O	30
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str711fr2h6

Contents

List of figures

2 Description

ARM® core with embedded Flash and RAM

The STR71x series is a family of ARM-powered 32-bit microcontrollers with embedded Flash and RAM. It combines the high performance ARM7TDMI CPU with an extensive range of peripheral functions and enhanced I/O capabilities. STR71xF devices have on-chip high-speed single voltage FLASH memory and high-speed RAM. STR710R devices have high-speed RAM but no internal Flash. The STR71x family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Extensive tools support

STMicroelectronics' 32-bit, ARM core-based microcontrollers are supported by a complete range of high-end and low-cost development tools to meet the needs of application developers. This extensive line of hardware/software tools includes starter kits and complete development packages all tailored for ST's ARM core-based MCUs. The range of development packages includes third-party solutions that come complete with a graphical development environment and an in-circuit emulator/programmer featuring a JTAG application interface. These support a range of embedded operating systems (OS), while several royalty-free OSs are also available.

For more information, please refer to ST MCU site http://www.st.com/mcu

3.3 Pin description for 144-pin packages

Figure 2. STR710 LQFP pinout

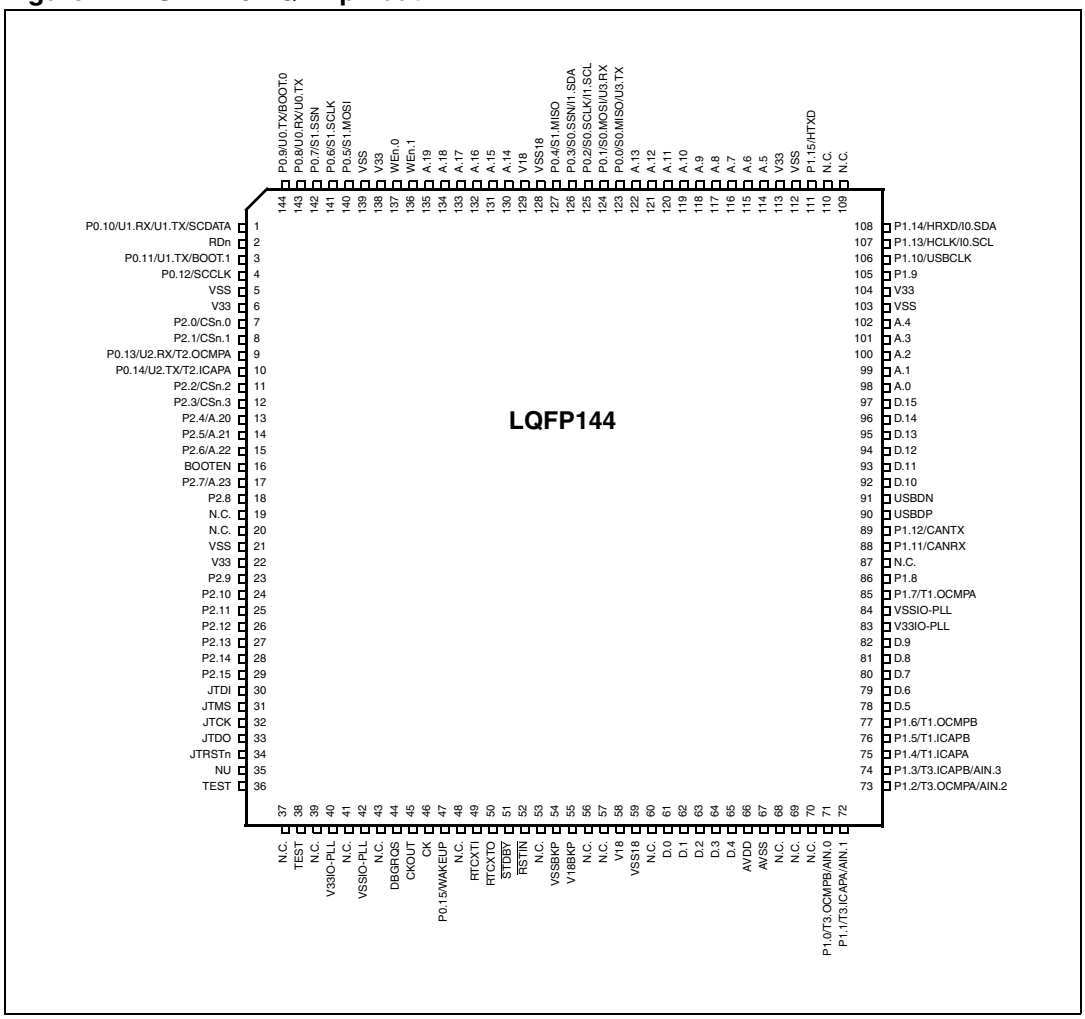


Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1)]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
20	P0.15/ WAKEUP	I		T_T	X				X	Port 0.15	Wakeup from Standby mode input.	
										Note: This port is input only.		
21	RTCXTI									Realtime Clock input and input of 32 kHz oscillator amplifier circuit		
22	RTCXTO									Output of 32 kHz oscillator amplifier circuit		
23	$\overline{STDBY}$	I/O		C_T		4mA	X		X	Input: Hardware Standby mode entry input active low. **Caution:** External pull-up to V_{33} required to select normal mode. Output: Standby mode active low output following Software Standby mode entry. **Note**: In Standby mode all pins are in high impedance except those marked Active in Stdby.		
24	$\overline{RSTIN}$	I		C_T					X	Reset input		
25	V_{SSBKP}			S					X	Stabilization for low power voltage regulator.		
26	V_{18BKP}			S					X	Stabilization for low power voltage regulator. Requires external capacitors of at least 1µF between V_{18BKP} and $V_{SS18BKP}$. See *Figure 5*. **Note:** If the low power voltage regulator is bypassed, this pin can be connected to an external 1.8V supply.		
27	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
28	V_{SS18}	S								Stabilization for main voltage regulator.		
29	V_{DDA}	S								Supply voltage for A/D Converter		
30	V_{SSA}	S								Ground voltage for A/D Converter		
31	P1.0/T3.OCMPB/AIN.0	I/O	pu	C_T		4mA	X	X		Port 1.0	Timer 3: Output Compare B	ADC: Analog input 0
32	P1.1/T3.ICAPA/T3.EXTCLK/AIN.1	I/O	pu	C_T		4mA	X	X		Port 1.1	Timer 3: Input Capture A or External Clock input	ADC: Analog input 1
33	P1.2/T3.OCMPA/AIN.2	I/O	pu	C_T		4mA	X	X		Port 1.2	Timer 3: Output Compare A	ADC: Analog input 2
34	P1.3/T3.ICAPB/AIN.3	I/O	pu	C_T		4mA	X	X		Port 1.3	Timer 3: Input Capture B	ADC: Analog input 3
35	P1.4/T1.ICAPA/T1.EXTCLK	I/O	pu	C_T		4mA	X	X		Port 1.4	Timer 1: Input Capture A	Timer 1: External Clock input

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
36	P1.5/T1.ICAPB	I/O	pu	C_T		4mA	X	X		Port 1.5	Timer 1: Input Capture B	
37	P1.6/T1.OCMPB	I/O	pu	C_T		4mA	X	X		Port 1.6	Timer 1: Output Compare B	
38	$V_{33IO-PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference[2]		
39	$V_{SSIO-PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[2]		
40	P1.7/T1.OCMPA	I/O	pu	C_T		4mA	X	X		Port 1.7	Timer 1: Output Compare A	
41	P1.8	I/O	pd	C_T		4mA	X	X		Port 1.8		
42	P1.11/CANRX	I/O	pu	C_T	X	4mA	X	X		Port 1.11	CAN: receive data input **Note:** On STR710 and STR712 only	
43	P1.12/CANTX	I/O	pu	C_T		4mA	X	X		Port 1.12	CAN: Transmit data output **Note:** On STR710 and STR712 only	
42	USBDP	I/O		C_T						USB bidirectional data (data +). Reset state = HiZ **Note:** On STR710 and STR711 only This pin requires an external pull-up to V_{33} to maintain a high level.		
43	USBDN	I/O		C_T						USB bidirectional data (data -). Reset state = HiZ **Note:** On STR710 and STR711 only.		
44	V_{SS}	S								Ground voltage for digital I/O circuitry[2]		
45	P1.9	I/O	pd	C_T		4mA	X	X		Port 1.9		
46	P1.10/USBCLK	I/O	pd	C/T		4mA	X	X		Port 1.10	USB: 48 MHZ clock input	
47	P1.13/HCLK/I0.SCL	I/O	pd	C_T	X	4mA	X	X		Port 1.13	HDLC: reference clock input	I2C clock
48	P1.14/HRXD/I0.SDA	I/O	pu	C_T	X	4mA	X	X		Port 1.14	HDLC: Receive data input	I2C serial data
49	P1.15/HTXD	I/O	pu	C_T		4mA	X	X		Port 1.15	HDLC: Transmit data output	
50	V_{SS}	S								Ground voltage for digital I/O circuitry[2]		
51	V_{33}	S								Supply voltage for digital I/O circuitry[2]		

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1)]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
52	P0.0/S0.MISO /U3.TX	I/O	pu	C_T		4mA	X	X		Port 0.0	SPI0 Master in/Slave out data	UART3 Transmit data output
											Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
53	P0.1/S0.MOSI /U3.RX	I/O	pu	C_T	X	4mA	X	X		Port 0.1	BSPI0: Master out/Slave in data	UART3: Receive Data input
											Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
54	P0.2/S0.SCLK /I1.SCL	I/O	pu	C_T	X	4mA	X	X		Port 0.2	BSPI0: Serial Clock	I2C1: Serial clock
											Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
55	P0.3/S0.$\overline{SS}$/I1 .SDA	I/O	pu	C_T		4mA	X	X		Port 0.3	SPI0: Slave Select input active low.	I2C1: Serial Data
											Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
56	P0.4/S1.MISO	I/O	pu	C_T		4mA	X	X		Port 0.4	SPI1: Master in/Slave out data	
57	V_{SS18}	S								Stabilization for main voltage regulator.		
58	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
59	V_{SS}	S								Ground voltage for digital I/Os		
60	P0.5/S1.MOSI	I/O	pu	C_T		4mA	X	X		Port 0.5	SPI1: Master out/Slave In data	
61	P0.6/S1.SCLK	I/O	pu	C_T	X	4mA	X	X		Port 0.6	SPI1: Serial Clock	
62	P0.7/S1.$\overline{SS}$	I/O	pu	C_T		4mA	X	X		Port 0.7	SPI1: Slave Select input active low	

3.6 I/O port configuration

Table 6. Port bit configuration table

Configuration mode		Input buffer	PxD register		PxC2 register	PxC1 register	PxC0 register
			Read access	Write access			
INPUT	TTL Input Floating	TTL floating	I/O pin	don't care	0	0	1
	CMOS Input Floating	CMOS floating	I/O pin	don't care	0	1	0
	CMOS Input Pull-Down (IPUPD)	CMOS Pull-Down	I/O pin	0	0	1	1
	CMOS Input Pull-Up (IPUPD)	CMOS Pull-Up	I/O pin	1	0	1	1
	Analog input	AIN	0	don't care	0	0	0
OUTPUT	Output Open-Drain	N.A.	I/O pin	0 or 1	1	0	0
	Output Push-Pull	N.A.	last value written	0 or 1	1	0	1
	Alternate Function Open-Drain	CMOS floating	I/O pin	don't care	1	1	0
	Alternate Function Push-Pull	CMOS floating	I/O pin	don't care	1	1	1

Legend:

AIN: Analog Input

CMOS: CMOS Input levels

IPUPD: Input Pull Up /Pull Down

TTL: TTL Input levels

N.A.: not applicable. In Output mode, a read access to the port gets the output latch value.

Figure 8. External memory map

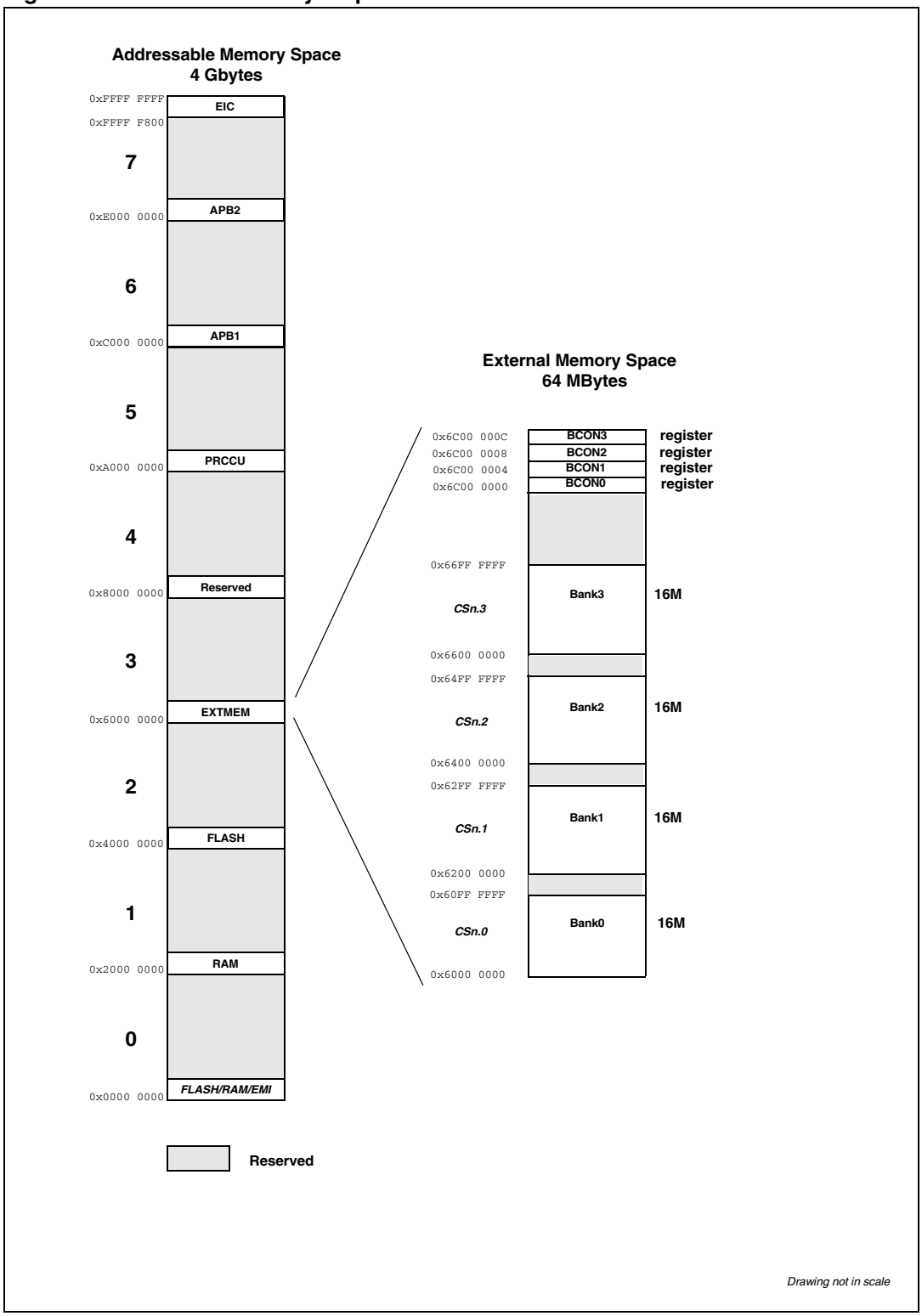


Table 17. RTCXT1 external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RTCXT1}	External clock source frequency		0		500	kHz
$V_{RTCXT1H}$	RTCXT1 input pin high level voltage		$0.7xV_{33}$		V_{33}	V
$V_{RTCXT1L}$	RTCXT1 input pin low level voltage		V_{SS}		$0.3xV_{33}$	
$t_{w(RTCXT1)}$ $t_{w(RTCXT1)}$	RTCXT1 high or low time [1]		100			ns
$t_{r(RTCXT1)}$ $t_{f(RTCXT1)}$	RTCXT1 rise or fall time [1]				5	
$C_{IN(RTCXT1)}$	RTCXT1 input capacitance[1]			5		pF
DuCy(RTCXT1)	Duty cycle		30		70	%
I_L	RTCXT1 Input leakage current	$V_{SS} \le V_{IN} \le V_{33}$			±1	µA

Notes:

1. Data based on design simulation and/or technology characteristics, not tested in production.

Table 25. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value [1]	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25°C	2000	V
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)		200	
$V_{ESD(CDM)}$	Electro-static discharge voltage (Charge Device Model)		750 on corner pins, 500 on others	

Notes:

1. Data based on characterization results, not tested in production.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Electrical sensitivities

Table 26. Static and dynamic latch-up

Symbol	Parameter	Conditions	Class[1]
LU	Static latch-up class	T_A=+25°C T_A=+85°C T_A=+105°C	A A A
DLU	Dynamic latch-up class	V_{DD}=3.3 V, f_{OSC4M}=4 MHz, f_{MCLK}=32 MHz, T_A=+25°C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

Figure 17. R_{PU} vs. V_{33} with $V_{IN}=V_{SS}$

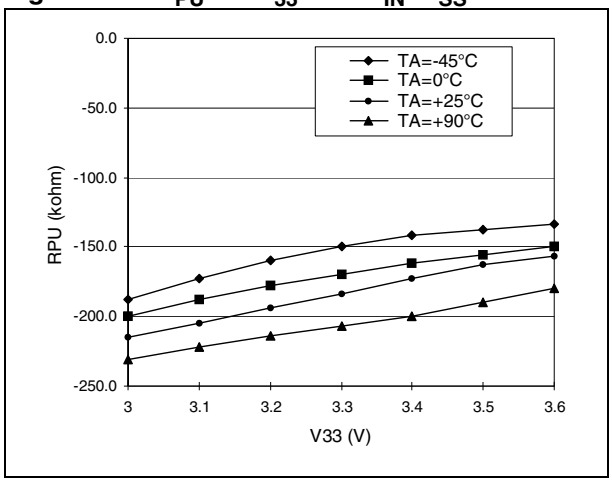


Figure 18. I_{PU} vs. V_{33} with $V_{IN}=V_{SS}$

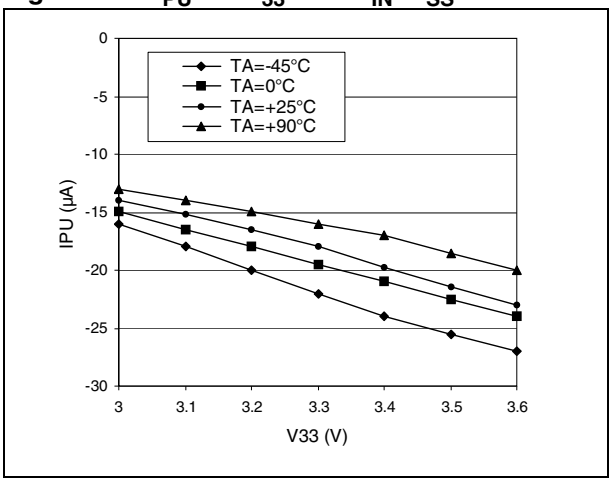


Figure 19. R_{PD} vs. V_{33} with $V_{IN}=V_{33}$

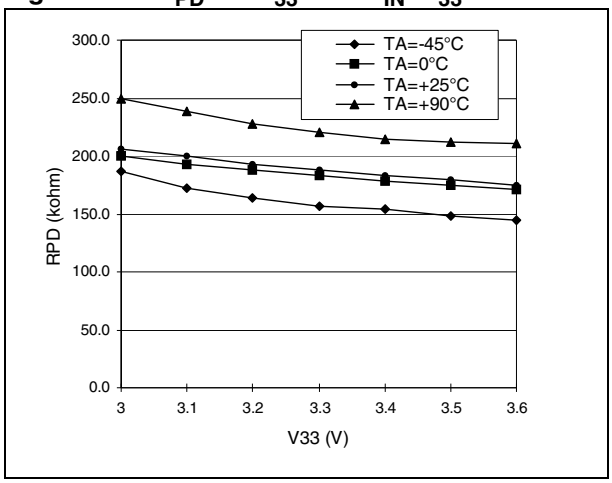
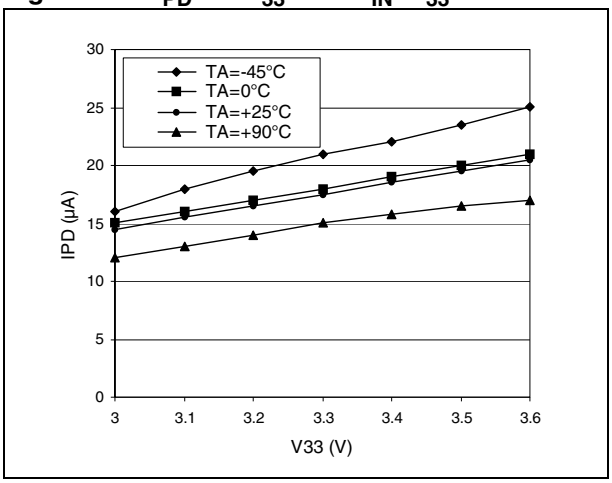


Figure 20. I_{PD} vs. V_{33} with $V_{IN}=V_{33}$



$\overline{\text{RSTIN}}$ pin

The $\overline{\text{RSTIN}}$ pin input driver is CMOS. A permanent pull-up is present which is the same as as R_{PU} (see *Table 27 on page 51*)

Subject to general operating conditions for V_{33} and T_A unless otherwise specified.

Table 29. $\overline{\text{RESET}}$ pin characteristics

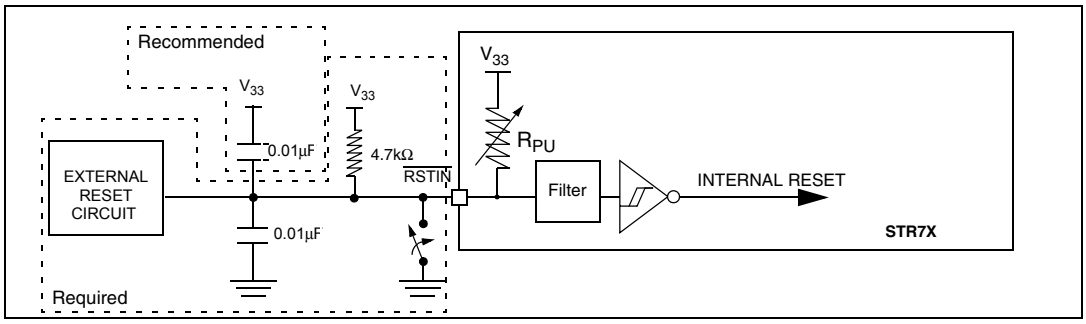
Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$V_{IL(RSTINn)}$	$\overline{\text{RSTIN}}$ Input low level voltage [1]				0.8	V
$V_{IH(RSTINn)}$	$\overline{\text{RSTIN}}$ Input high level voltage [1]		2			
$V_{F(RSTINn)}$	$\overline{\text{RSTIN}}$ Input filtered pulse[2]				500	ns
$V_{NF(RSTINn)}$	$\overline{\text{RSTIN}}$ Input not filtered pulse[2]		1.2			µs

Notes:

1. Data based on characterization results, not tested in production.

2) Data guaranteed by design, not tested in production.

Figure 24. Recommended $\overline{\text{RSTIN}}$ pin protection.[1]



Notes:

1. The R_{PU} pull-up equivalent resistor is based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 18*).
2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the $\overline{\text{RSTIN}}$ pin can go below the $V_{IL(RSTINn)}$ max. level specified in *Table 29*. Otherwise the reset will not be taken into account internally.

4.3.6 TIM timer characteristics

Subject to general operating conditions for V_{33}, f_{MCLK}, and T_A unless otherwise specified.

Refer to *Section 4.3.5: I/O port pin characteristics on page 51* for more details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output...).

Table 30. TIM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time		2			t_{CK_TIM}
$t_{res(TIM)}$	Timer resolution time		1			t_{PCLK2}
		f_{PCLK2} = 30 MHz	33.3			ns
f_{EXT}	Timer external clock frequency	$f_{CK\_TIM(MAX)} = f_{MCLK}$	0		$f_{CK\_TIM}/4$	MHz
		$f_{CK\_TIM} = f_{MCLK}$ = 60 MHz	0		15	MHz
Res_{TIM}	Timer resolution				16	bit
$t_{COUNTER}$	16-bit Counter clock period when internal clock is selected		1		65536	t_{PCLK2}
		f_{PCLK2} = 30 MHz	0.033		2184	µs
T_{MAX_COUNT}	Maximum Possible Count				65536x 65536	t_{PCLK}
		f_{PCLK2} = 30 MHz			143.1	s

4.3.7 EMI - external memory interface

Subject to general operating conditions for V_{DD}, f_{HCLK}, and T_A unless otherwise specified.

The tables below use a variable which is derived from the EMI_BCONn registers (described in the STR71x Reference Manual) and represents the special characteristics of the programmed memory cycle.

Table 31. EMI general characteristics

Symbol	Parameter	Value
t_{MCLK}	CPU clock period	1 / f_{MCLK}
t_C	Memory cycle time wait states	t_{MCLK} x (1 + [C_LENGTH])

Table 32. EMI read operation

Symbol	Parameter	Test Conditions	Value			Unit
			Min[1)]	Typ	Max[1)]	
t_{RCR}	Read to CSn Removal Time	MCLK=50 MHz 4 wait states 50 pf load on all pins	19	t_{MCLK}	21	ns
t_{RP}	Read Pulse Time		98	t_C	100	ns
t_{RDS}	Read Data Setup Time		22			ns
t_{RDH}	Read Data Hold Time		0			ns
t_{RAS}	Read Address Setup Time		27	$1.5*t_{MCLK}$	33	ns
t_{RAH}	Read Address Hold Time		0.65		2	ns
t_{RAT}	Read Address Turnaround Time		1.9		3.25	ns
t_{RRT}	RDn Turnaround Time		20	t_{MCLK}	21	ns

See *Figure 25*, *Figure 26*, *Figure 27* and *Figure 28* for related timing diagrams.

1. Data based on characterisation results, not tested in production.

Table 33. EMI write operation

Symbol	Parameter	Test conditions	Value			Unit
			Min[1)]	Typ	Max[1)]	
t_{WCR}	WEn to CSn Removal Time	MCLK=50 MHz 3 wait states 50 pf load on all pins	20	t_{MCLK}	22.5	ns
t_{WP}	Write Pulse Time		77.5	t_C	80	ns
t_{WDS1}	Write Data Setup Time 1		97	$t_C + t_{MCLK}$	100	ns
t_{WDS2}	Write Data Setup Time 2		77	t_C	80	ns
t_{WDH}	Write Data Hold Time		20	t_{MCLK}	23	ns
t_{WAS}	Write Address Setup Time		27	$1.5*t_{MCLK}$	33	ns
t_{WAH}	Write Address Hold Time		0.6		3	ns
t_{WAT}	Write Address Turnaround Time		1.75		4.1	ns
t_{WWT}	WEn Turnaround Time		20	t_{MCLK}	23	ns

See *Figure 29*, *Figure 30*, *Figure 31* and *Figure 32* for related timing diagrams.

1. Data based on characterisation results, not tested in production.

Figure 25. Read cycle timing: 16-bit read on 16-bit memory

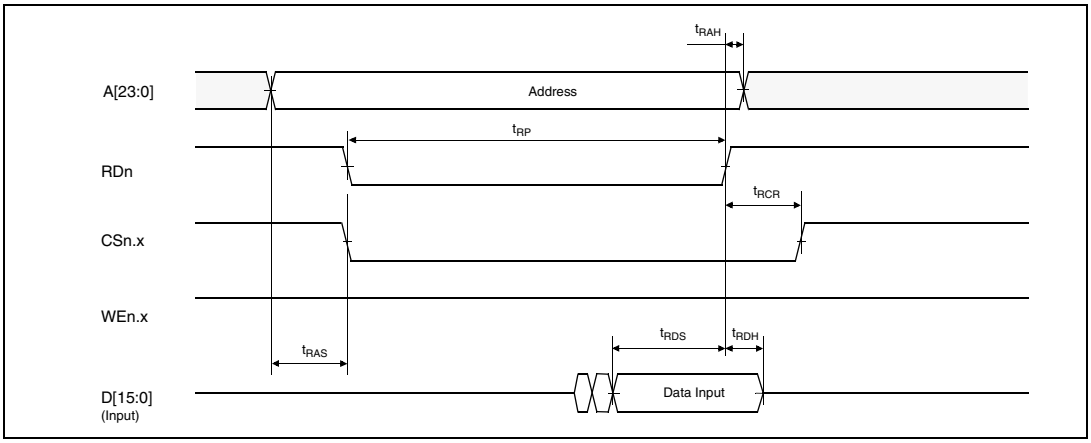
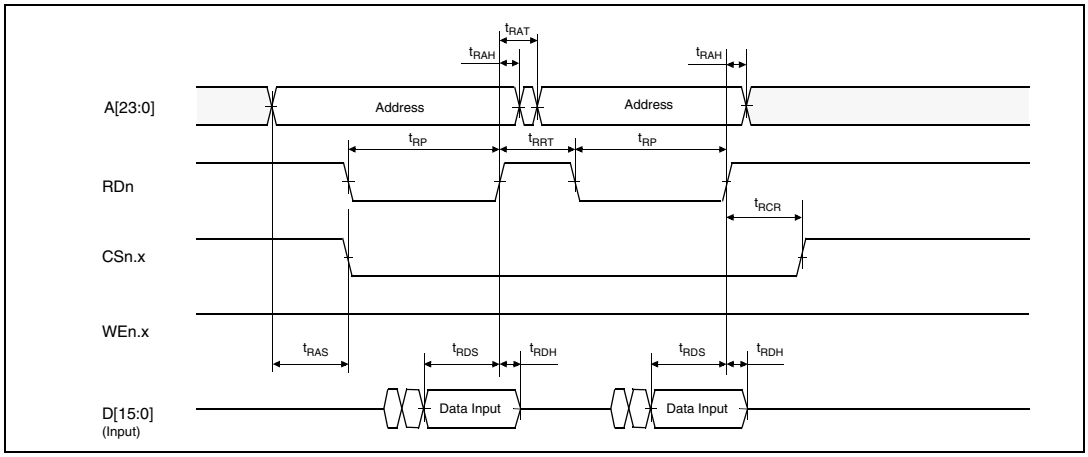


Figure 26. Read cycle timing: 32-bit read on 16-bit memory



See *Table 32* for read timing data.

Figure 27. Read cycle timing: 16-bit read on 8-bit memory

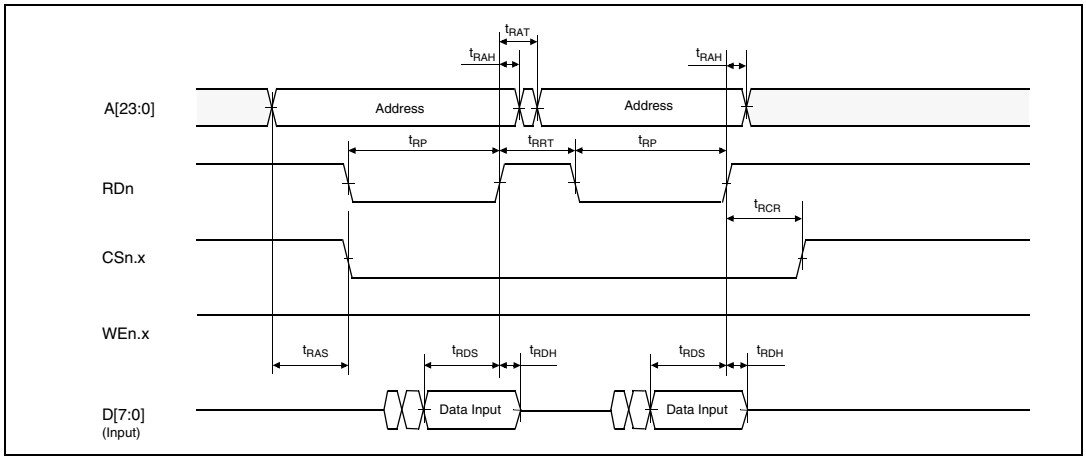
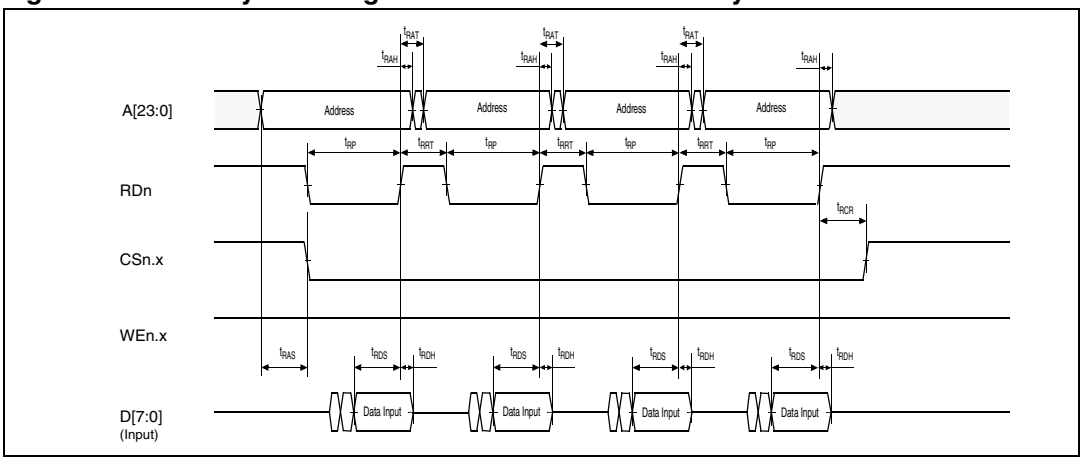


Figure 28. Read cycle timing: 32-bit read on 8-bit memory



See *Table 32* for read timing data.

Figure 29. Write cycle timing: 16-bit write on 16-bit memory

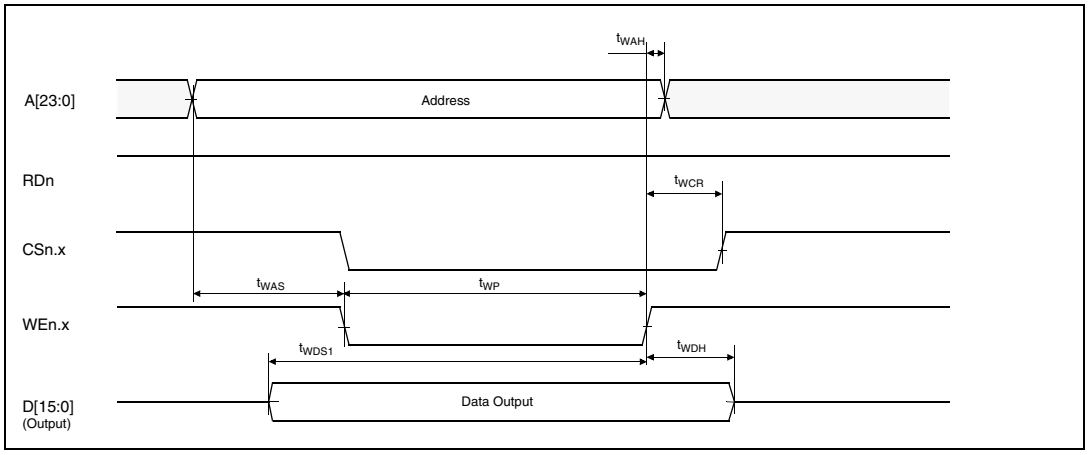
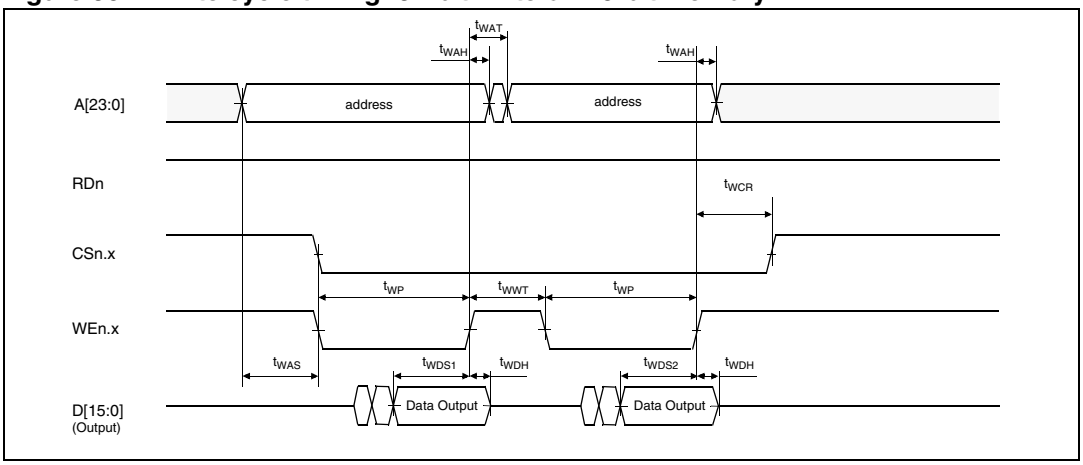


Figure 30. Write cycle timing: 32-bit write on 16-bit memory



See *Table 44* for write timing data.

Table 34. I2C characteristics

Symbol	Parameter	Standard mode I^2C		Fast mode I^2C[5]		Unit
		Min [1]	Max [1]	Min [1]	Max [1]	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0 [3]		0 [2]	900 [3]	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	20+0.1C_b	300	
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

Notes:

1. Data based on standard I^2C protocol requirement, not tested in production.
2. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
3. The maximum hold time $t_{h(SDA)}$ is not applicable.
4. Measurement points are done at CMOS levels: $0.3xV_{DD}$ and $0.7xV_{DD}$.
5. f_{PCLK1}, must be at least 8 MHz to achieve max fast I^2C speed (400 kHz).
6. The following table gives the values to be written in the I2CCCR register to obtain the required I^2C SCL line frequency.

Table 41. ADC accuracy with f_{PCLK2} = 20 MHz, f_{ADC}=10 MHz, AV_{DD}=3.3 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ADC_DATA(0V)	Converted code when AIN=0V 1)		2370		2565	Decimal code
ADC_DATA(2.5V)	Converted code when AIN=2.5V 1)		1480		1680	
VCM	Center voltage of Sigma-Delta Modulator1)		1.23	1.25	1.30	V
TUE	Total unadjusted error	In this type of ADC, calibration is necessary to correct gain error and offset errors. Once calibrated, the TUE is limited to the ILE.				
$\lvert E_D \rvert$	Differential linearity error1)			1.96	2.19	LSB
$\lvert E_L \rvert$	Integral linearity error 1)			2.36	3.95	

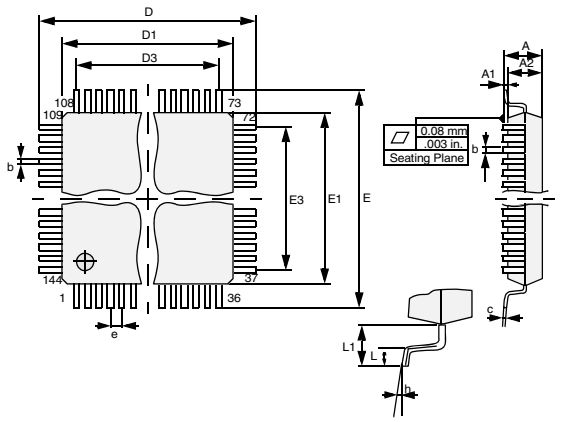
Data are based on characterisation and are not tested in production.

ADC Accuracy vs. Negative Injection Current

Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. The effect of negative injection current on robust pins is specified in *Section 4.3.5*.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 4.3.5* does not affect the ADC accuracy.

Figure 41. 144-Pin low profile quad flat package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053		0.057
b	0.17	0.22	0.27	0.007		0.011
c	0.09		0.20	0.004		0.008
D	21.80	22.00	22.20	0.858	0.867	0.874
D1	19.80	20.00	20.20	0.780	0.787	0.795
D3		17.50			0.689	
E	21.80	22.00	22.20	0.858	0.867	0.874
E1	19.80	20.00	20.20	0.780	0.787	0.795
E3		17.50			0.689	
e		0.50			0.020	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	144					

Jedec Ref. MS-026-BFB

1.Values in inches are converted from mm and rounded to 3 decimal digits.

Recommended footprint (dimensions in mm)