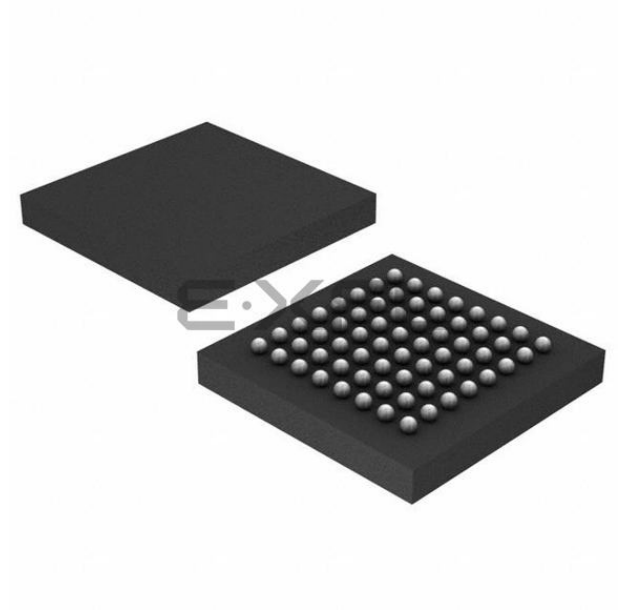


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, HDLC, I²C, SmartCard, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8 + 16K)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str712fr0h6

List of tables

1 Introduction

This datasheet provides the STR71x pinout, ordering information, mechanical and electrical device characteristics.

For complete information on the STR71x microcontroller memory, registers and peripherals. please refer to the STR71x reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash programming reference manual.

For information on the ARM7TDMI core please refer to the ARM7TDMI technical reference manual.

Table 2. Device overview

Features	STR710 FZ1	STR710 FZ2	STR710 RZ	STR711 FR0	STR711 FR1	STR711 FR2	STR712 FR0	STR712 FR1	STR712 FR2	STR715 FRx
Flash - Kbytes	128+16	256+16	0	64+16	128+16	256+16	64+16	128+16	256+16	64+16
RAM - Kbytes	32	64	64	16	32	64	16	32	64	16
Peripheral Functions	CAN, EMI, USB, 48 I/Os			USB, 30 I/Os			CAN, 32 I/Os			32 I/Os
Operating Voltage	3.0 to 3.6 V									
Operating Temperature	-40 to +85°C or 0 to 70° C									
Packages	**T**=LQFP144 20 x 20 **H**=LFBGA144 10 x10			**T**=LQFP64 10 x10						

.

2 Description

ARM® core with embedded Flash and RAM

The STR71x series is a family of ARM-powered 32-bit microcontrollers with embedded Flash and RAM. It combines the high performance ARM7TDMI CPU with an extensive range of peripheral functions and enhanced I/O capabilities. STR71xF devices have on-chip high-speed single voltage FLASH memory and high-speed RAM. STR710R devices have high-speed RAM but no internal Flash. The STR71x family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Extensive tools support

STMicroelectronics' 32-bit, ARM core-based microcontrollers are supported by a complete range of high-end and low-cost development tools to meet the needs of application developers. This extensive line of hardware/software tools includes starter kits and complete development packages all tailored for ST's ARM core-based MCUs. The range of development packages includes third-party solutions that come complete with a graphical development environment and an in-circuit emulator/programmer featuring a JTAG application interface. These support a range of embedded operating systems (OS), while several royalty-free OSs are also available.

For more information, please refer to ST MCU site http://www.st.com/mcu

Realtime clock (RTC)

The RTC provides a set of continuously running counters driven by the 32 kHz external crystal. The RTC can be used as a general timebase or clock/calendar/alarm function. When the STR71x is in Standby mode the RTC can be kept running, powered by the low power voltage regulator and driven by the 32 kHz external crystal.

UARTs

The 4 UARTs allow full duplex, asynchronous, communications with external devices with independently programmable TX and RX baud rates up to 1.25 Mb/s.

Smartcard interface

UART1 is configurable to function either as a general purpose UART or as an asynchronous Smartcard interface as defined by ISO 7816-3. It includes Smartcard clock generation and provides support features for synchronous cards.

Buffered serial peripheral interfaces (BSPI)

Each of the two SPIs allow full duplex, synchronous communications with external devices, master or slave communication at up to 5.5 Mb/s in Master mode and 4 Mb/s in Slave mode.

I^2C interfaces

The two I^2C Interfaces provide multi-master and slave functions, support normal and fast I^2C mode (400 kHz) and 7 or 10-bit addressing modes.

One I^2C Interface is multiplexed with one SPI, so either 2xSPI+1x I^2C or 1xSPI+2x I^2C may be used at a time.

HDLC interface

The High Level Data Link Controller (HDLC) unit supports full duplex operation and NRZ, NRZI, FM0 or MANCHESTER protocols. It has an internal 8-bit baud rate generator.

A/D converter

The Analog to Digital Converter, converts in single channel or up to 4 channels in single-shot or round robin mode. Resolution is 12-bit with a sampling frequency of up to 1 kHz. The input voltage range is 0-2.5V.

Watchdog

The 16-bit Watchdog Timer protects the application against hardware or software failures and ensures recovery by generating a reset.

I/O ports

The 48 I/O ports are programmable as Inputs or Outputs.

External interrupts

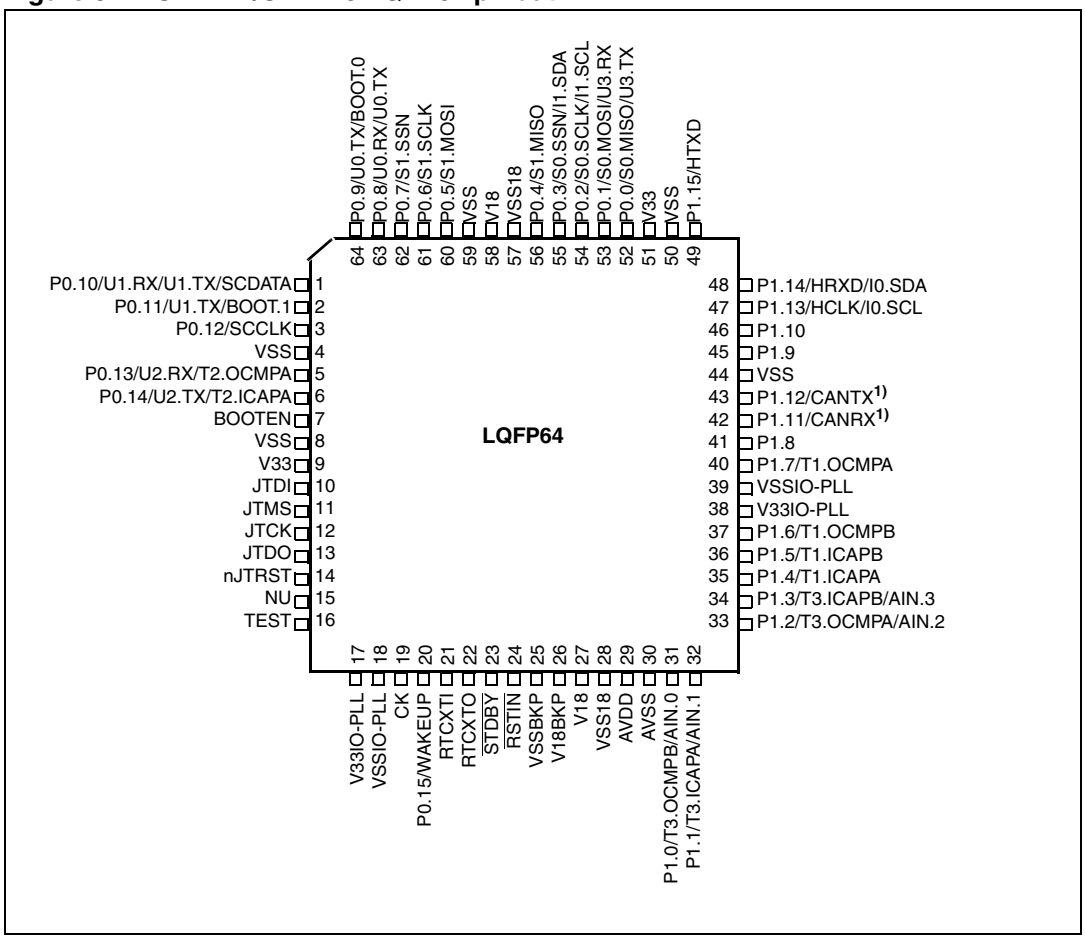
Up to 14 external interrupts are available for application use or to wake up the application from STOP mode.

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
1	A1	P0.10/U1.RX/ U1.TX/ SC.DATA	I/O	pd	C_T	X	4mA	T			Port 0.10	UART1: Receive Data input	UART1: Transmit data output.
												Note: This pin may be used for Smartcard DataIn/DataOut or single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress	
2	B2	$\overline{RD}$	O	5)					X		External Memory Interface: Active low read signal for external memory. It maps to the OE_N input of the external components.		
3	C2	P0.11/BOOT.1 /U1.TX	I/O	pd	C_T		4mA	X	X		Port 0.11	Select Boot Configuration input	UART1: Transmit data output.
4	C3	P0.12/SC.CLK	I/O	pd	C_T		4mA	X	X		Port 0.12	Smartcard reference clock output	
5	D1	V_{SS}	S								Ground voltage for digital I/Os[4]		
6	D2	V_{33}	S								Supply voltage for digital I/Os[4]		
7	B1	P2.0/$\overline{CS}$.0	I/O	8)	C_T		8mA	X	X		Port 2.0	External Memory Interface: Select Memory Bank 0 output **Note:** This pin is forced to output push-pull 1 mode at reset to allow boot from external memory	
8	C1	P2.1/$\overline{CS}$.1	I/O	pu 2)	C_T		8mA	X	X		Port 2.1	External Memory Interface: Select Memory Bank 1 output	
9	D3	P0.13/U2.RX/ T2.OCMPA	I/O	pu	C_T	X	4mA	X	X		Port 0.13	UART2: Receive Data input	Timer2: Output Compare A output
10	D4	P0.14/U2.TX/ T2.ICAPA	I/O	pu	C_T		4mA	X	X		Port 0.14	UART2: Transmit data output	Timer2: Input Capture A input
11	E1	P2.2/$\overline{CS}$.2	I/O	pu 2)	C_T		8mA	X	X		Port 2.2	External Memory Interface: Select Memory Bank 2 output	
12	E2	P2.3/$\overline{CS}$.3	I/O	pu 2)	C_T		8mA	X	X		Port 2.3	External Memory Interface: Select Memory Bank 3 output	

3.4 Pin description for 64-pin packages

Figure 3. STR712/STR715 LQFP64 pinout



1. CANTX and CANRX in STR712F only, in STR715F they are general purpose I/Os.

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1)]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
20	P0.15/ WAKEUP	I		T_T	X				X	Port 0.15	Wakeup from Standby mode input.	
										Note: This port is input only.		
21	RTCXTI									Realtime Clock input and input of 32 kHz oscillator amplifier circuit		
22	RTCXTO									Output of 32 kHz oscillator amplifier circuit		
23	$\overline{STDBY}$	I/O		C_T		4mA	X		X	Input: Hardware Standby mode entry input active low. **Caution:** External pull-up to V_{33} required to select normal mode. Output: Standby mode active low output following Software Standby mode entry. **Note**: In Standby mode all pins are in high impedance except those marked Active in Stdby.		
24	$\overline{RSTIN}$	I		C_T					X	Reset input		
25	V_{SSBKP}			S					X	Stabilization for low power voltage regulator.		
26	V_{18BKP}			S					X	Stabilization for low power voltage regulator. Requires external capacitors of at least 1µF between V_{18BKP} and $V_{SS18BKP}$. See *Figure 5*. **Note:** If the low power voltage regulator is bypassed, this pin can be connected to an external 1.8V supply.		
27	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
28	V_{SS18}	S								Stabilization for main voltage regulator.		
29	V_{DDA}	S								Supply voltage for A/D Converter		
30	V_{SSA}	S								Ground voltage for A/D Converter		
31	P1.0/T3.OCMPB/AIN.0	I/O	pu	C_T		4mA	X	X		Port 1.0	Timer 3: Output Compare B	ADC: Analog input 0
32	P1.1/T3.ICAPA/T3.EXTCLK/AIN.1	I/O	pu	C_T		4mA	X	X		Port 1.1	Timer 3: Input Capture A or External Clock input	ADC: Analog input 1
33	P1.2/T3.OCMPA/AIN.2	I/O	pu	C_T		4mA	X	X		Port 1.2	Timer 3: Output Compare A	ADC: Analog input 2
34	P1.3/T3.ICAPB/AIN.3	I/O	pu	C_T		4mA	X	X		Port 1.3	Timer 3: Input Capture B	ADC: Analog input 3
35	P1.4/T1.ICAPA/T1.EXTCLK	I/O	pu	C_T		4mA	X	X		Port 1.4	Timer 1: Input Capture A	Timer 1: External Clock input

4.3 Operating conditions

Subject to general operating conditions for V_{33}, and T_A.

Table 11. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	Internal CPU Clock frequency	Accessing SRAM or external memory with 0 wait states	0	66	MHz
		Accessing FLASH in burst mode	0	50	
		Executing from FLASH with RWW	0	45 [1)]	
		Accessing FLASH with 0 wait states	0	33	
f_{PCLK}	Internal APB Clock frequency		0	33	MHz
V_{33}	Standard Operating Voltage (includes V_{33I0_PLL})		3.0	3.6	V
V_{18BKP}	Backup Operating Voltage		1.4	1.8	V
T_A	Ambient temperature range	6 Partnumber Suffix	-40	85	°C

1. Data guaranteed by characterization, not tested in production

Table 12. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{V33}	V_{33} rise time rate	Subject to general operating conditions for T_A.	20			µs/V
					20	ms/V

4.3.1 Supply current characteristics

The current consumption is measured as described in *Figure 9 on page 34* and *Figure 10 on page 34*.

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{33} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.
- Embedded Regulators are used to provide 1.8V (except if explicitly mentioned)

Subject to general operating conditions for V_{33}, and T_A.

Table 13. Total current consumption

Symbol	Parameter	Conditions	Typ [1]	Max [2]	Unit
I_{DD} [4]	Supply current in RUN mode	f_{MCLK}=66 MHz, RAM execution	73.6	100	mA
		f_{MCLK}=32 MHz, Flash non-burst execution	49.3		
	Supply current in STOP mode	T_A=25°C	10	50[3]	µA
	Supply current in STANDBY mode	OSC32K bypassed	12	30	µA

Notes:

1. Typical data are based on T_A=25°C, V_{33}=3.3V.
2. Data based on characterization results, tested in production at V_{33}, f_{MCLK} max. and T_A max.
3. Based on device characterisation, device power consumption in STOP mode at T_A 25°C is predicted to be 30µA or less in 99.730020% of parts.
4. The conditions for these consumption measurements are described in application note AN2100.

On-chip peripherals

Table 15. Peripheral current consumption

Symbol	Parameter	Conditions	Typ	Unit
$I_{DD(PLL1)}$	PLL1 supply current	T_A= 25°C	3.42	mA
$I_{DD(PLL2)}$	PLL2 supply current		5.81	
$I_{DD(TIM)}$	TIM Timer supply current [1]	T_A= 25°C, f_{PCLK1}= f_{PCLK2}=33 MHz	0.88	
$I_{DD(BSPI)}$	BSPI supply current [2]		1.1	
$I_{DD(UART)}$	UART supply current [2]		1.05	
$I_{DD(I2C)}$	I2C supply current [2]		0.45	
$I_{DD(ADC)}$	ADC supply current when converting [5]		1.89	
$I_{DD(HDLC)}$	HDLC supply current [2]		1.82	
$I_{DD(USB)}$	USB supply current [2]		2.08	
$I_{DD(CAN)}$	CAN supply current [2]		1.11	

Notes:

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16MHz. No IC/OC programmed (no I/O pads toggling).
2. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

4.3.4 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electro magnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

In the case of an ARM7 CPU, in order to write robust code that can withstand all kinds of stress, such as very strong electromagnetic disturbance, it is mandatory that the Data Abort, Prefetch Abort and Undefined Instruction exceptions are managed by the application software. This will prevent the code going into an undefined state or performing any unexpected operation.

4.3.5 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{33} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 27. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage 1)	CMOS ports			$0.3V_{33}$	V
V_{IH}	Input high level voltage 1)		$0.7V_{33}$			
V_{hys}	Schmitt trigger voltage hysteresis 2)			0.8		V
V_{IL}	Input low level voltage 1)	P0.15 WAKEUP		0.9	0.8	V
V_{IH}	Input high level voltage 1)		2	1.35		
V_{hys}	Schmitt trigger voltage hysteresis 2)			0.4		V
V_{IL}	Input low level voltage 1)	TTL ports			0.8	V
V_{IH}	Input high level voltage 1)		2.0			
$I_{INJ(PIN)}$	Injected Current on any I/O pin				± 4	mA
$\Sigma I_{INJ(PIN)}$ 3)	Total injected current (sum of all I/O and control pins)				± 25	
I_{lkg}	Input leakage current 4)	$V_{SS} \le V_{IN} \le V_{33}$			±1	µA
R_{PU}	Weak pull-up equivalent resistor5)	$V_{IN}=V_{SS}$	110	150	700	kΩ
R_{PD}	Weak pull-down equivalent resistor5)	$V_{IN}=V_{33}$	110	150	700	kΩ
C_{IO}	I/O pin capacitance			5		pF

Notes:

1. Data based on characterization results, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
3. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{33}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Refer to *Section 4.2 on page 35* for more details.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. The R_{PU} pull-up and R_{PD} pull-down equivalent resistor are based on a resistive transistor (corresponding I_{PU} and I_{PD} current characteristics described in *Figure 18* to *Figure 19*).

Figure 17. R_{PU} vs. V_{33} with $V_{IN}=V_{SS}$

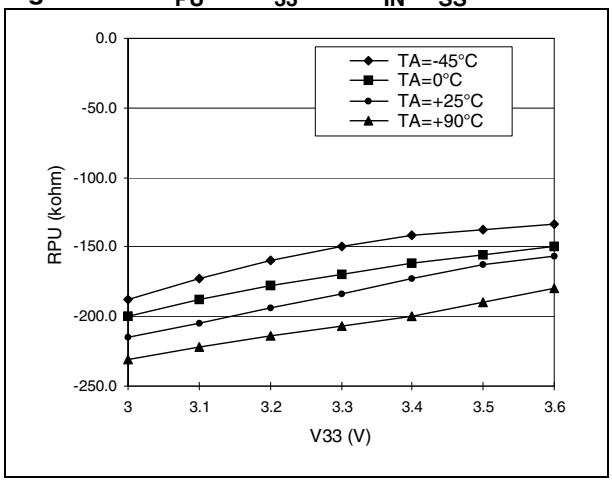


Figure 18. I_{PU} vs. V_{33} with $V_{IN}=V_{SS}$

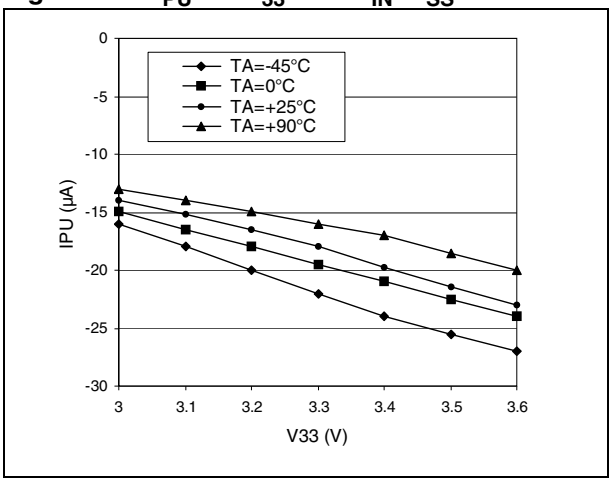


Figure 19. R_{PD} vs. V_{33} with $V_{IN}=V_{33}$

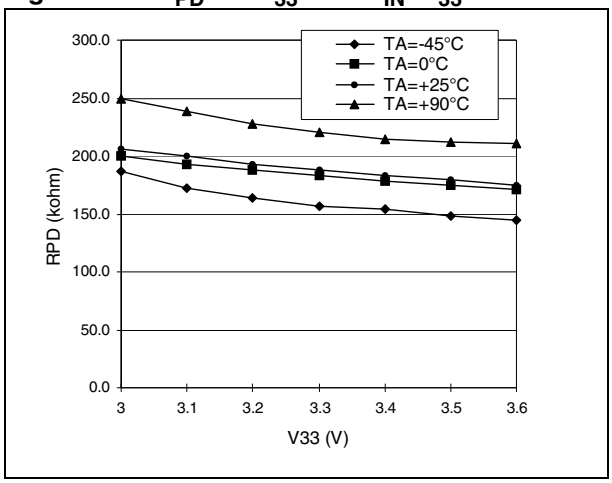
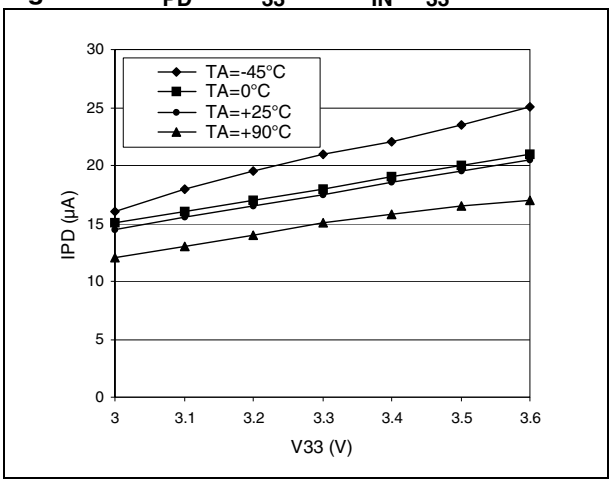


Figure 20. I_{PD} vs. V_{33} with $V_{IN}=V_{33}$



Output driving current

Subject to general operating conditions for V_{33} and T_A unless otherwise specified.

Table 28. Output driving current

I/O type	Symbol	Parameter	Conditions	Min	Max	Unit
Standard	V_{OL} 1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO}=+4mA		0.4	V
	V_{OH} 2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-4mA	V_{33}-0.8		
High Current	V_{OL} 1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO}=+8mA		0.4	
	V_{OH} 2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-8mA	V_{33}-0.8		

Notes:

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 9* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 9* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{V33}.

Figure 21. Typical V_{OL} and V_{OH} at V_{33}=3.3V (high current ports)

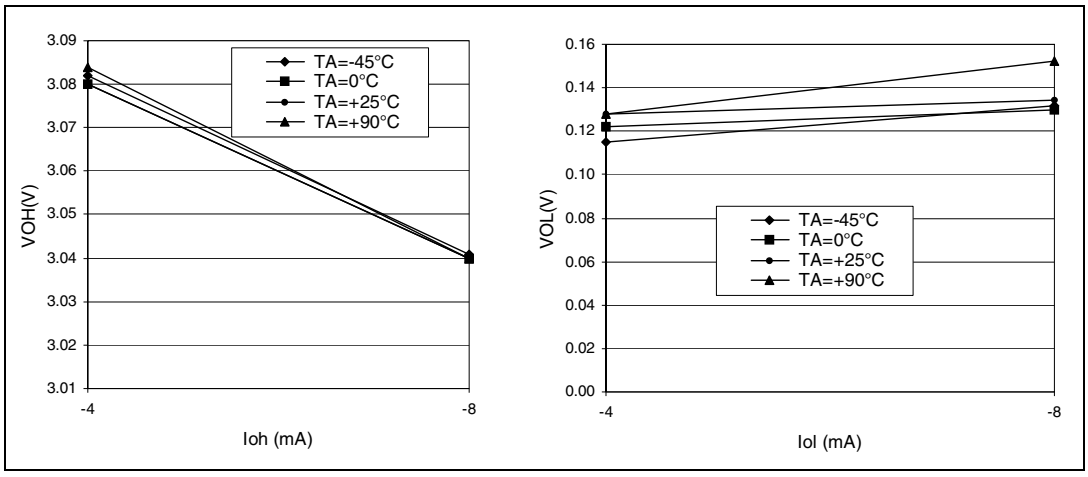


Table 32. EMI read operation

Symbol	Parameter	Test Conditions	Value			Unit
			Min[1)]	Typ	Max[1)]	
t_{RCR}	Read to CSn Removal Time	MCLK=50 MHz 4 wait states 50 pf load on all pins	19	t_{MCLK}	21	ns
t_{RP}	Read Pulse Time		98	t_C	100	ns
t_{RDS}	Read Data Setup Time		22			ns
t_{RDH}	Read Data Hold Time		0			ns
t_{RAS}	Read Address Setup Time		27	$1.5*t_{MCLK}$	33	ns
t_{RAH}	Read Address Hold Time		0.65		2	ns
t_{RAT}	Read Address Turnaround Time		1.9		3.25	ns
t_{RRT}	RDn Turnaround Time		20	t_{MCLK}	21	ns

See *Figure 25*, *Figure 26*, *Figure 27* and *Figure 28* for related timing diagrams.

1. Data based on characterisation results, not tested in production.

Table 33. EMI write operation

Symbol	Parameter	Test conditions	Value			Unit
			Min[1)]	Typ	Max[1)]	
t_{WCR}	WEn to CSn Removal Time	MCLK=50 MHz 3 wait states 50 pf load on all pins	20	t_{MCLK}	22.5	ns
t_{WP}	Write Pulse Time		77.5	t_C	80	ns
t_{WDS1}	Write Data Setup Time 1		97	$t_C + t_{MCLK}$	100	ns
t_{WDS2}	Write Data Setup Time 2		77	t_C	80	ns
t_{WDH}	Write Data Hold Time		20	t_{MCLK}	23	ns
t_{WAS}	Write Address Setup Time		27	$1.5*t_{MCLK}$	33	ns
t_{WAH}	Write Address Hold Time		0.6		3	ns
t_{WAT}	Write Address Turnaround Time		1.75		4.1	ns
t_{WWT}	WEn Turnaround Time		20	t_{MCLK}	23	ns

See *Figure 29*, *Figure 30*, *Figure 31* and *Figure 32* for related timing diagrams.

1. Data based on characterisation results, not tested in production.

Figure 33. Typical application with I²C bus and timing diagram

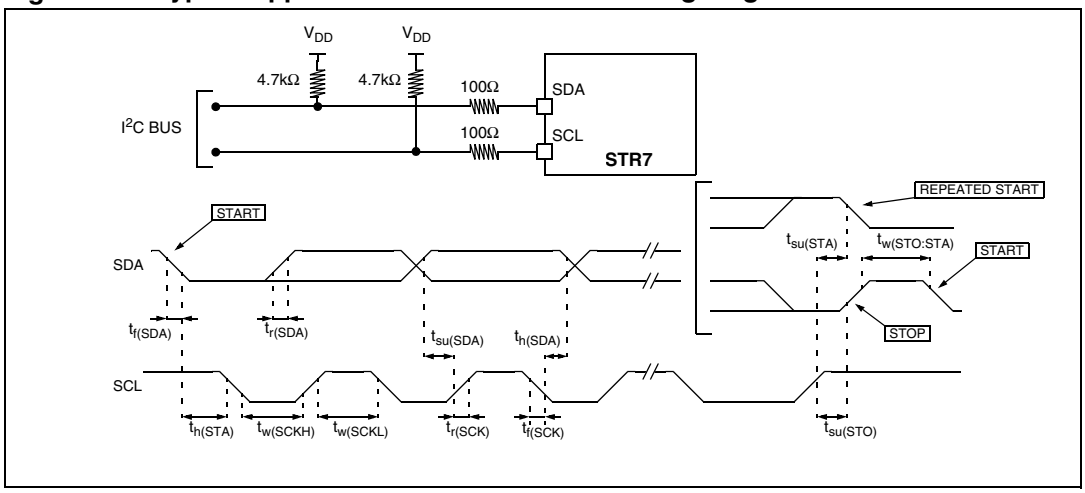


Table 35. SCL Frequency Table (f_{PCLK1}=8 MHz.,V_{33} = 3.3 V)

f_{SCL} (kHz)	I2CCCR Value
	R_P=4.7kΩ
400	83
300	85h
200	8Ah
100	24h
50	4Ch
20	C4h

Legend:

R_P = External pull-up resistance

f_{SCL} = I²C speed

NA = Not achievable

Note: For speeds around 200 kHz, achieved speed can have ± 5% tolerance

For other speed ranges, achieved speed can have ± 2% tolerance

The above variations depend on the accuracy of the external components used.

4.3.10 USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 37. USB startup time

Symbol	Parameter	Conditions	Max	Unit
$t_{STARTUP}$	USB transceiver startup time		1	µs

Table 38. USB DC characteristics

Symbol	Parameter	Conditions	Min.(1)(2)	Max.(1)(2)	Unit
Input Levels					
V_{DI}	Differential Input Sensitivity	I(DP, DM)	0.2		V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8	2.5	
V_{SE}	Single Ended Receiver Threshold		1.3	2.0	
Output Levels					
V_{OL}	Static Output Level Low	R_L of 1.5 kΩ to 3.6V(3)		0.3	V
V_{OH}	Static Output Level High	R_L of 15 kΩ to V_{SS}(3)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. It is important to be aware that the DP/DM pins are not 5 V tolerant. As a consequence, in case of a a shortcut with Vbus (typ: 5.0V), the protection diodes of the DP/DM pins will be direct biased . This will not damage the device if not more than 50 mA is sunk for longer than 24 hours but the reliability may be affected.
3. R_L is the load connected on the USB drivers

Figure 37. USB: data signal rise and fall time

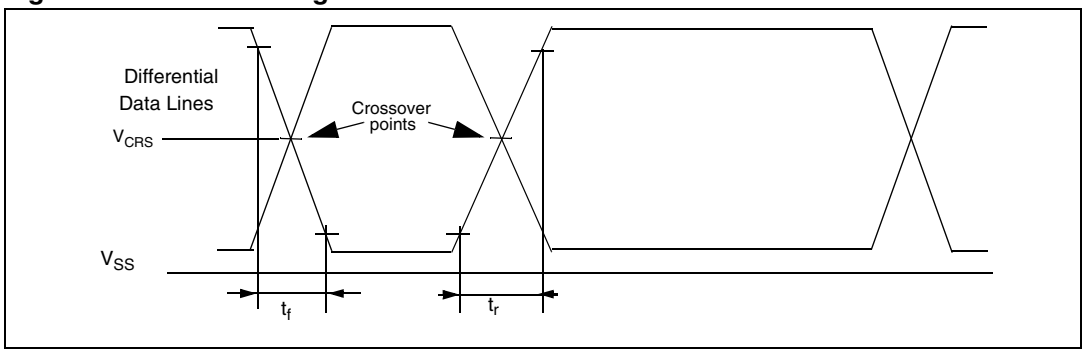


Table 39. USB: Full speed driver electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time(1)	C_L=50 pF	4	20	ns
t_f	Fall Time1)	C_L=50 pF	4	20	ns
t_{rfm}	Rise/ Fall Time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal Crossover Voltage		1.3	2.0	V

1. Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification - Chapter 7 (version 2.0).

Figure 47. BGA144 STR710 version “Z”

Figure 48. BGA64 STR711 version “X”

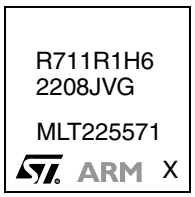


Table 43. A, Z and X version differences

Feature	A version	Z version	X version
ARM7TDMI core device Identification (ID) code register (see ARM7TDMI Technical Reference Manual)	Version bits [31:28] = 0001	Version bits [31:28] = 0010	Version bits [31:28] = 0010
Low power mode consumption in STOP mode at 25 °C	Not guaranteed Typical 49 µA	50 µA maximum at 25°C. Less than 30 µA at 25 °C for 99.730020% of parts	Same as Z.
SC.DATA pin	Not TRUE open drain When addressing 5V cards, the SCDATA Line must be connected to an open drain buffer.		Pin P0.10/U1.RX/U1.TX/SC.DATA has been modified to offer TRUE OPEN DRAIN functionality when in Smartcard mode. When addressing 5V cards, the SCDATA line can now be connected directly to the card I/O. This modification is backward compatible with previous designs, and no board modification is required.

9 Revision history

Table 44. Document revision history

Date	Revision	Changes
17-Mar-2004	1	First Release
05-Apr-2004	2	Updated “Electrical parameters” on page 34
08-Apr-2004	2.1	Corrected STR712F Pinout. Pins 43/42 swapped.
15-Apr-2004	2.2	PDF hyperlinks corrected.
7-Jul-2004	3	Corrected description of STDBY, V18, VSS18 V18BKP VSSBKP pins Added IDDrun typical data Updated BSPI max. baudrate. Updated “EMI - external memory interface” on page 56
29-Oct-2004	4	Corrected Flash sector B1F0/F1 address in *Figure 6: Memory map on page 31* Corrected *Table 5 on page 25* LQFP64 TEST pin is 16 instead of 17. Added to TQPFP64 column: pin 7 BOOTEN, pin 17 $V_{33IO-PLL}$ Changed description of JTCK from ‘External pull-down required’ to ‘External pull-up or pull down required’.
25-Jan-2005	5	Changed “Product Preview” to “Preliminary Data” on page 1 and 3 Renamed ‘PU/PD’ column to ‘Reset state’ in *Table 5 on page 25* Added reference to STR7 Flash Programming Reference Manual
19-Apr-2005	6	Added STR715F devices and modified RAM size of STR71xF1 devices Added BGA package in *Section 5* Updated ordering information in *Section 7*. Added PLL duty cycle min and max. in *PLL electrical characteristics on page 45*
13-Oct-2005	7	Updated feature description on page 1 Update overview *Section 1.1* Added OD/PP to P0.12 in *Table 5* Changed name of WFI mode to WAIT mode Changed Memory Map *Table 6*: Ext. Memory changed to 64 MB and flash register changed to 36 bytes. Added Power Consumption *Table 13* Modified BGA144 F3, F5, F12 and G12 in *Table 3* and *Table 4* Update EMI Timing *Table 24* and *Figure 29*