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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, HDLC, I²C, SmartCard, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8 + 16K)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str712fr0t6

Flexible power management

To minimize power consumption, you can program the STR71x to switch to SLOW, WAIT, LPWAIT (low power wait), STOP or STANDBY mode depending on the current system activity in the application.

Flexible clock control

Two external clock sources can be used, a main clock and a 32 kHz backup clock. The embedded PLL allows the internal system clock (up to 66 MHz) to be generated from a main clock frequency of 16 MHz or less. The PLL output frequency can be programmed using a wide selection of multipliers and dividers. The microcontroller core, APB1 and APB2 peripherals are in separate clock domains and can be programmed to run at different frequencies during application runtime. The clock to each peripheral is gated with an individual control bit to optimize power usage by turning off peripherals any time they are not required.

Voltage regulators

The STR71x requires an external 3.0-3.6V power supply. There are two internal Voltage Regulators for generating the 1.8V power supply for the core and peripherals. The main VR is switched off during low power operation.

Low voltage detectors

Both the Main Voltage Regulator and the Low Power Voltage Regulator contain each a low voltage detection circuitry which keep the device under reset when the corresponding controlled voltage value (V_{18} or V_{18BKP}) falls below 1.35V (+/- 10%). This enhances the security of the system by preventing the MCU from going into an unpredictable state.

An external reset circuit must be used to provide the RESET at V_{33} power-up. It is not sufficient to rely on the RESET generated by the LVD in this case. This is because LVD operation is guaranteed only when V_{33} is within the specification.

3.1 On-chip peripherals

CAN interface (STR710 and STR712)

The CAN module is compliant with the CAN specification V2.0 part B (active). The bit rate can be programmed up to 1 MBaud.

USB interface (STR710 and STR711)

The full-speed USB interface is USB V2.0 compliant and provides up to 16 bidirectional/32 unidirectional endpoints, up to 12 Mb/s (full-speed), support for bulk transfer, isochronous transfers and USB Suspend/Resume functions.

Standard timers

Each of the four timers have a 16-bit free-running counter with 7-bit prescaler

Three timers each provide up to two input capture/output compare functions, a pulse counter function, and a PWM channel with selectable frequency.

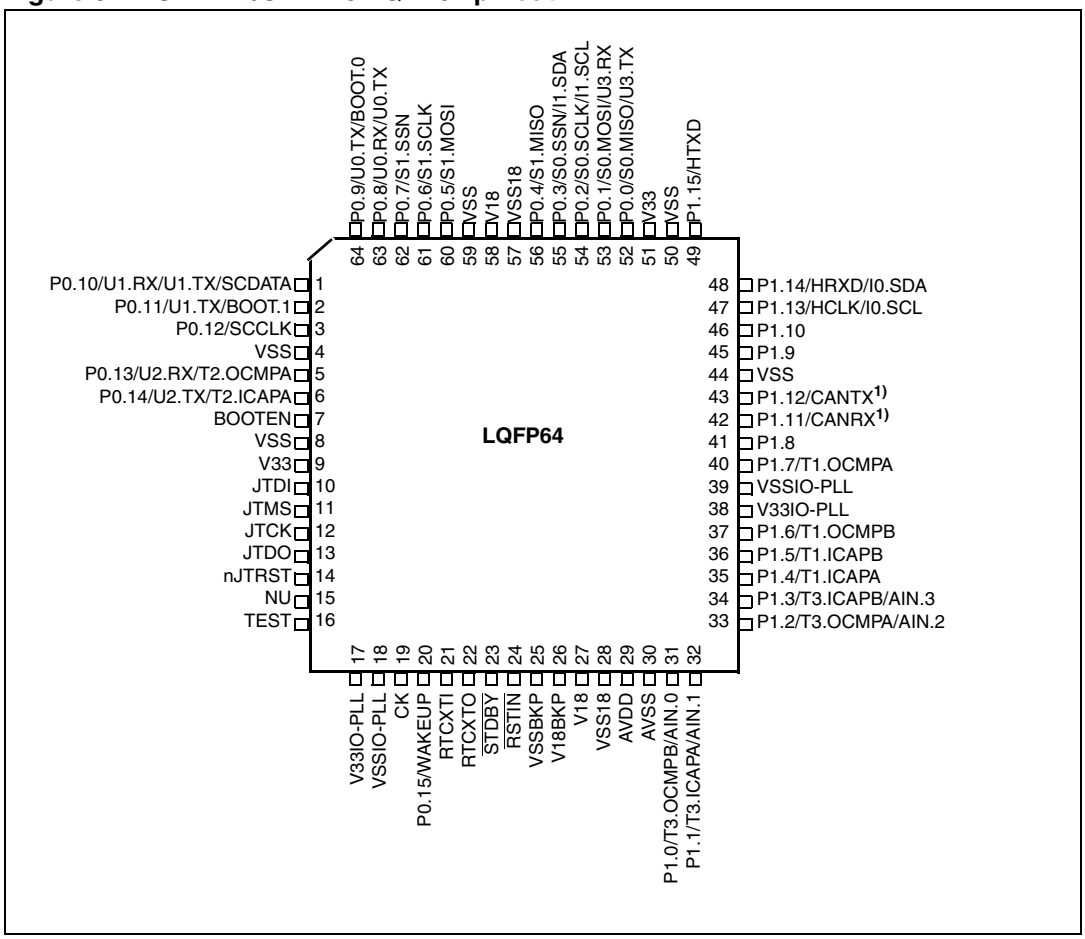
The fourth timer is not connected to the I/O ports. It can be used by the application software for general timing functions.

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
1	A1	P0.10/U1.RX/ U1.TX/ SC.DATA	I/O	pd	C_T	X	4mA	T			Port 0.10	UART1: Receive Data input	UART1: Transmit data output.
												Note: This pin may be used for Smartcard DataIn/DataOut or single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress	
2	B2	$\overline{RD}$	O	5)					X		External Memory Interface: Active low read signal for external memory. It maps to the OE_N input of the external components.		
3	C2	P0.11/BOOT.1 /U1.TX	I/O	pd	C_T		4mA	X	X		Port 0.11	Select Boot Configuration input	UART1: Transmit data output.
4	C3	P0.12/SC.CLK	I/O	pd	C_T		4mA	X	X		Port 0.12	Smartcard reference clock output	
5	D1	V_{SS}	S								Ground voltage for digital I/Os[4]		
6	D2	V_{33}	S								Supply voltage for digital I/Os[4]		
7	B1	P2.0/$\overline{CS}$.0	I/O	8)	C_T		8mA	X	X		Port 2.0	External Memory Interface: Select Memory Bank 0 output **Note:** This pin is forced to output push-pull 1 mode at reset to allow boot from external memory	
8	C1	P2.1/$\overline{CS}$.1	I/O	pu 2)	C_T		8mA	X	X		Port 2.1	External Memory Interface: Select Memory Bank 1 output	
9	D3	P0.13/U2.RX/ T2.OCMPA	I/O	pu	C_T	X	4mA	X	X		Port 0.13	UART2: Receive Data input	Timer2: Output Compare A output
10	D4	P0.14/U2.TX/ T2.ICAPA	I/O	pu	C_T		4mA	X	X		Port 0.14	UART2: Transmit data output	Timer2: Input Capture A input
11	E1	P2.2/$\overline{CS}$.2	I/O	pu 2)	C_T		8mA	X	X		Port 2.2	External Memory Interface: Select Memory Bank 2 output	
12	E2	P2.3/$\overline{CS}$.3	I/O	pu 2)	C_T		8mA	X	X		Port 2.3	External Memory Interface: Select Memory Bank 3 output	

3.4 Pin description for 64-pin packages

Figure 3. STR712/STR715 LQFP64 pinout

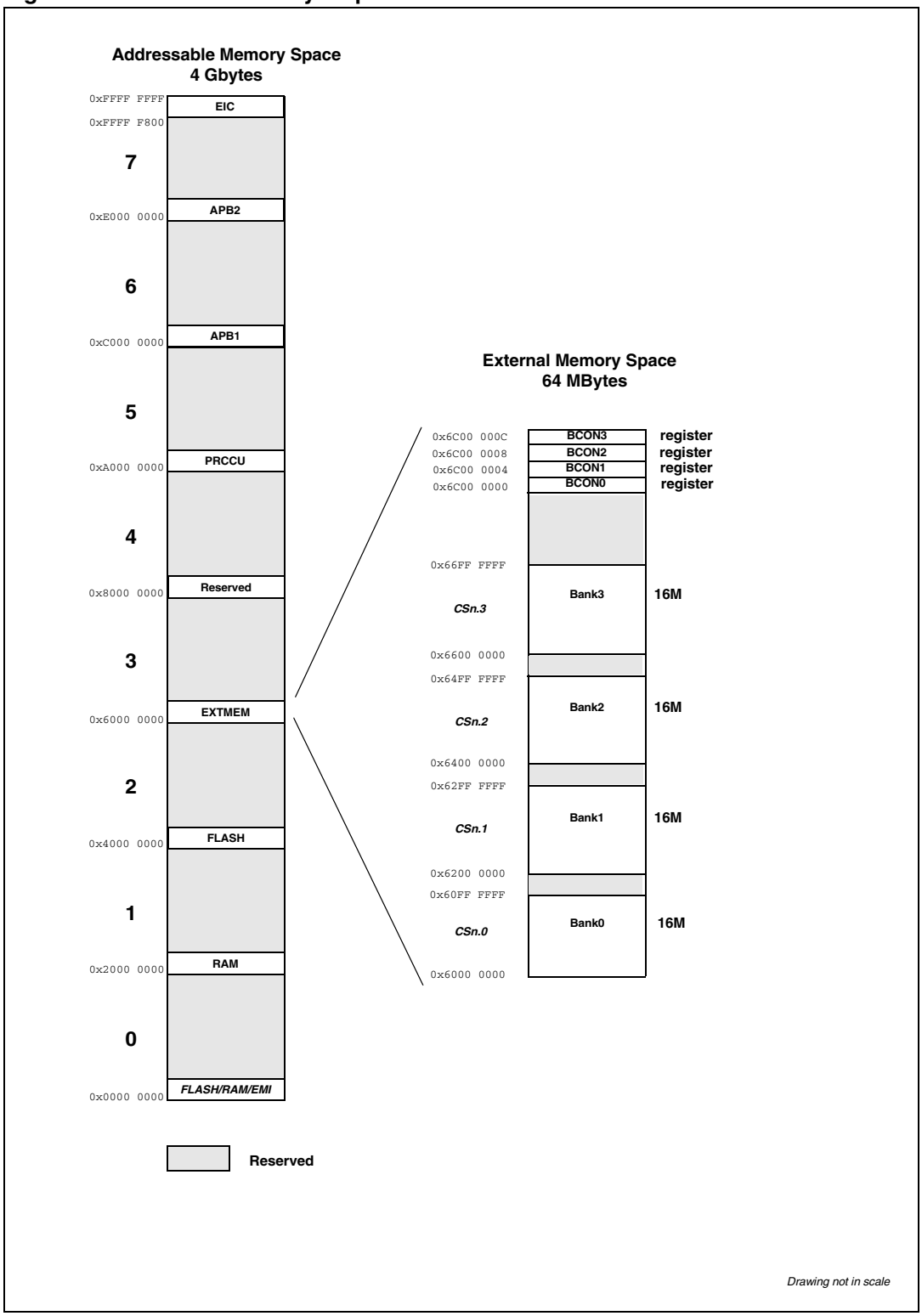


1. CANTX and CANRX in STR712F only, in STR715F they are general purpose I/Os.

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
36	P1.5/T1.ICAPB	I/O	pu	C_T		4mA	X	X		Port 1.5	Timer 1: Input Capture B	
37	P1.6/T1.OCMPB	I/O	pu	C_T		4mA	X	X		Port 1.6	Timer 1: Output Compare B	
38	$V_{33IO-PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference[2]		
39	$V_{SSIO-PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[2]		
40	P1.7/T1.OCMPA	I/O	pu	C_T		4mA	X	X		Port 1.7	Timer 1: Output Compare A	
41	P1.8	I/O	pd	C_T		4mA	X	X		Port 1.8		
42	P1.11/CANRX	I/O	pu	C_T	X	4mA	X	X		Port 1.11	CAN: receive data input **Note:** On STR710 and STR712 only	
43	P1.12/CANTX	I/O	pu	C_T		4mA	X	X		Port 1.12	CAN: Transmit data output **Note:** On STR710 and STR712 only	
42	USBDP	I/O		C_T						USB bidirectional data (data +). Reset state = HiZ **Note:** On STR710 and STR711 only This pin requires an external pull-up to V_{33} to maintain a high level.		
43	USBDN	I/O		C_T						USB bidirectional data (data -). Reset state = HiZ **Note:** On STR710 and STR711 only.		
44	V_{SS}	S								Ground voltage for digital I/O circuitry[2]		
45	P1.9	I/O	pd	C_T		4mA	X	X		Port 1.9		
46	P1.10/USBCLK	I/O	pd	C/T		4mA	X	X		Port 1.10	USB: 48 MHZ clock input	
47	P1.13/HCLK/I0.SCL	I/O	pd	C_T	X	4mA	X	X		Port 1.13	HDLC: reference clock input	I2C clock
48	P1.14/HRXD/I0.SDA	I/O	pu	C_T	X	4mA	X	X		Port 1.14	HDLC: Receive data input	I2C serial data
49	P1.15/HTXD	I/O	pu	C_T		4mA	X	X		Port 1.15	HDLC: Transmit data output	
50	V_{SS}	S								Ground voltage for digital I/O circuitry[2]		
51	V_{33}	S								Supply voltage for digital I/O circuitry[2]		

Figure 8. External memory map



4.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{33}- V_{SS}	External 3.3V Supply voltage (including AV_{DD} and $V_{33IO-PLL}$)[2]	-0.3	4.0	V
V_{18BKP} - V_{SSBKP}	Digital 1.8V Supply voltage on V_{18BKP} backup supply [2]	-0.3	2.0	
V_{IN}	Input voltage on true open drain pin (P0.10) [1]	V_{SS}-0.3	+5.5	
	Input voltage on any other pin [1]	V_{SS}-0.3	V_{33}+0.3	
$\|\Delta V_{33x}\|$	Variations between different 3.3V power pins	50	50	mV
$\|\Delta V_{18x}\|$	Variations between different 1.8V power pins [5]	25	25	
$\|V_{SSX}$ - $V_{SS}\|$	Variations between all the different ground pins	50	50	
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	see *: Absolute maximum ratings (electrical sensitivity) on page 49*		
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)			

Table 14. Typical power consumption data

Symbol	Parameter		Conditions	Typical current on V33	Unit
I_{DDRUN}	RUN mode current from RAM	All periphs ON	MCLK = 16 MHz, PCLK1 = PCLK2 = 16 MHz	23	mA
			MCLK = 32 MHz, PCLK1 = PCLK2 = 32 MHz	40	
			MCLK = 48 MHz, PCLK1 = PCLK2 = 24 MHz	50	
			MCLK = 64 MHz, PCLK1 = PCLK2 = 32 MHz	63	
		All periphs OFF	MCLK = 16 MHz	16	
			MCLK = 32 MHz	26	
			MCLK = 48 MHz	39	
			MCLK = 64 MHz	48	
	RUN mode current from FLASH	All periphs ON	MCLK = 16 MHz, PCLK1 = PCLK2 = 16 MHz	27	
			MCLK = 32 MHz, PCLK1 = PCLK2 = 32 MHz	47	
			MCLK = 48 MHz, PCLK1 = PCLK2 = 24 MHz	62	
		All periphs OFF	MCLK = 16 MHz	21	
			MCLK = 32 MHz	36	
			MCLK = 48 MHz	53	
I_{DDSLOW}	SLOW mode current		MCLK = CK_AF (32 kHz), MVR off	1.7	
I_{DDWAIT}	WAIT mode current (all periphs ON)		PCLK1 = PCLK2 = 1 MHz	13	
$I_{DDLPWAIT}$	LPWAIT mode current		CK_AF (32 kHz), Main VReg off, FLASH in power-down	37	µA
I_{DDSTOP}	STOP mode current		Main VReg off, FLASH in power down, RTC on	18	
			Main VReg off, FLASH in power down, RTC off	10	
I_{DDSB}	STANDBY mode current		LP VReg on, LVD on, RTC on	10	
			LP VReg off (ext 1.8V on V18BKP), LVD on, RTC on	9	
			LP VReg off (ext1.8V on V18BKP), LVD off, RTC on	5	
			LP VReg off (ext 1.8V on V18BKP), LVD off, RTC off	1	

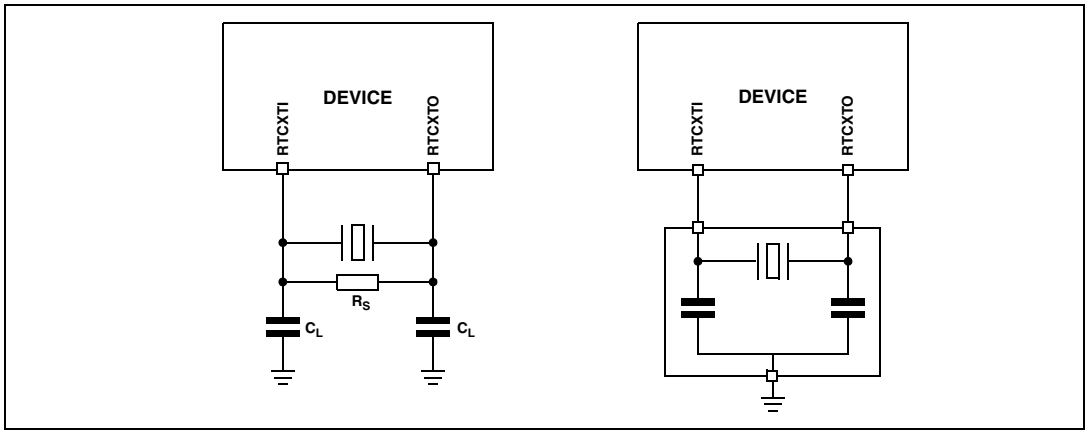
Table 17. RTCXT1 external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RTCXT1}	External clock source frequency		0		500	kHz
$V_{RTCXT1H}$	RTCXT1 input pin high level voltage		$0.7xV_{33}$		V_{33}	V
$V_{RTCXT1L}$	RTCXT1 input pin low level voltage		V_{SS}		$0.3xV_{33}$	
$t_{w(RTCXT1)}$ $t_{w(RTCXT1)}$	RTCXT1 high or low time [1]		100			ns
$t_{r(RTCXT1)}$ $t_{f(RTCXT1)}$	RTCXT1 rise or fall time [1]				5	
$C_{IN(RTCXT1)}$	RTCXT1 input capacitance[1]			5		pF
DuCy(RTCXT1)	Duty cycle		30		70	%
I_L	RTCXT1 Input leakage current	$V_{SS} \le V_{IN} \le V_{33}$			±1	µA

Notes:

1. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 16. RTC crystal oscillator and resonator



PLL electrical characteristics

V_{33} = 3.0 to 3.6V, $V_{33IOPLL}$ = 3.0 to 3.6V, T_A = -40 / 85 °C unless otherwise specified.

Table 19. PLL1 characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$f_{PLLCLK1}$	PLL multiplier output clock				165	MHz
f_{PLL1}	PLL input clock	FREF_RANGE = 0	1.5		3.0	MHz
		FREF_RANGE = 1 MX[1:0]='00' or '01'	3.0		8.25	MHz
		FREF_RANGE = 1 MX[1:0]='10' or '11'	3.0		6	MHz
	PLL input clock duty cycle		25		75	%
f_{FREE1}	PLL free running frequency	FREF_RANGE = 0 MX[1:0]='01' or '11'		125		kHz
		FREF_RANGE = 0 MX[1:0]='00' or '10'		250		kHz
		FREF_RANGE = 1 MX[1:0]='01' or '11'		250		kHz
		FREF_RANGE = 1 MX[1:0]='00' or '10'		500		kHz
t_{LOCK1}	PLL lock time	FREF_RANGE = 0 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			300	µs
		FREF_RANGE = 1 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			600	µs

Table 19. PLL1 characteristics (continued)

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$\Delta t_{JITTER1}$	PLL jitter (peak to peak)	t_{PLL} = 4 MHz, MX[1:0]='11' Global Output division = 32 (Output Clock = 2 MHz)		0.7	2	ns

Table 20. PLL2 characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$f_{PLLCLK2}$	PLL multiplier output clock				140	MHz
f_{PLL2}	PLL input clock	FREF_RANGE = 0	1.5		3.0	MHz
		FREF_RANGE = 1	3.0		5	MHz
t_{LOCK2}	PLL lock time	FREF_RANGE = 0 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			300	µs
		FREF_RANGE = 1 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			600	µs
$\Delta t_{JITTER2}$	PLL jitter (peak to peak)	t_{PLL} = 4 MHz, MX[1:0]='11' Global Output division = 32 (Output Clock = 2 MHz)		0.7	2	ns

Table 21. Low-power mode wakeup timing

Symbol	Parameter	Typ	Unit
$t_{WULPWFI}$	Wakeup from LPWFI mode	26(1)	µs
t_{WUSTOP}	Wakeup from STOP mode	2048	CLK Cycles (2)
t_{WUSTBY}	Wakeup from STANDBY mode	2048 CLK Cycles + 8 CLK2 Cycles(3)	Cycles

1. Clock selected is CK2_16, Main VReg OFF and Flash in power-down
2. The CLK clock is derived from the external oscillator.
3. Refer to Figure 7. Reset General Timing in the STR71xF Reference Manual (UM0084)

4.3.3 Memory characteristics

Flash memory

V_{33} = 3.0 to 3.6V, T_A = -40 to 85 °C unless otherwise specified.

Table 22. Flash memory characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ	Max[1]	
t_{PW}	Word Program			40		µs
t_{PDW}	Double Word Program			60		µs
t_{PB0}	Bank 0 Program (256K)	Double Word Program		1.6	2.1	s
t_{PB1}	Bank 1 Program (16K)	Double Word Program		130	170	ms
t_{ES}	Sector Erase (64K)	Not preprogrammed Preprogrammed		2.3 1.9	4.0 3.3	s
t_{ES}	Sector Erase (8K)	Not preprogrammed Preprogrammed		0.7 0.6	1.1 1.0	s
t_{ES}	Bank 0 Erase (256K)	Not preprogrammed Preprogrammed		8.0 6.6	13.7 11.2	s
t_{ES}	Bank 1 Erase (16K)	Not preprogrammed Preprogrammed		0.9 0.8	1.5 1.3	s
t_{RPD}[2]	Recovery when disabled				20	µs
t_{PSL}[2]	Program Suspend Latency				10	µs
t_{ESL}[2]	Erase Suspend Latency				300	µs
N_{END_B0}	Endurance (Bank 0 sectors)		10			kcycles
N_{END_B1}	Endurance (Bank 1 sectors)		100			kcycles
t_{RET}	Data Retention (Bank 0 and Bank 1)	T_A=85°	20			Years
t_{ESR}	Erase Suspend Rate	Min time from Erase Resume to next Erase Suspend	20			ms

Notes:

1. T_A=45°C after 0 cycles. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production

Table 25. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value [1]	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25°C	2000	V
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)		200	
$V_{ESD(CDM)}$	Electro-static discharge voltage (Charge Device Model)		750 on corner pins, 500 on others	

Notes:

1. Data based on characterization results, not tested in production.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Electrical sensitivities

Table 26. Static and dynamic latch-up

Symbol	Parameter	Conditions	Class[1]
LU	Static latch-up class	T_A=+25°C T_A=+85°C T_A=+105°C	A A A
DLU	Dynamic latch-up class	V_{DD}=3.3 V, f_{OSC4M}=4 MHz, f_{MCLK}=32 MHz, T_A=+25°C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

Figure 17. R_{PU} vs. V_{33} with $V_{IN}=V_{SS}$

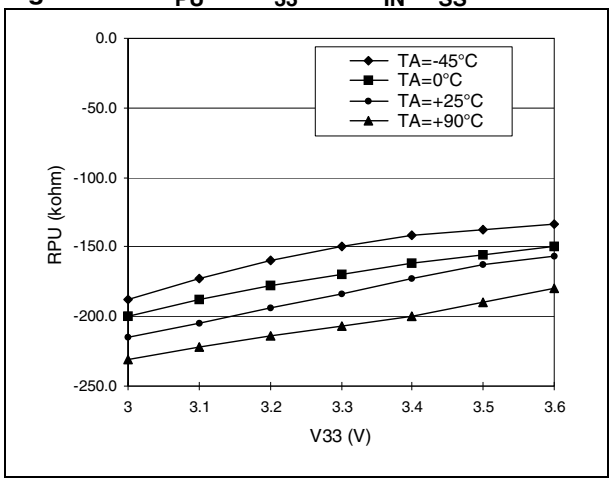


Figure 18. I_{PU} vs. V_{33} with $V_{IN}=V_{SS}$

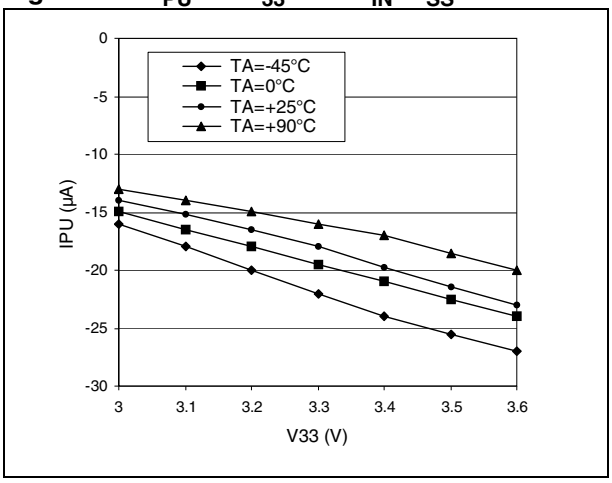


Figure 19. R_{PD} vs. V_{33} with $V_{IN}=V_{33}$

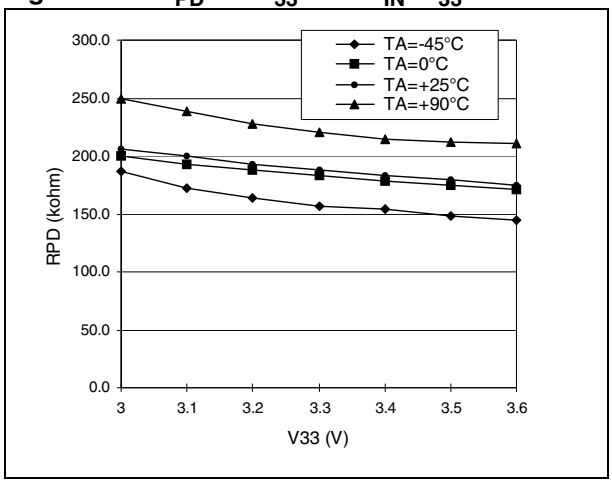


Figure 20. I_{PD} vs. V_{33} with $V_{IN}=V_{33}$

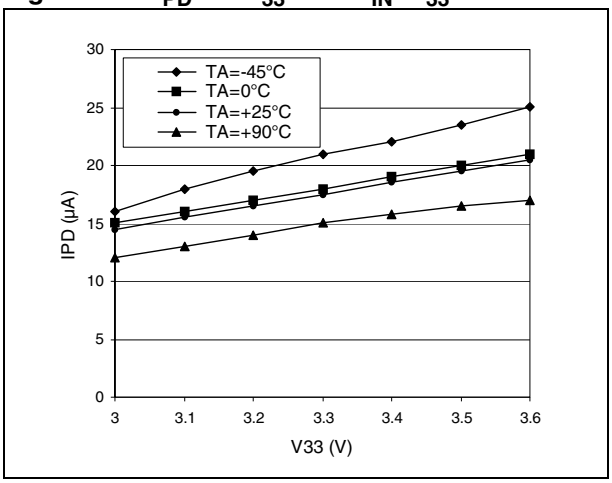


Table 32. EMI read operation

Symbol	Parameter	Test Conditions	Value			Unit
			Min[1)]	Typ	Max[1)]	
t_{RCR}	Read to CSn Removal Time	MCLK=50 MHz 4 wait states 50 pf load on all pins	19	t_{MCLK}	21	ns
t_{RP}	Read Pulse Time		98	t_C	100	ns
t_{RDS}	Read Data Setup Time		22			ns
t_{RDH}	Read Data Hold Time		0			ns
t_{RAS}	Read Address Setup Time		27	$1.5*t_{MCLK}$	33	ns
t_{RAH}	Read Address Hold Time		0.65		2	ns
t_{RAT}	Read Address Turnaround Time		1.9		3.25	ns
t_{RRT}	RDn Turnaround Time		20	t_{MCLK}	21	ns

See *Figure 25*, *Figure 26*, *Figure 27* and *Figure 28* for related timing diagrams.

1. Data based on characterisation results, not tested in production.

Table 33. EMI write operation

Symbol	Parameter	Test conditions	Value			Unit
			Min[1)]	Typ	Max[1)]	
t_{WCR}	WEn to CSn Removal Time	MCLK=50 MHz 3 wait states 50 pf load on all pins	20	t_{MCLK}	22.5	ns
t_{WP}	Write Pulse Time		77.5	t_C	80	ns
t_{WDS1}	Write Data Setup Time 1		97	$t_C + t_{MCLK}$	100	ns
t_{WDS2}	Write Data Setup Time 2		77	t_C	80	ns
t_{WDH}	Write Data Hold Time		20	t_{MCLK}	23	ns
t_{WAS}	Write Address Setup Time		27	$1.5*t_{MCLK}$	33	ns
t_{WAH}	Write Address Hold Time		0.6		3	ns
t_{WAT}	Write Address Turnaround Time		1.75		4.1	ns
t_{WWT}	WEn Turnaround Time		20	t_{MCLK}	23	ns

See *Figure 29*, *Figure 30*, *Figure 31* and *Figure 32* for related timing diagrams.

1. Data based on characterisation results, not tested in production.

Figure 31. Write cycle timing: 16-bit write on 8-bit memory

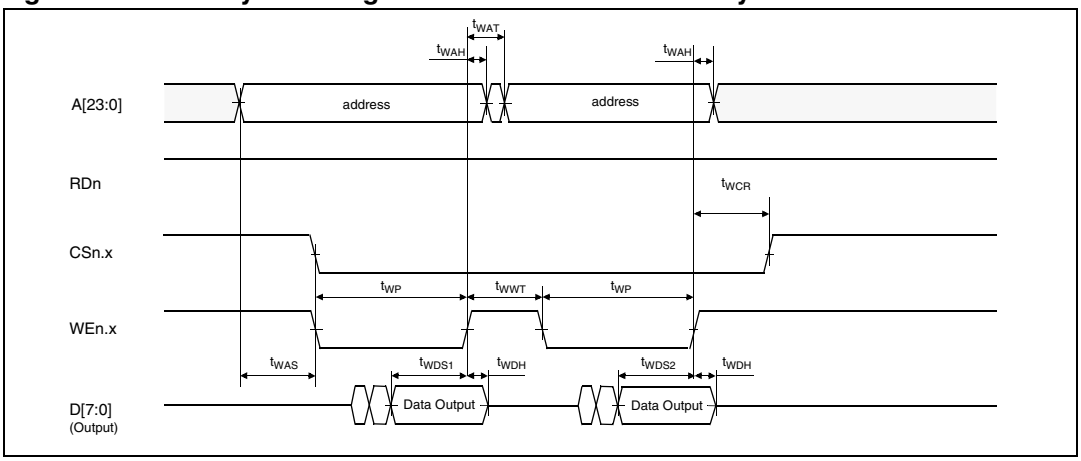
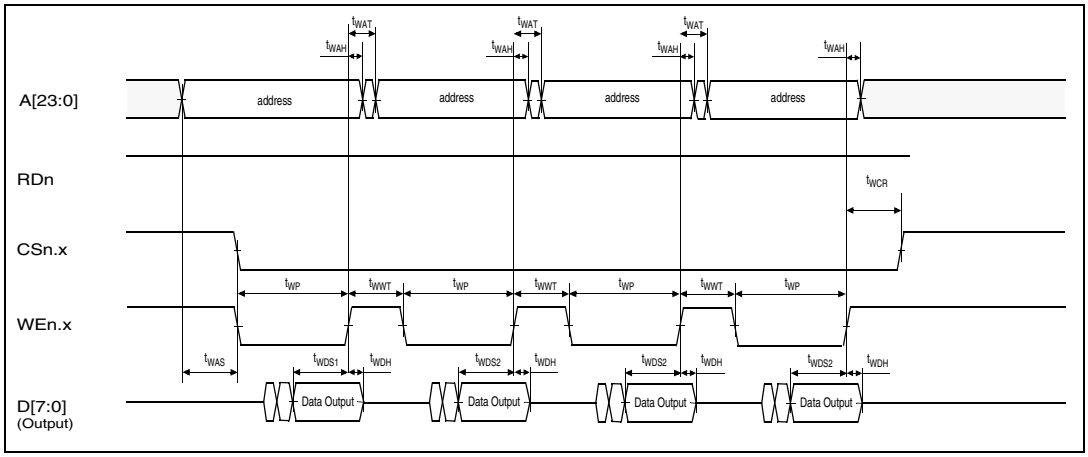


Figure 32. Write cycle timing: 32-bit write on 8-bit memory



See *Table 33* for write timing data.

4.3.8 I²C - inter IC control interface

Subject to general operating conditions for V_{33}, f_{PCLK1}, and T_A unless otherwise specified.

The STR7 I²C interface meets the requirements of the Standard I²C communications protocol described in the following table with the restriction mentioned below:

Note: ***Restriction:*** *The I/O pins which SDA and SCL are mapped to are not "True" Open-Drain: when configured as open-drain, the PMOS connected between the I/O pin and V_{33} is disabled, but it is still present. Also, there is a protection diode between the I/O pin and V_{33}. Consequently, when using this I²C in a multi-master network, it is not possible to power off the STR7X while some another I²C master node remains powered on: otherwise, the STR7X will be powered by the protection diode.*

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

4.3.10 USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 37. USB startup time

Symbol	Parameter	Conditions	Max	Unit
$t_{STARTUP}$	USB transceiver startup time		1	µs

Table 38. USB DC characteristics

Symbol	Parameter	Conditions	Min.(1)(2)	Max.(1)(2)	Unit
Input Levels					
V_{DI}	Differential Input Sensitivity	I(DP, DM)	0.2		V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8	2.5	
V_{SE}	Single Ended Receiver Threshold		1.3	2.0	
Output Levels					
V_{OL}	Static Output Level Low	R_L of 1.5 kΩ to 3.6V(3)		0.3	V
V_{OH}	Static Output Level High	R_L of 15 kΩ to V_{SS}(3)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. It is important to be aware that the DP/DM pins are not 5 V tolerant. As a consequence, in case of a a shortcut with Vbus (typ: 5.0V), the protection diodes of the DP/DM pins will be direct biased . This will not damage the device if not more than 50 mA is sunk for longer than 24 hours but the reliability may be affected.
3. R_L is the load connected on the USB drivers

Figure 37. USB: data signal rise and fall time

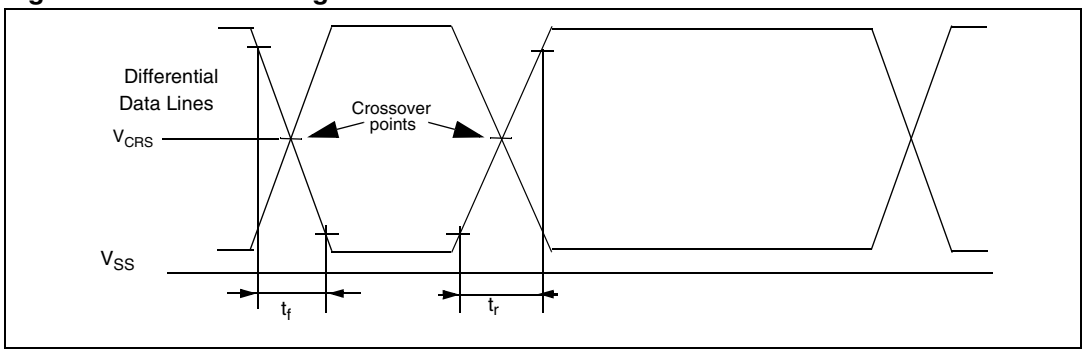
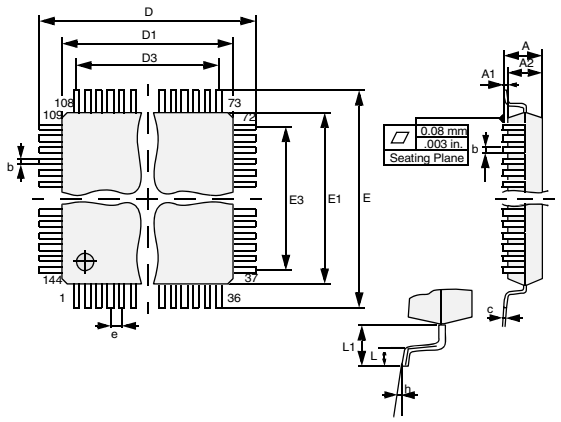


Table 39. USB: Full speed driver electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time(1)	C_L=50 pF	4	20	ns
t_f	Fall Time1)	C_L=50 pF	4	20	ns
t_{rfm}	Rise/ Fall Time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal Crossover Voltage		1.3	2.0	V

1. Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification - Chapter 7 (version 2.0).

Figure 41. 144-Pin low profile quad flat package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053		0.057
b	0.17	0.22	0.27	0.007		0.011
c	0.09		0.20	0.004		0.008
D	21.80	22.00	22.20	0.858	0.867	0.874
D1	19.80	20.00	20.20	0.780	0.787	0.795
D3		17.50			0.689	
E	21.80	22.00	22.20	0.858	0.867	0.874
E1	19.80	20.00	20.20	0.780	0.787	0.795
E3		17.50			0.689	
e		0.50			0.020	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	144					

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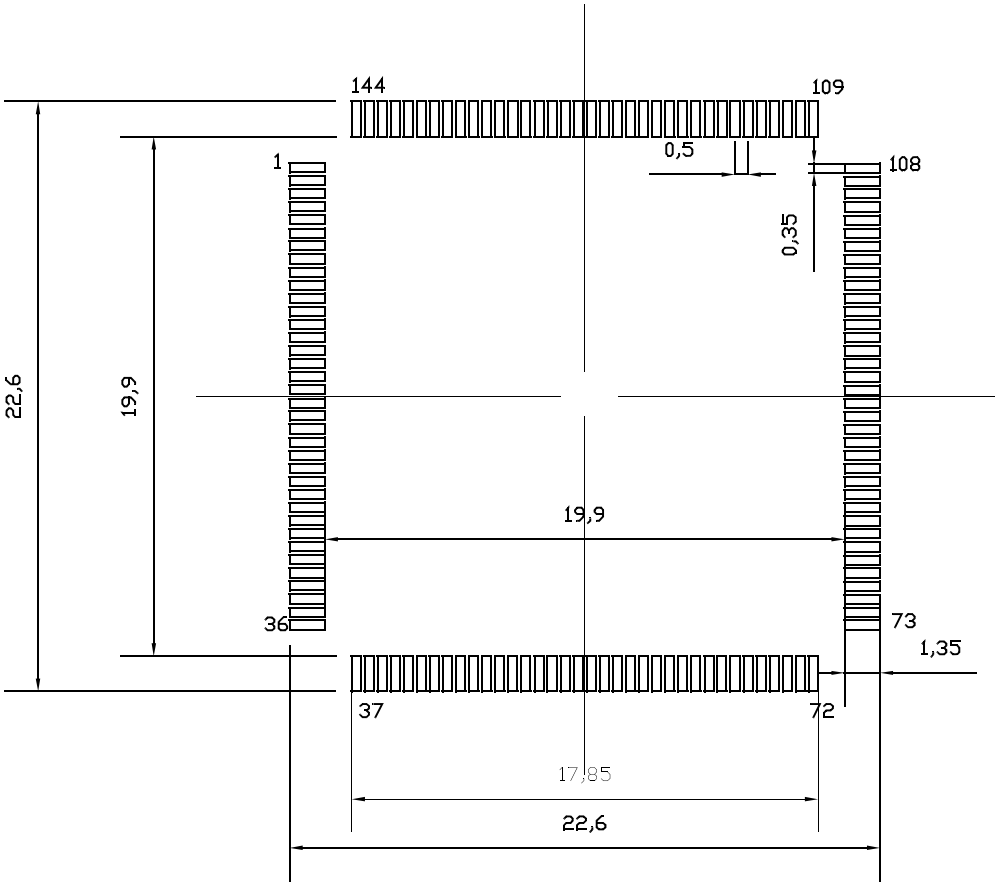
1.Values in inches are converted from mm and rounded to 3 decimal digits.

Recommended footprint (dimensions in mm)



8 Known limitations

Description

If an IRQ or FIQ interrupt is pending and the Interrupt vector register (EIC_IVR) is not yet read, the HALT bit in the RCCU_SMR register can not be written. Therefore a software reset can not be generated.

Workaround

To generate a software reset when an IRQ or FIQ line is pending, either:

- reset the EIC peripheral by setting bit 14 in the APB2_SWRES register, or
- read the EIC_IVR register prior to generating a software reset.

9 Revision history

Table 44. Document revision history

Date	Revision	Changes
17-Mar-2004	1	First Release
05-Apr-2004	2	Updated “Electrical parameters” on page 34
08-Apr-2004	2.1	Corrected STR712F Pinout. Pins 43/42 swapped.
15-Apr-2004	2.2	PDF hyperlinks corrected.
7-Jul-2004	3	Corrected description of STDBY, V18, VSS18 V18BKP VSSBKP pins Added IDDrun typical data Updated BSPI max. baudrate. Updated “EMI - external memory interface” on page 56
29-Oct-2004	4	Corrected Flash sector B1F0/F1 address in *Figure 6: Memory map on page 31* Corrected *Table 5 on page 25* LQFP64 TEST pin is 16 instead of 17. Added to TQPFP64 column: pin 7 BOOTEN, pin 17 $V_{33IO-PLL}$ Changed description of JTCK from ‘External pull-down required’ to ‘External pull-up or pull down required’.
25-Jan-2005	5	Changed “Product Preview” to “Preliminary Data” on page 1 and 3 Renamed ‘PU/PD’ column to ‘Reset state’ in *Table 5 on page 25* Added reference to STR7 Flash Programming Reference Manual
19-Apr-2005	6	Added STR715F devices and modified RAM size of STR71xF1 devices Added BGA package in *Section 5* Updated ordering information in *Section 7*. Added PLL duty cycle min and max. in *PLL electrical characteristics on page 45*
13-Oct-2005	7	Updated feature description on page 1 Update overview *Section 1.1* Added OD/PP to P0.12 in *Table 5* Changed name of WFI mode to WAIT mode Changed Memory Map *Table 6*: Ext. Memory changed to 64 MB and flash register changed to 36 bytes. Added Power Consumption *Table 13* Modified BGA144 F3, F5, F12 and G12 in *Table 3* and *Table 4* Update EMI Timing *Table 24* and *Figure 29*

Table 44. Document revision history (continued)

Date	Revision	Changes
22-May-2006	8	Added Flashless device. Changed reset state of pins P1.10 and P1.13 from pu to pd, P0.15 from pu to floating and removed x in interrupt column for P1.15 and P1.12 in *Table 4* and *Table 5* Added notes under *Table 4* on EMI pin reset state. Corrected inch value for d3 in *Figure 40* Added footprint diagrams in *Figure 40* and *Figure 43* Updated *Section 4: Electrical parameters*
01-Aug-2006	9	Flash data retention changed to 20 years at 85° C. Changed note 8 on page 19 Changed note 1 on page 45
06-Nov-2006	10	Added STR715FR0T1 in *Table 42: Order codes* P0.12 corrected in *Table 5 on page 25*
20-Mar-2007	11	Added characteristics of *BSPI - buffered serial peripheral interface on page 63* Updated *Table 21: Low-power mode wakeup timing on page 46*
13-Feb-2008	12	Updated ordering information Updated USB characteristics Updated external clock characteristics
03-Apr-2013	13	Updated title (to be in line with the “device summary” table) Updated ST Logo and Disclaimer Added *Section 8: Known limitations*