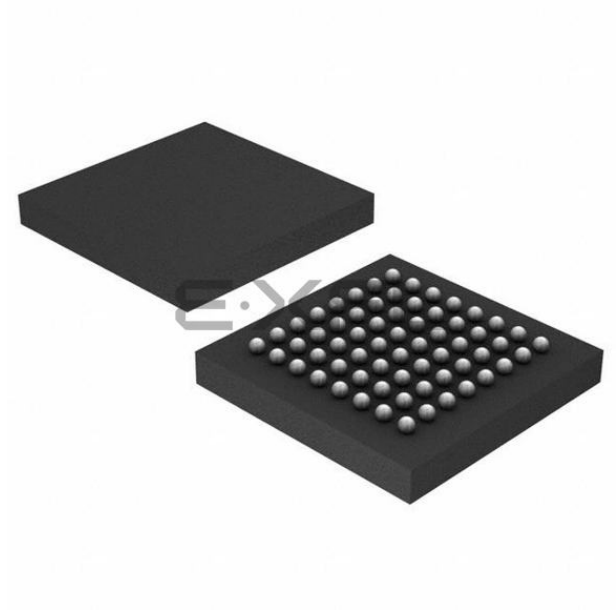

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, HDLC, I²C, SmartCard, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8 + 16K)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str712fr1h6

2 Description

ARM® core with embedded Flash and RAM

The STR71x series is a family of ARM-powered 32-bit microcontrollers with embedded Flash and RAM. It combines the high performance ARM7TDMI CPU with an extensive range of peripheral functions and enhanced I/O capabilities. STR71xF devices have on-chip high-speed single voltage FLASH memory and high-speed RAM. STR710R devices have high-speed RAM but no internal Flash. The STR71x family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Extensive tools support

STMicroelectronics' 32-bit, ARM core-based microcontrollers are supported by a complete range of high-end and low-cost development tools to meet the needs of application developers. This extensive line of hardware/software tools includes starter kits and complete development packages all tailored for ST's ARM core-based MCUs. The range of development packages includes third-party solutions that come complete with a graphical development environment and an in-circuit emulator/programmer featuring a JTAG application interface. These support a range of embedded operating systems (OS), while several royalty-free OSs are also available.

For more information, please refer to ST MCU site http://www.st.com/mcu

Flexible power management

To minimize power consumption, you can program the STR71x to switch to SLOW, WAIT, LPWAIT (low power wait), STOP or STANDBY mode depending on the current system activity in the application.

Flexible clock control

Two external clock sources can be used, a main clock and a 32 kHz backup clock. The embedded PLL allows the internal system clock (up to 66 MHz) to be generated from a main clock frequency of 16 MHz or less. The PLL output frequency can be programmed using a wide selection of multipliers and dividers. The microcontroller core, APB1 and APB2 peripherals are in separate clock domains and can be programmed to run at different frequencies during application runtime. The clock to each peripheral is gated with an individual control bit to optimize power usage by turning off peripherals any time they are not required.

Voltage regulators

The STR71x requires an external 3.0-3.6V power supply. There are two internal Voltage Regulators for generating the 1.8V power supply for the core and peripherals. The main VR is switched off during low power operation.

Low voltage detectors

Both the Main Voltage Regulator and the Low Power Voltage Regulator contain each a low voltage detection circuitry which keep the device under reset when the corresponding controlled voltage value (V_{18} or V_{18BKP}) falls below 1.35V (+/- 10%). This enhances the security of the system by preventing the MCU from going into an unpredictable state.

An external reset circuit must be used to provide the RESET at V_{33} power-up. It is not sufficient to rely on the RESET generated by the LVD in this case. This is because LVD operation is guaranteed only when V_{33} is within the specification.

3.1 On-chip peripherals

CAN interface (STR710 and STR712)

The CAN module is compliant with the CAN specification V2.0 part B (active). The bit rate can be programmed up to 1 MBaud.

USB interface (STR710 and STR711)

The full-speed USB interface is USB V2.0 compliant and provides up to 16 bidirectional/32 unidirectional endpoints, up to 12 Mb/s (full-speed), support for bulk transfer, isochronous transfers and USB Suspend/Resume functions.

Standard timers

Each of the four timers have a 16-bit free-running counter with 7-bit prescaler

Three timers each provide up to two input capture/output compare functions, a pulse counter function, and a PWM channel with selectable frequency.

The fourth timer is not connected to the I/O ports. It can be used by the application software for general timing functions.

Table 3. STR710 BGA ball connections

	A	B	C	D	E	F	G	H	J	K	L	M
1	P0.10	P2.0	P2.1	VSS	P2.2	P2.6	BOOT EN	P2.12	P2.13	P2.15	JTDI	N.C.
2	VSS	RDn	P0.11	V33	P2.3	P2.8	P2.9	JTMS	JTRSTn	TEST	TEST	N.C.
3	V33	P0.9	P0.12	P0.13	P2.4	N.C.	P2.10	JTCK	NU	V33	N.C.	DBG RQS
4	P0.6	P0.7	P0.8	P0.14	P2.5	N.C.	P2.11	JTDO	CK	CKOUT	VSSIO-PLL	N.C.
5	A.19	WEn.1	WEn.0	P0.5	P2.7	VSS	P2.14	N.C.	RTCX-TO	RTCXTI	N.C.	P0.15
6	P0.3	A.15	A.16	A.17	A.18	V33	V18	N.C.	N.C.	V18BKP	VSS BKP	$\overline{\text{STDBY}}$
7	P0.2	P0.1	P0.4	VSS18	V18	A.14	D.12	D.1	D.0	nc	VSS18	$\overline{\text{RSTIN}}$
8	A.9	A.10	A.11	A.13	P0.0	A.0	D.11	P1.12/ CANTX	N.C.	AVSS	D.3	D.2
9	VSS	V33	A.5	A.6	V33	D.15	D.10	P1.8	D.9	P1.0	N.C.	N.C.
10	A.8	N.C.	P1.15	P1.13	VSS	D.14	USBDN	P1.7	D.8	P1.5	P1.1	D.4
11	A.7	N.C.	P1.14	P1.10	A.2	D.13	USBDP	VSS	D.5	P1.4	P1.3	AVDD
12	A.12	A.4	A.3	P1.9	A.1	P1.11/ CANRX	N.C.	V33IO-PLL	P1.6	D.7	D.6	P1.2

Legend / abbreviations for *Table 4*:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: C = CMOS $0.3V_{DD}/0.7V_{DD}$
C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger
T_T= TTL 0.8 V/2 V with input trigger
C/T = Programmable levels: CMOS $0.3V_{DD}/0.7V_{DD}$ or TTL 0.8 V / 2 V

Port and control configuration:

Input: pu/pd= software enabled internal pull-up or pull down
pu= in reset state, the internal 100kΩ weak pull-up is enabled.
pd = in reset state, the internal 100kΩ weak pull-down is enabled.

Output: OD = open drain (logic level)
PP = push-pull
T = true OD, (P-Buffer and protection diode to V_{DD} not implemented), 5 V tolerant.

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
59	L7	V_{SS18}	S								Stabilization for main voltage regulator.		
60	K7	N.C.									Not connected (not bonded)		
61	J7	D.0	I/O	6)			8mA				External Memory Interface: data bus		
62	H7	D.1	I/O	6)			8mA						
63	M8	D.2	I/O	6)			8mA						
64	L8	D.3	I/O	6)			8mA						
65	M10	D.4	I/O	6)			8mA						
66	M11	V_{DDA}	S								Supply voltage for A/D Converter		
67	K8	V_{SSA}	S								Ground voltage for A/D Converter		
68	J8	N.C.									Not connected (not bonded)		
69	M9	N.C.									Not connected (not bonded)		
70	L9	N.C.									Not connected (not bonded)		
71	K9	P1.0/T3.OCMPB/AIN.0	I/O	pu	C_T		4mA	X	X		Port 1.0	Timer 3: Output Compare B	ADC: Analog input 0
72	L10	P1.1/T3.ICAPA/T3.EXTCLK/AIN.1	I/O	pu	C_T		4mA	X	X		Port 1.1	Timer 3: Input Capture A or External Clock input	ADC: Analog input 1
73	M12	P1.2/T3.OCMPA/AIN.2	I/O	pu	C_T		4mA	X	X		Port 1.2	Timer 3: Output Compare A	ADC: Analog input 2
74	L11	P1.3/T3.ICAPB/AIN.3	I/O	pu	C_T		4mA	X	X		Port 1.3	Timer 3: Input Capture B	ADC: Analog input 3
75	K11	P1.4/T1.ICAPA/T1.EXTCLK	I/O	pu	C_T		4mA	X	X		Port 1.4	Timer 1: Input Capture A	Timer 1: External Clock input
76	K10	P1.5/T1.ICAPB	I/O	pu	C_T		4mA	X	X		Port 1.5	Timer 1: Input Capture B	
77	J12	P1.6/T1.OCMPB	I/O	pu	C_T		4mA	X	X		Port 1.6	Timer 1: Output Compare B	
78	J11	D.5	I/O	6)			8mA				External Memory Interface: data bus		
79	L12	D.6	I/O	6)			8mA						
80	K12	D.7	I/O	6)			8mA						
81	J10	D.8	I/O	6)			8mA						
82	J9	D.9	I/O	6)			8mA						

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
83	H12	$V_{33IO-PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference[4]		
84	H11	$V_{SSIO-PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[4]		
85	H10	P1.7/T1.OCMPA	I/O	pu	C_T		4mA	X	X		Port 1.7	Timer 1: Output Compare A	
86	H9	P1.8	I/O	pd	C_T		4mA	X	X		Port 1.8		
87	G12	N.C.									Not connected (not bonded)		
88	F12	P1.11/CANRX	I/O	pu	C_T	X	4mA	X	X		Port 1.11	CAN: receive data input **Note:** On STR710 and STR712 only	
89	H8	P1.12/CANTX	I/O	pu	C_T		4mA	X	X		Port 1.12	CAN: Transmit data output **Note:** On STR710 and STR712 only	
90	G11	USBDP	I/O		C_T						USB bidirectional data (data +). Reset state = HiZ **Note:** On STR710 and STR711 only This pin requires an external pull-up to V_{33} to maintain a high level.		
91	G10	USBDN	I/O		C_T						USB bidirectional data (data -). Reset state = HiZ **Note:** On STR710 and STR711 only.		
92	G9	D.10	I/O	6)			8mA				External Memory Interface: data bus		
93	G8	D.11	I/O	6)			8mA						
94	G7	D.12	I/O	6)			8mA						
95	F11	D.13	I/O	6)			8mA						
96	F10	D.14	I/O	6)			8mA						
97	F9	D.15	I/O	6)			8mA						
98	F8	A.0	O	7)			8mA		X		External Memory Interface: address bus		
99	E12	A.1	O	7)			8mA		X				
100	E11	A.2	O	7)			8mA		X				
101	C12	A.3	O	7)			8mA		X				
102	B12	A.4	O	7)			8mA		X				
103	E10	V_{SS}	S								Ground voltage for digital I/O circuitry[4]		
104	E9	V_{33}	S								Supply voltage for digital I/O circuitry[4]		
105	D12	P1.9	I/O	pd	C_T		4mA	X	X		Port 1.9		
106	D11	P1.10/ USBCLK	I/O	pd	C/ T		4mA	X	X		Port 1.10	USB: 48 MHZ clock input	

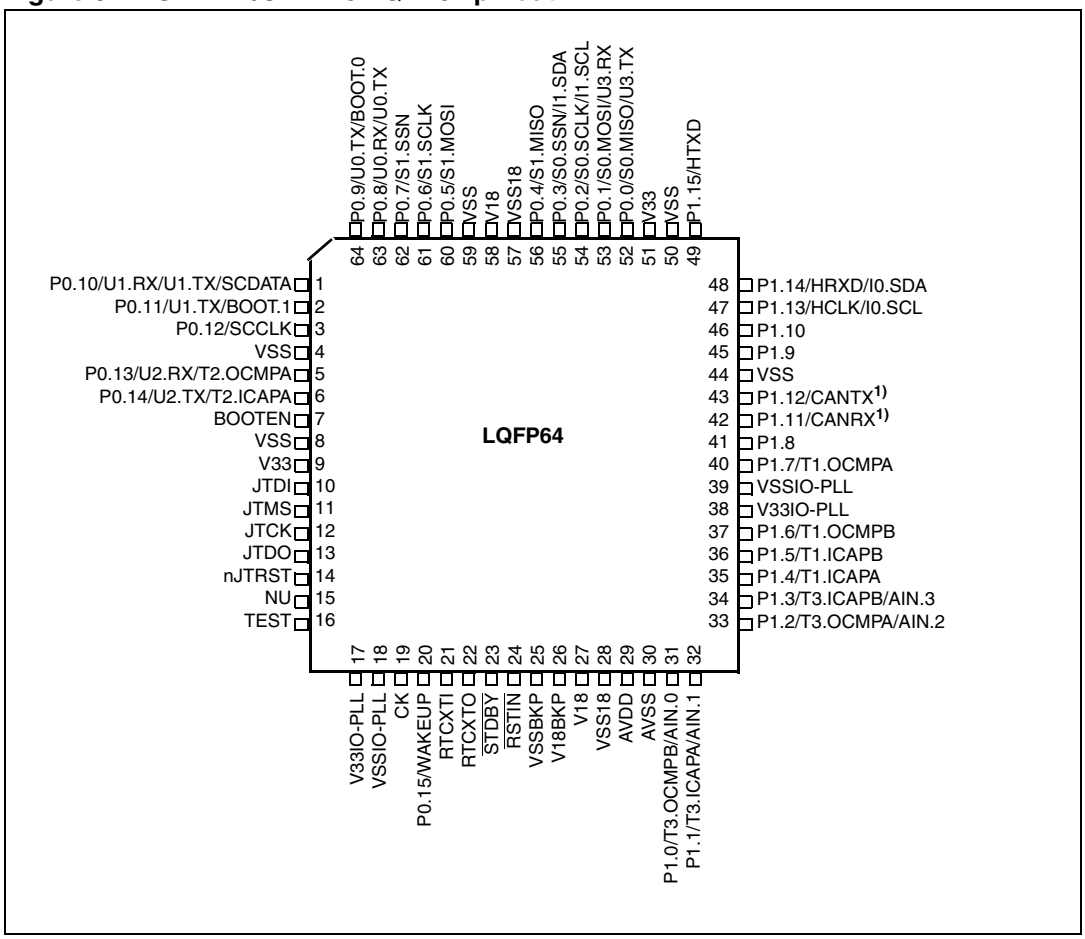
Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
143	C4	P0.8/U0.RX/ U0.TX	I/O	pd	C_T	X	4mA	T			Port 0.8	UART0: Receive Data input	UART0: Transmit data output.
											Note: This pin may be used for single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress		
144	B3	P0.9/U0.TX/ BOOT.0	I/O	pd	C_T		4mA	X	X		Port 0.9	Select Boot Configuration input	UART0: Transmit data output

1. The Reset configuration of the I/O Ports is IPUPD (input pull-up/pull down). Refer to *Table 6 on page 30*. The Port bit configuration at reset is PC0=1, PC1=1, PC2=0. The port data register bit (PD) value depends on the pu/pd column which specifies whether the pull-up or pull-down is enabled at reset
2. In reset state, these pins configured as Input PU/PD with weak pull-up enabled. They must be configured by software as Alternate Function (see *Table 6: Port bit configuration table on page 30*) to be used by the External Memory Interface.
3. In reset state, these pins configured as Input PU/PD with weak pull-down enabled to output Address 0x0000 0000 using the External Memory Interface. To access memory banks greater than 1Mbyte, they need to be configured by software as Alternate Function (see *Table 6: Port bit configuration table on page 30*).
4. $V_{33IO\text{-}PLL}$ and V_{33} are internally connected. $V_{SSIO\text{-}PLL}$ and V_{SS} are internally connected.
5. During the reset phase, these pins are in input pull-up state. When reset is released, they are configured as Output Push-Pull.
6. During the reset phase, these pins are in input pull-up state. When reset is released, they are configured as Hi-Z.
7. During the reset phase, these pins are in input pull-down state. When reset is released, they are configured as Output Push-Pull.
8. During the reset phase, this pin is in input floating state. When reset is released, it is configured as Output Push-Pull.

3.4 Pin description for 64-pin packages

Figure 3. STR712/STR715 LQFP64 pinout



1. CANTX and CANRX in STR712F only, in STR715F they are general purpose I/Os.

4 Electrical parameters

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

4.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25°C and T_A=$T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

4.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25°C, V_{33}=3.3V (for the 3.0V≤V_{33}≤3.6V voltage range) and V_{18}=1.8V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

4.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

4.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

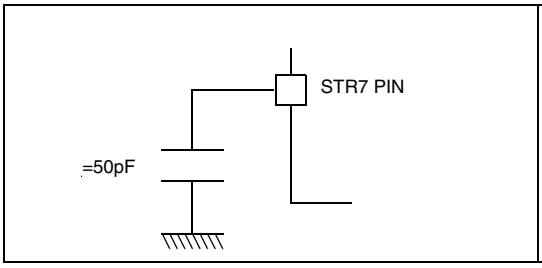


Figure 10. Pin input voltage

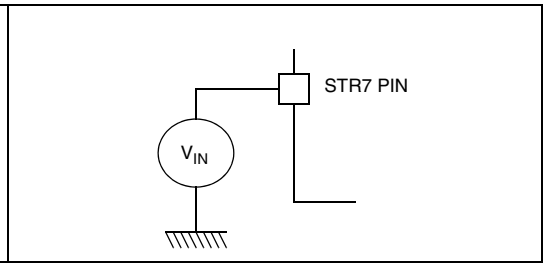


Table 9. Current characteristics

Symbol	Ratings	Max.	Unit
I_{V33}	Total current into $V_{33}/V_{33IO-PLL}$ power lines (source) [2]	150	mA
I_{VSS}	Total current out of $V_{SS}/V_{SSIO-PLL}$ ground lines (sink) [2]	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$ [1] [3]	Injected current on $\overline{RSTIN}$ pin	± 5	
	Injected current on CK pin	± 5	
	Injected current on any other pin [4]	± 5	
$\Sigma I_{INJ(PIN)}$ [1]	Total injected current (sum of all I/O and control pins) [4]	± 25	

The $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{33}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected. Data based on T_A = 25 °C.

All 3.3V power (V_{33}, AV_{DD}, $V_{33IO-PLL}$) and ground (V_{SS}, AV_{SS}, $V_{SSIO-PLL}$) pins must always be connected to the external 3.3V supply.

Negative injection disturbs the analog performance of the device. See note in *Section 4.3.11: ADC characteristics on page 66*.

When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Only when using external 1.8V power supply. All the power (V_{18}, V_{18BKP}) and ground (V_{SS18}, V_{SSBKP}) pins must always be connected to the external 1.8V supply.

Table 10. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature (see *Section 5.2: Thermal characteristics on page 73*)		

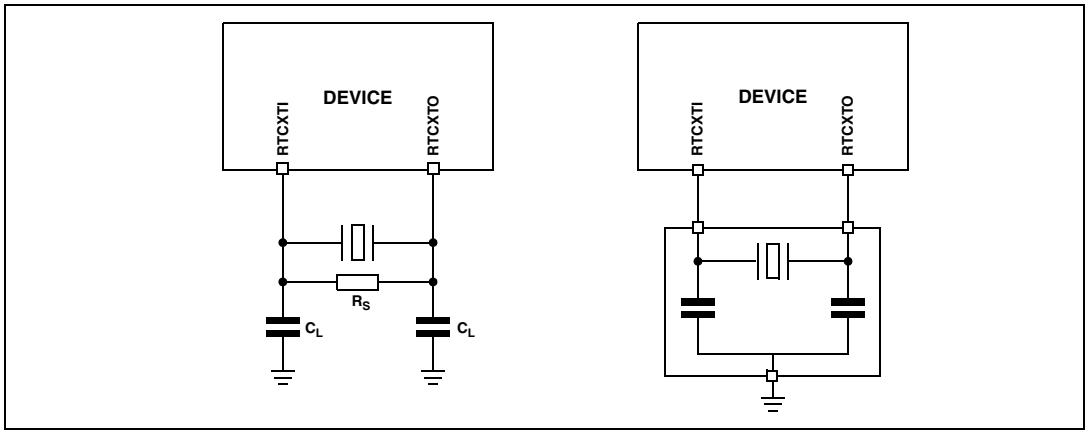
Table 17. RTCXT1 external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RTCXT1}	External clock source frequency		0		500	kHz
$V_{RTCXT1H}$	RTCXT1 input pin high level voltage		$0.7xV_{33}$		V_{33}	V
$V_{RTCXT1L}$	RTCXT1 input pin low level voltage		V_{SS}		$0.3xV_{33}$	
$t_{w(RTCXT1)}$ $t_{w(RTCXT1)}$	RTCXT1 high or low time [1]		100			ns
$t_{r(RTCXT1)}$ $t_{f(RTCXT1)}$	RTCXT1 rise or fall time [1]				5	
$C_{IN(RTCXT1)}$	RTCXT1 input capacitance[1]			5		pF
DuCy(RTCXT1)	Duty cycle		30		70	%
I_L	RTCXT1 Input leakage current	$V_{SS} \le V_{IN} \le V_{33}$			±1	µA

Notes:

1. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 16. RTC crystal oscillator and resonator



PLL electrical characteristics

V_{33} = 3.0 to 3.6V, $V_{33IOPLL}$ = 3.0 to 3.6V, T_A = -40 / 85 °C unless otherwise specified.

Table 19. PLL1 characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$f_{PLLCLK1}$	PLL multiplier output clock				165	MHz
f_{PLL1}	PLL input clock	FREF_RANGE = 0	1.5		3.0	MHz
		FREF_RANGE = 1 MX[1:0]='00' or '01'	3.0		8.25	MHz
		FREF_RANGE = 1 MX[1:0]='10' or '11'	3.0		6	MHz
	PLL input clock duty cycle		25		75	%
f_{FREE1}	PLL free running frequency	FREF_RANGE = 0 MX[1:0]='01' or '11'		125		kHz
		FREF_RANGE = 0 MX[1:0]='00' or '10'		250		kHz
		FREF_RANGE = 1 MX[1:0]='01' or '11'		250		kHz
		FREF_RANGE = 1 MX[1:0]='00' or '10'		500		kHz
t_{LOCK1}	PLL lock time	FREF_RANGE = 0 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			300	µs
		FREF_RANGE = 1 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			600	µs

Table 19. PLL1 characteristics (continued)

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$\Delta t_{JITTER1}$	PLL jitter (peak to peak)	t_{PLL} = 4 MHz, MX[1:0]='11' Global Output division = 32 (Output Clock = 2 MHz)		0.7	2	ns

Table 20. PLL2 characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$f_{PLLCLK2}$	PLL multiplier output clock				140	MHz
f_{PLL2}	PLL input clock	FREF_RANGE = 0	1.5		3.0	MHz
		FREF_RANGE = 1	3.0		5	MHz
t_{LOCK2}	PLL lock time	FREF_RANGE = 0 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			300	µs
		FREF_RANGE = 1 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			600	µs
$\Delta t_{JITTER2}$	PLL jitter (peak to peak)	t_{PLL} = 4 MHz, MX[1:0]='11' Global Output division = 32 (Output Clock = 2 MHz)		0.7	2	ns

Table 21. Low-power mode wakeup timing

Symbol	Parameter	Typ	Unit
$t_{WULPWFI}$	Wakeup from LPWFI mode	26(1)	µs
t_{WUSTOP}	Wakeup from STOP mode	2048	CLK Cycles (2)
t_{WUSTBY}	Wakeup from STANDBY mode	2048 CLK Cycles + 8 CLK2 Cycles(3)	Cycles

1. Clock selected is CK2_16, Main VReg OFF and Flash in power-down
2. The CLK clock is derived from the external oscillator.
3. Refer to Figure 7. Reset General Timing in the STR71xF Reference Manual (UM0084)

4.3.3 Memory characteristics

Flash memory

V_{33} = 3.0 to 3.6V, T_A = -40 to 85 °C unless otherwise specified.

Table 22. Flash memory characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ	Max[1]	
t_{PW}	Word Program			40		µs
t_{PDW}	Double Word Program			60		µs
t_{PB0}	Bank 0 Program (256K)	Double Word Program		1.6	2.1	s
t_{PB1}	Bank 1 Program (16K)	Double Word Program		130	170	ms
t_{ES}	Sector Erase (64K)	Not preprogrammed Preprogrammed		2.3 1.9	4.0 3.3	s
t_{ES}	Sector Erase (8K)	Not preprogrammed Preprogrammed		0.7 0.6	1.1 1.0	s
t_{ES}	Bank 0 Erase (256K)	Not preprogrammed Preprogrammed		8.0 6.6	13.7 11.2	s
t_{ES}	Bank 1 Erase (16K)	Not preprogrammed Preprogrammed		0.9 0.8	1.5 1.3	s
t_{RPD}[2]	Recovery when disabled				20	µs
t_{PSL}[2]	Program Suspend Latency				10	µs
t_{ESL}[2]	Erase Suspend Latency				300	µs
N_{END_B0}	Endurance (Bank 0 sectors)		10			kcycles
N_{END_B1}	Endurance (Bank 1 sectors)		100			kcycles
t_{RET}	Data Retention (Bank 0 and Bank 1)	T_A=85°	20			Years
t_{ESR}	Erase Suspend Rate	Min time from Erase Resume to next Erase Suspend	20			ms

Notes:

1. T_A=45°C after 0 cycles. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production

$\overline{\text{RSTIN}}$ pin

The $\overline{\text{RSTIN}}$ pin input driver is CMOS. A permanent pull-up is present which is the same as as R_{PU} (see *Table 27 on page 51*)

Subject to general operating conditions for V_{33} and T_A unless otherwise specified.

Table 29. $\overline{\text{RESET}}$ pin characteristics

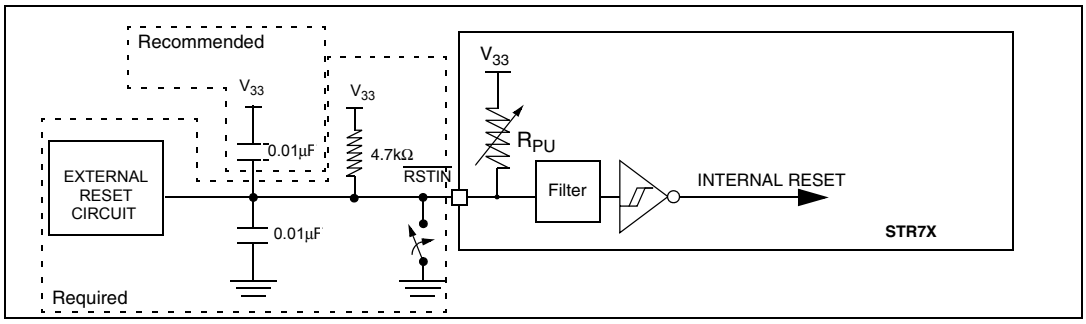
Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$V_{IL(RSTINn)}$	$\overline{\text{RSTIN}}$ Input low level voltage [1]				0.8	V
$V_{IH(RSTINn)}$	$\overline{\text{RSTIN}}$ Input high level voltage [1]		2			
$V_{F(RSTINn)}$	$\overline{\text{RSTIN}}$ Input filtered pulse[2]				500	ns
$V_{NF(RSTINn)}$	$\overline{\text{RSTIN}}$ Input not filtered pulse[2]		1.2			µs

Notes:

1. Data based on characterization results, not tested in production.

2) Data guaranteed by design, not tested in production.

Figure 24. Recommended $\overline{\text{RSTIN}}$ pin protection.[1]



Notes:

1. The R_{PU} pull-up equivalent resistor is based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 18*).
2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the $\overline{\text{RSTIN}}$ pin can go below the $V_{IL(RSTINn)}$ max. level specified in *Table 29*. Otherwise the reset will not be taken into account internally.

Table 34. I2C characteristics

Symbol	Parameter	Standard mode I^2C		Fast mode I^2C[5]		Unit
		Min [1]	Max [1]	Min [1]	Max [1]	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0 [3]		0 [2]	900 [3]	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	20+0.1C_b	300	
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

Notes:

1. Data based on standard I^2C protocol requirement, not tested in production.
2. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
3. The maximum hold time $t_{h(SDA)}$ is not applicable.
4. Measurement points are done at CMOS levels: $0.3xV_{DD}$ and $0.7xV_{DD}$.
5. f_{PCLK1}, must be at least 8 MHz to achieve max fast I^2C speed (400 kHz).
6. The following table gives the values to be written in the I2CCCR register to obtain the required I^2C SCL line frequency.

4.3.10 USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 37. USB startup time

Symbol	Parameter	Conditions	Max	Unit
$t_{STARTUP}$	USB transceiver startup time		1	µs

Table 38. USB DC characteristics

Symbol	Parameter	Conditions	Min.(1)(2)	Max.(1)(2)	Unit
Input Levels					
V_{DI}	Differential Input Sensitivity	I(DP, DM)	0.2		V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8	2.5	
V_{SE}	Single Ended Receiver Threshold		1.3	2.0	
Output Levels					
V_{OL}	Static Output Level Low	R_L of 1.5 kΩ to 3.6V(3)		0.3	V
V_{OH}	Static Output Level High	R_L of 15 kΩ to V_{SS}(3)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. It is important to be aware that the DP/DM pins are not 5 V tolerant. As a consequence, in case of a a shortcut with Vbus (typ: 5.0V), the protection diodes of the DP/DM pins will be direct biased . This will not damage the device if not more than 50 mA is sunk for longer than 24 hours but the reliability may be affected.
3. R_L is the load connected on the USB drivers

Figure 37. USB: data signal rise and fall time

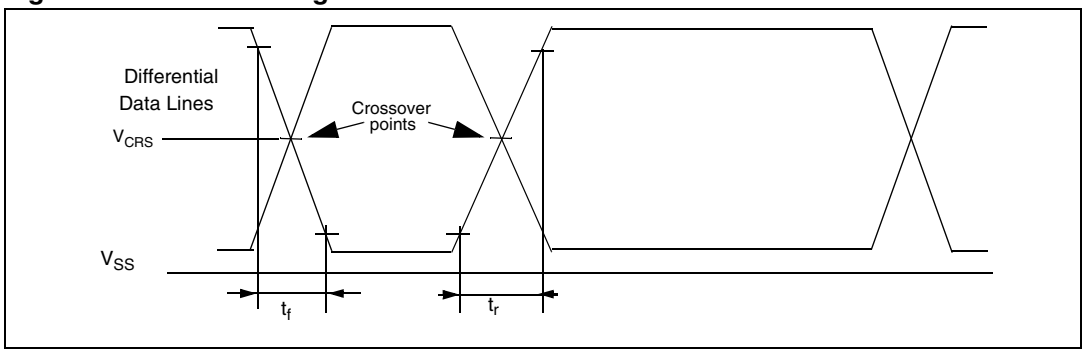
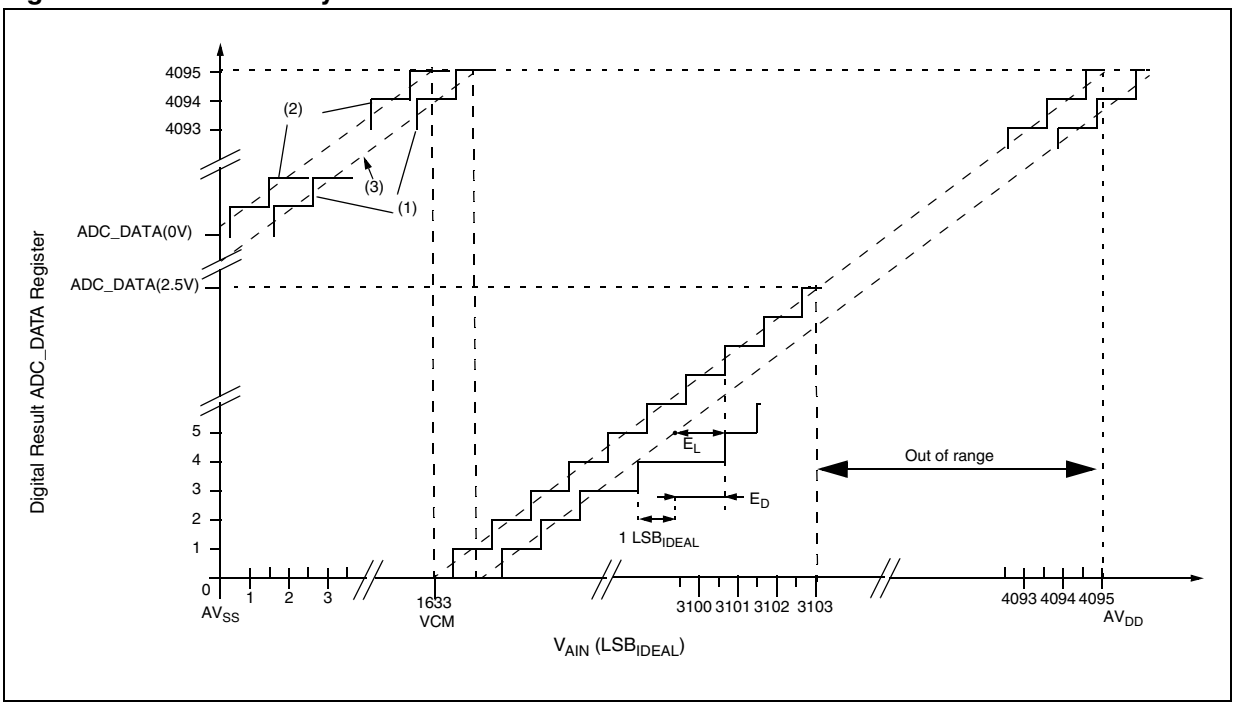


Table 39. USB: Full speed driver electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time(1)	C_L=50 pF	4	20	ns
t_f	Fall Time1)	C_L=50 pF	4	20	ns
t_{rfm}	Rise/ Fall Time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal Crossover Voltage		1.3	2.0	V

1. Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification - Chapter 7 (version 2.0).

Figure 38. ADC accuracy characteristics



1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line

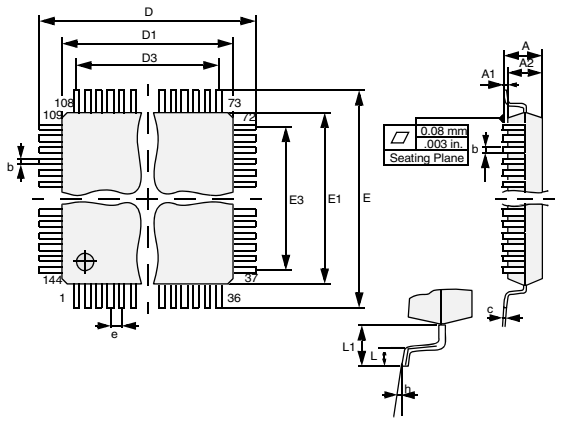
Legend for *Figure 38*

E_D=Differential Linearity Error: maximum deviation between actual steps and the ideal one.
E_L=Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Equation 1

$$1LSB_{IDEAL} = \frac{AVDD - AVSS}{4095}$$

Figure 41. 144-Pin low profile quad flat package

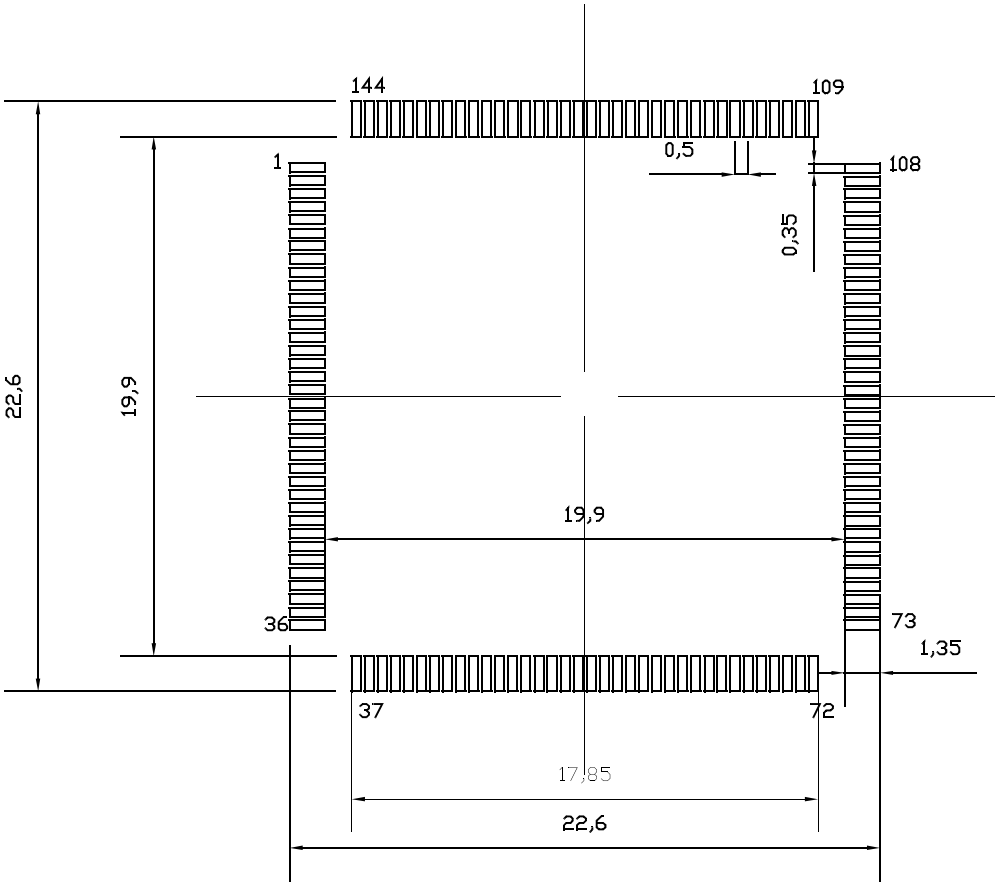


Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053		0.057
b	0.17	0.22	0.27	0.007		0.011
c	0.09		0.20	0.004		0.008
D	21.80	22.00	22.20	0.858	0.867	0.874
D1	19.80	20.00	20.20	0.780	0.787	0.795
D3		17.50			0.689	
E	21.80	22.00	22.20	0.858	0.867	0.874
E1	19.80	20.00	20.20	0.780	0.787	0.795
E3		17.50			0.689	
e		0.50			0.020	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	144					

Jedec Ref. MS-026-BFB

1.Values in inches are converted from mm and rounded to 3 decimal digits.

Recommended footprint (dimensions in mm)



5.2 Thermal characteristics

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

- T_A is the Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the Chip Internal Power.

$P_{I/O}$ represents the Power Dissipation on Input and Output Pins;

Most of the time for the application $P_{I/O} < P_{INT}$ and can be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273°C) \quad (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

where:

K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 42. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal Resistance Junction-Ambient LQFP 144 - 20 x 20 mm / 0.5 mm pitch	42	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LFBGA 144 - 10 x 10 x 1.7mm	50	°C/W

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