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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, HDLC, I²C, SmartCard, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8 + 16K)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str712fr1t6

Contents

List of tables

2 Description

ARM® core with embedded Flash and RAM

The STR71x series is a family of ARM-powered 32-bit microcontrollers with embedded Flash and RAM. It combines the high performance ARM7TDMI CPU with an extensive range of peripheral functions and enhanced I/O capabilities. STR71xF devices have on-chip high-speed single voltage FLASH memory and high-speed RAM. STR710R devices have high-speed RAM but no internal Flash. The STR71x family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Extensive tools support

STMicroelectronics' 32-bit, ARM core-based microcontrollers are supported by a complete range of high-end and low-cost development tools to meet the needs of application developers. This extensive line of hardware/software tools includes starter kits and complete development packages all tailored for ST's ARM core-based MCUs. The range of development packages includes third-party solutions that come complete with a graphical development environment and an in-circuit emulator/programmer featuring a JTAG application interface. These support a range of embedded operating systems (OS), while several royalty-free OSs are also available.

For more information, please refer to ST MCU site http://www.st.com/mcu

3 System architecture

Package choice: low pin-count 64-pin or feature-rich 144-pin LQFP or BGA

The STR71x family is available in 5 main versions.

The 144-pin versions have the full set of all features including CAN, USB and External Memory Interface (EMI).

- **STR710F:** 144-pin BGA or LQFP with CAN, USB and EMI
- **STR710R:** Flashless 144-pin BGA or LQFP with CAN, USB and EMI (no internal Flash memory)

The three 64-pin versions (LQFP) do not include External Memory Interface.

- **STR715F:** 64-pin LQFP without CAN or USB
- **STR711F:** 64-pin LQFP with USB
- **STR712F:** 64-pin LQFP with CAN

High speed Flash memory (STR71xF)

The Flash program memory is organized in two banks of 32-bit wide Burst Flash memories enabling true read-while-write (RWW) operation. Device Bank 0 is up to 256 Kbytes in size, typically for the application program code. Bank 1 is 16 Kbytes, typically used for storing data constants. Both banks are accessed by the CPU with zero wait states @ 33 MHz

Bank 0 memory endurance is 10K write/erase cycles and Bank 1 endurance is 100K write/erase cycles. Data retention is 20 years at 85°C on both banks. The two banks can be accessed independently in read or write. Flash memory can be accessed in two modes:

- Burst mode: 64-bit wide memory access at up to 50 MHz.
- Direct 32-bit wide memory access for deterministic operation at up to 33 MHz.

The STR7 embedded Flash memory can be programmed using In-Circuit Programming or In-Application programming.

IAP (in-application programming): The IAP is the ability to re-program the Flash memory of a microcontroller while the user program is running.

ICP (in-circuit programming): The ICP is the ability to program the Flash memory of a microcontroller using JTAG protocol while the device is mounted on the user application board.

The Flash memory can be protected against different types of unwanted access (read/write/erase). There are two types of protection:

- Sector Write Protection
- Flash Debug Protection (locks JTAG access)

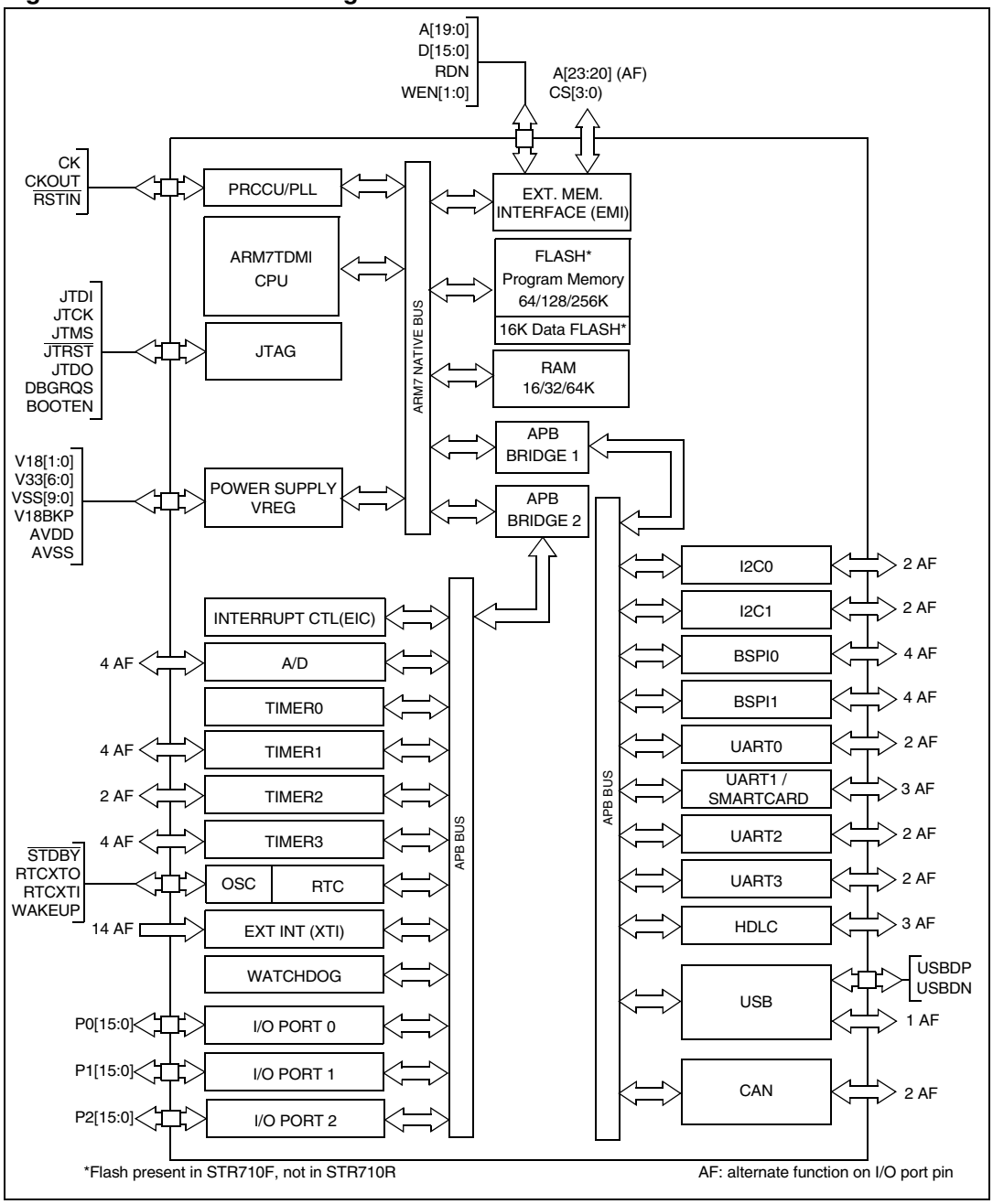
Refer to the STR7 Flash Programming Reference manual for details.

Optional external memory (STR710)

The non-multiplexed 16-bit data/24-bit address bus available on the STR710 (144-pin) supports four 16-Mbyte banks of external memory. Wait states are programmable individually for each bank allowing different memory types (Flash, EPROM, ROM, SRAM etc.) to be used to store programs or data.

Figure 1 shows the general block diagram of the device family.

Figure 1. STR71x block diagram



3.3 Pin description for 144-pin packages

Figure 2. STR710 LQFP pinout

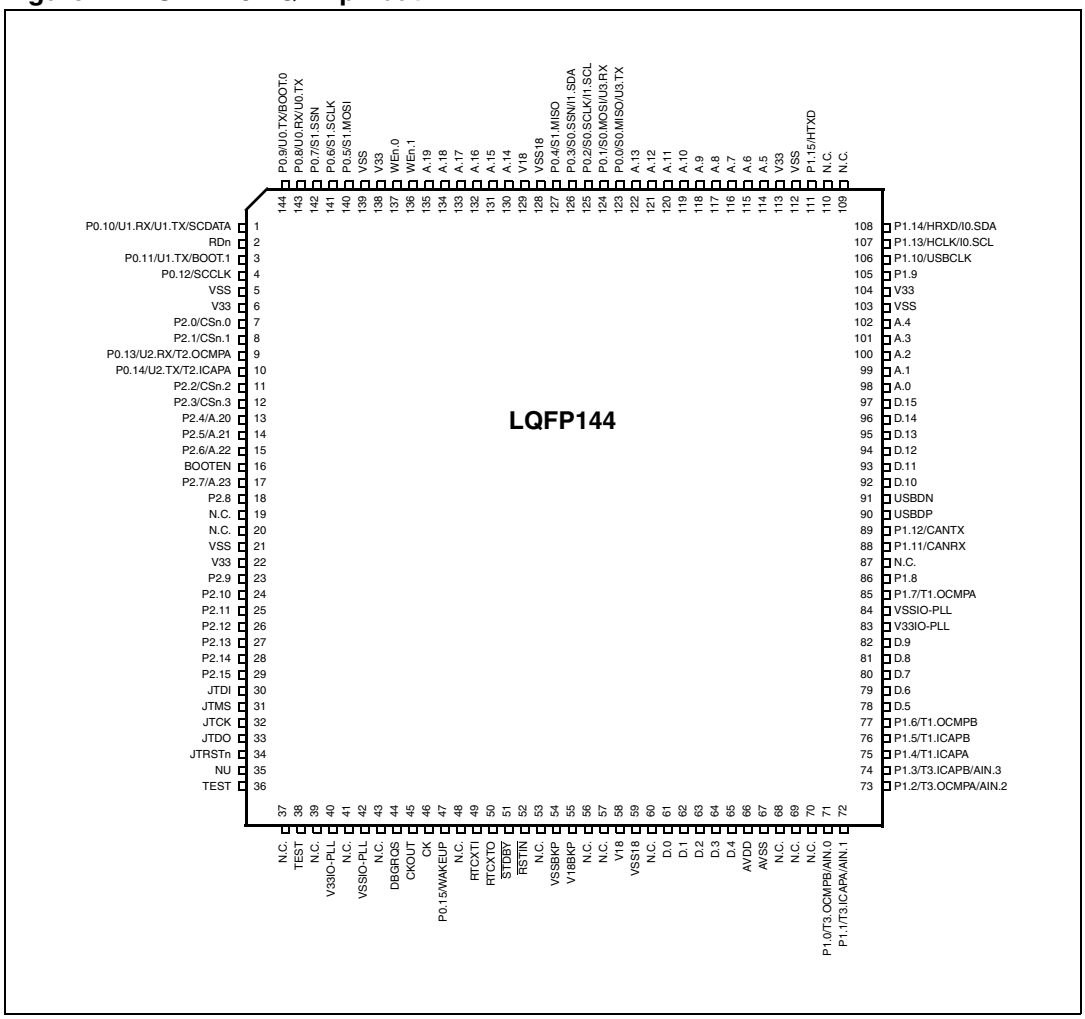
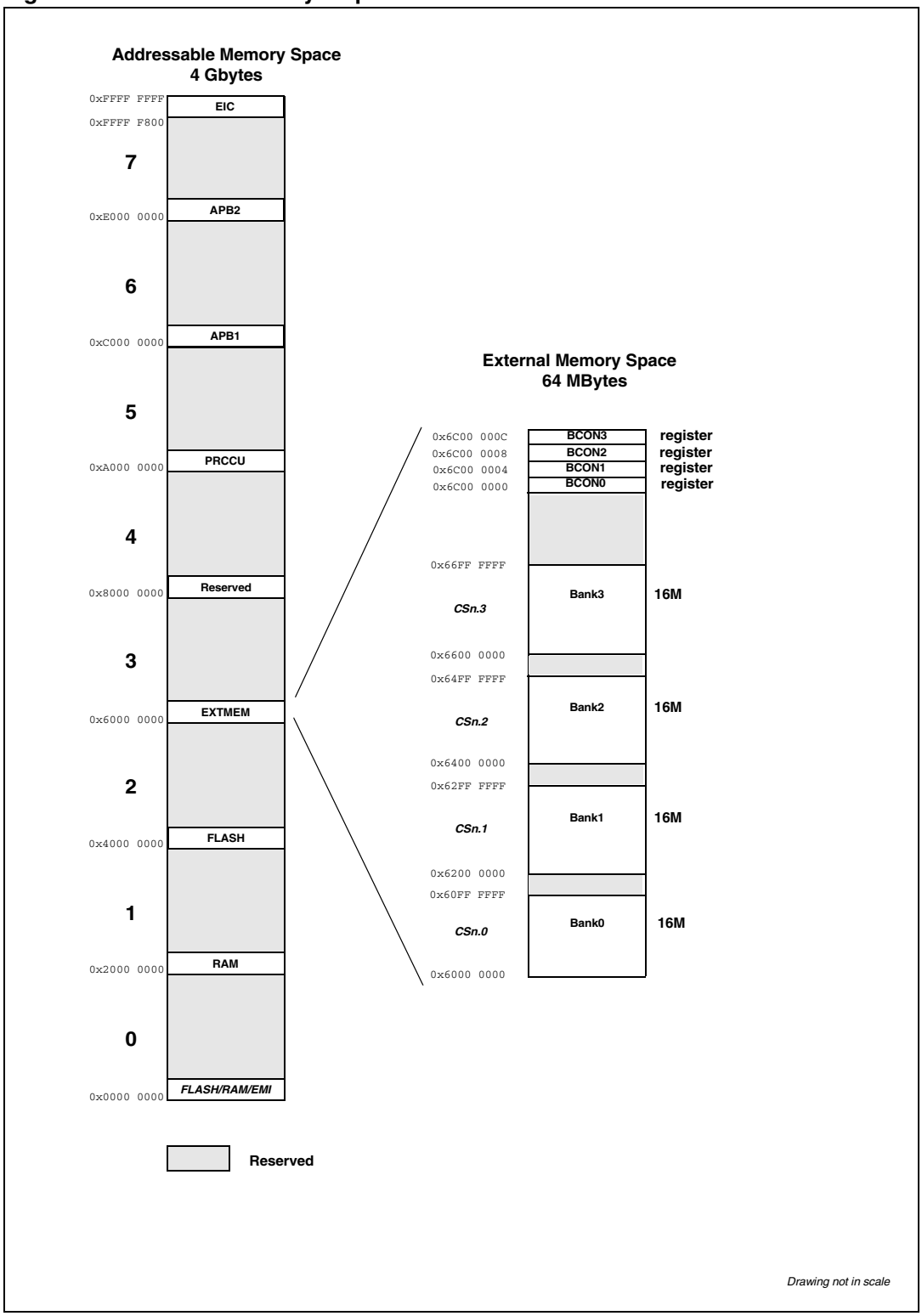


Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1)]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
52	P0.0/S0.MISO /U3.TX	I/O	pu	C_T		4mA	X	X		Port 0.0	SPI0 Master in/Slave out data	UART3 Transmit data output
											Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
53	P0.1/S0.MOSI /U3.RX	I/O	pu	C_T	X	4mA	X	X		Port 0.1	BSPI0: Master out/Slave in data	UART3: Receive Data input
											Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
54	P0.2/S0.SCLK /I1.SCL	I/O	pu	C_T	X	4mA	X	X		Port 0.2	BSPI0: Serial Clock	I2C1: Serial clock
											Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
55	P0.3/S0.$\overline{SS}$/I1 .SDA	I/O	pu	C_T		4mA	X	X		Port 0.3	SPI0: Slave Select input active low.	I2C1: Serial Data
											Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
56	P0.4/S1.MISO	I/O	pu	C_T		4mA	X	X		Port 0.4	SPI1: Master in/Slave out data	
57	V_{SS18}	S								Stabilization for main voltage regulator.		
58	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
59	V_{SS}	S								Ground voltage for digital I/Os		
60	P0.5/S1.MOSI	I/O	pu	C_T		4mA	X	X		Port 0.5	SPI1: Master out/Slave In data	
61	P0.6/S1.SCLK	I/O	pu	C_T	X	4mA	X	X		Port 0.6	SPI1: Serial Clock	
62	P0.7/S1.$\overline{SS}$	I/O	pu	C_T		4mA	X	X		Port 0.7	SPI1: Slave Select input active low	

Figure 8. External memory map



4 Electrical parameters

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

4.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25°C and T_A=$T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

4.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25°C, V_{33}=3.3V (for the 3.0V≤V_{33}≤3.6V voltage range) and V_{18}=1.8V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

4.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

4.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

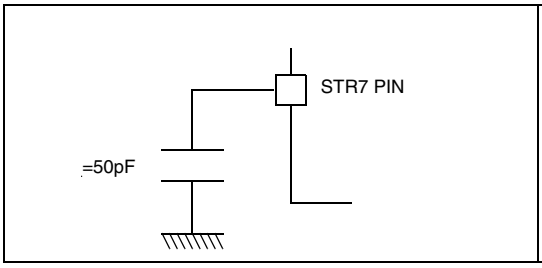


Figure 10. Pin input voltage

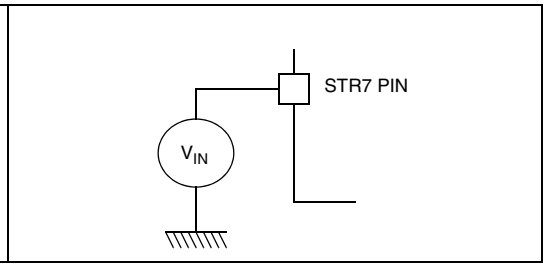


Table 9. Current characteristics

Symbol	Ratings	Max.	Unit
I_{V33}	Total current into $V_{33}/V_{33IO-PLL}$ power lines (source) [2]	150	mA
I_{VSS}	Total current out of $V_{SS}/V_{SSIO-PLL}$ ground lines (sink) [2]	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$ [1] [3]	Injected current on $\overline{RSTIN}$ pin	± 5	
	Injected current on CK pin	± 5	
	Injected current on any other pin [4]	± 5	
$\Sigma I_{INJ(PIN)}$ [1]	Total injected current (sum of all I/O and control pins) [4]	± 25	

The $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{33}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected. Data based on T_A = 25 °C.

All 3.3V power (V_{33}, AV_{DD}, $V_{33IO-PLL}$) and ground (V_{SS}, AV_{SS}, $V_{SSIO-PLL}$) pins must always be connected to the external 3.3V supply.

Negative injection disturbs the analog performance of the device. See note in *Section 4.3.11: ADC characteristics on page 66*.

When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Only when using external 1.8V power supply. All the power (V_{18}, V_{18BKP}) and ground (V_{SS18}, V_{SSBKP}) pins must always be connected to the external 1.8V supply.

Table 10. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature (see *Section 5.2: Thermal characteristics on page 73*)		

4.3.1 Supply current characteristics

The current consumption is measured as described in *Figure 9 on page 34* and *Figure 10 on page 34*.

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{33} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.
- Embedded Regulators are used to provide 1.8V (except if explicitly mentioned)

Subject to general operating conditions for V_{33}, and T_A.

Table 13. Total current consumption

Symbol	Parameter	Conditions	Typ [1]	Max [2]	Unit
I_{DD} [4]	Supply current in RUN mode	f_{MCLK}=66 MHz, RAM execution	73.6	100	mA
		f_{MCLK}=32 MHz, Flash non-burst execution	49.3		
	Supply current in STOP mode	T_A=25°C	10	50[3]	µA
	Supply current in STANDBY mode	OSC32K bypassed	12	30	µA

Notes:

1. Typical data are based on T_A=25°C, V_{33}=3.3V.
2. Data based on characterization results, tested in production at V_{33}, f_{MCLK} max. and T_A max.
3. Based on device characterisation, device power consumption in STOP mode at T_A 25°C is predicted to be 30µA or less in 99.730020% of parts.
4. The conditions for these consumption measurements are described in application note AN2100.

Figure 11. STOP I_{DD} vs. V_{33}

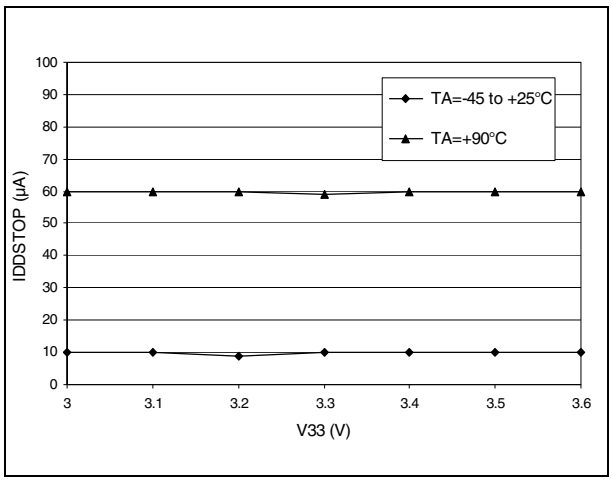


Figure 12. STANDBY I_{DD} vs. V_{33}

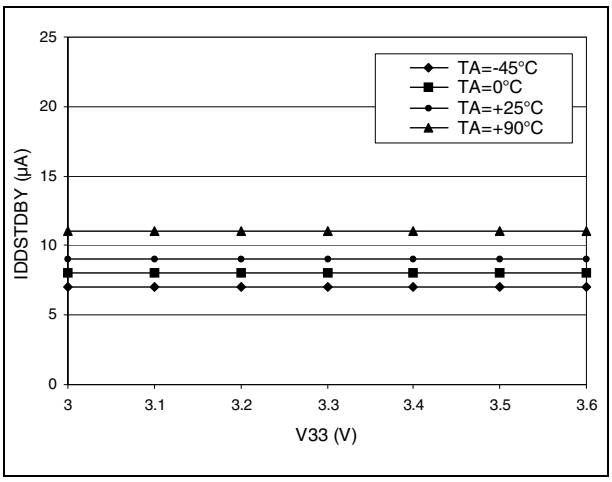
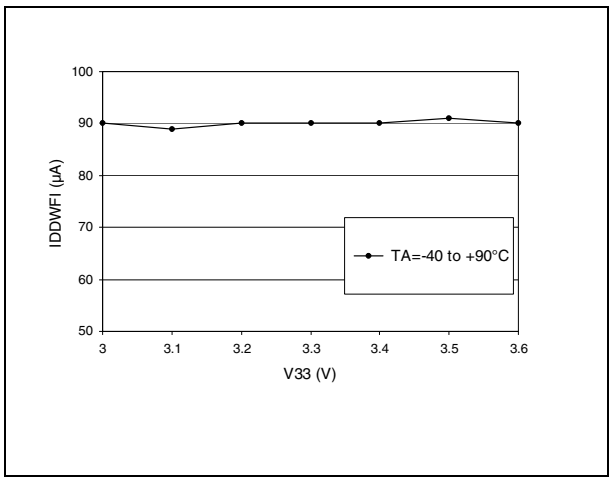


Figure 13. WFI I_{DD} vs. V_{33}



4.3.3 Memory characteristics

Flash memory

V_{33} = 3.0 to 3.6V, T_A = -40 to 85 °C unless otherwise specified.

Table 22. Flash memory characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ	Max[1]	
t_{PW}	Word Program			40		µs
t_{PDW}	Double Word Program			60		µs
t_{PB0}	Bank 0 Program (256K)	Double Word Program		1.6	2.1	s
t_{PB1}	Bank 1 Program (16K)	Double Word Program		130	170	ms
t_{ES}	Sector Erase (64K)	Not preprogrammed Preprogrammed		2.3 1.9	4.0 3.3	s
t_{ES}	Sector Erase (8K)	Not preprogrammed Preprogrammed		0.7 0.6	1.1 1.0	s
t_{ES}	Bank 0 Erase (256K)	Not preprogrammed Preprogrammed		8.0 6.6	13.7 11.2	s
t_{ES}	Bank 1 Erase (16K)	Not preprogrammed Preprogrammed		0.9 0.8	1.5 1.3	s
t_{RPD}[2]	Recovery when disabled				20	µs
t_{PSL}[2]	Program Suspend Latency				10	µs
t_{ESL}[2]	Erase Suspend Latency				300	µs
N_{END_B0}	Endurance (Bank 0 sectors)		10			kcycles
N_{END_B1}	Endurance (Bank 1 sectors)		100			kcycles
t_{RET}	Data Retention (Bank 0 and Bank 1)	T_A=85°	20			Years
t_{ESR}	Erase Suspend Rate	Min time from Erase Resume to next Erase Suspend	20			ms

Notes:

1. T_A=45°C after 0 cycles. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production

4.3.4 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electro magnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

In the case of an ARM7 CPU, in order to write robust code that can withstand all kinds of stress, such as very strong electromagnetic disturbance, it is mandatory that the Data Abort, Prefetch Abort and Undefined Instruction exceptions are managed by the application software. This will prevent the code going into an undefined state or performing any unexpected operation.

Table 25. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value [1]	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25°C	2000	V
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)		200	
$V_{ESD(CDM)}$	Electro-static discharge voltage (Charge Device Model)		750 on corner pins, 500 on others	

Notes:

1. Data based on characterization results, not tested in production.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Electrical sensitivities

Table 26. Static and dynamic latch-up

Symbol	Parameter	Conditions	Class[1]
LU	Static latch-up class	T_A=+25°C T_A=+85°C T_A=+105°C	A A A
DLU	Dynamic latch-up class	V_{DD}=3.3 V, f_{OSC4M}=4 MHz, f_{MCLK}=32 MHz, T_A=+25°C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

Figure 22. Typical V_{OL} vs. V_{33}

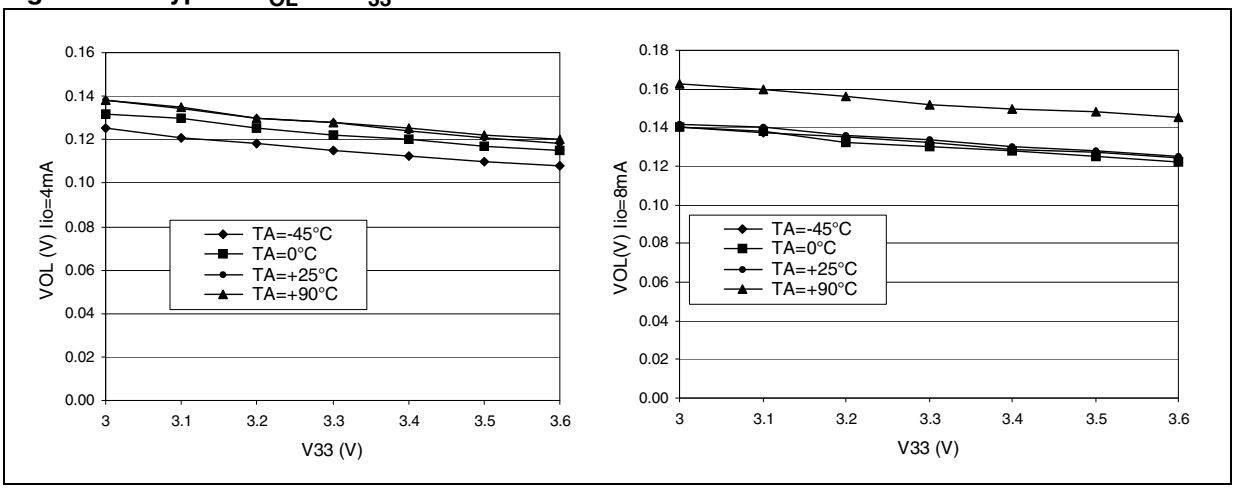


Figure 23. Typical V_{OH} vs. V_{33}

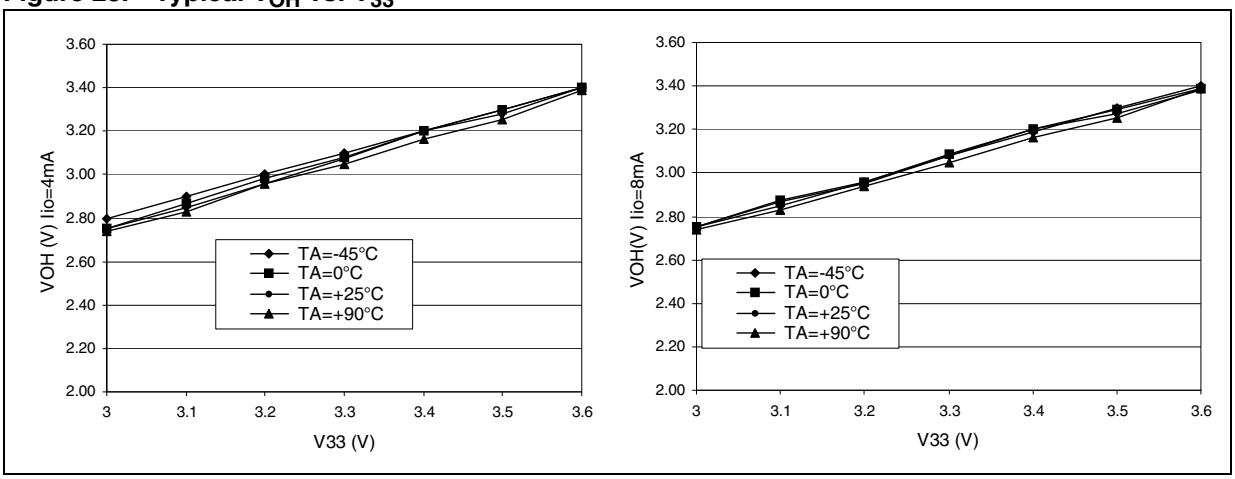


Table 41. ADC accuracy with f_{PCLK2} = 20 MHz, f_{ADC}=10 MHz, AV_{DD}=3.3 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ADC_DATA(0V)	Converted code when AIN=0V 1)		2370		2565	Decimal code
ADC_DATA(2.5V)	Converted code when AIN=2.5V 1)		1480		1680	
VCM	Center voltage of Sigma-Delta Modulator1)		1.23	1.25	1.30	V
TUE	Total unadjusted error	In this type of ADC, calibration is necessary to correct gain error and offset errors. Once calibrated, the TUE is limited to the ILE.				
$\lvert E_D \rvert$	Differential linearity error1)			1.96	2.19	LSB
$\lvert E_L \rvert$	Integral linearity error 1)			2.36	3.95	

Data are based on characterisation and are not tested in production.

ADC Accuracy vs. Negative Injection Current

Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. The effect of negative injection current on robust pins is specified in *Section 4.3.5*.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 4.3.5* does not affect the ADC accuracy.

5.2 Thermal characteristics

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

- T_A is the Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the Chip Internal Power.

$P_{I/O}$ represents the Power Dissipation on Input and Output Pins;

Most of the time for the application $P_{I/O} < P_{INT}$ and can be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273°C) \quad (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

where:

K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 42. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal Resistance Junction-Ambient LQFP 144 - 20 x 20 mm / 0.5 mm pitch	42	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	Thermal Resistance Junction-Ambient LFBGA 144 - 10 x 10 x 1.7mm	50	°C/W

9 Revision history

Table 44. Document revision history

Date	Revision	Changes
17-Mar-2004	1	First Release
05-Apr-2004	2	Updated “Electrical parameters” on page 34
08-Apr-2004	2.1	Corrected STR712F Pinout. Pins 43/42 swapped.
15-Apr-2004	2.2	PDF hyperlinks corrected.
7-Jul-2004	3	Corrected description of STDBY, V18, VSS18 V18BKP VSSBKP pins Added IDDrun typical data Updated BSPI max. baudrate. Updated “EMI - external memory interface” on page 56
29-Oct-2004	4	Corrected Flash sector B1F0/F1 address in *Figure 6: Memory map on page 31* Corrected *Table 5 on page 25* LQFP64 TEST pin is 16 instead of 17. Added to TQPFP64 column: pin 7 BOOTEN, pin 17 $V_{33IO-PLL}$ Changed description of JTCK from ‘External pull-down required’ to ‘External pull-up or pull down required’.
25-Jan-2005	5	Changed “Product Preview” to “Preliminary Data” on page 1 and 3 Renamed ‘PU/PD’ column to ‘Reset state’ in *Table 5 on page 25* Added reference to STR7 Flash Programming Reference Manual
19-Apr-2005	6	Added STR715F devices and modified RAM size of STR71xF1 devices Added BGA package in *Section 5* Updated ordering information in *Section 7*. Added PLL duty cycle min and max. in *PLL electrical characteristics on page 45*
13-Oct-2005	7	Updated feature description on page 1 Update overview *Section 1.1* Added OD/PP to P0.12 in *Table 5* Changed name of WFI mode to WAIT mode Changed Memory Map *Table 6*: Ext. Memory changed to 64 MB and flash register changed to 36 bytes. Added Power Consumption *Table 13* Modified BGA144 F3, F5, F12 and G12 in *Table 3* and *Table 4* Update EMI Timing *Table 24* and *Figure 29*