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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, HDLC, I²C, SmartCard, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	32
Program Memory Size	256KB (256K x 8 + 16K)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str712fr2t6

List of figures

Table 4. STR710 pin description

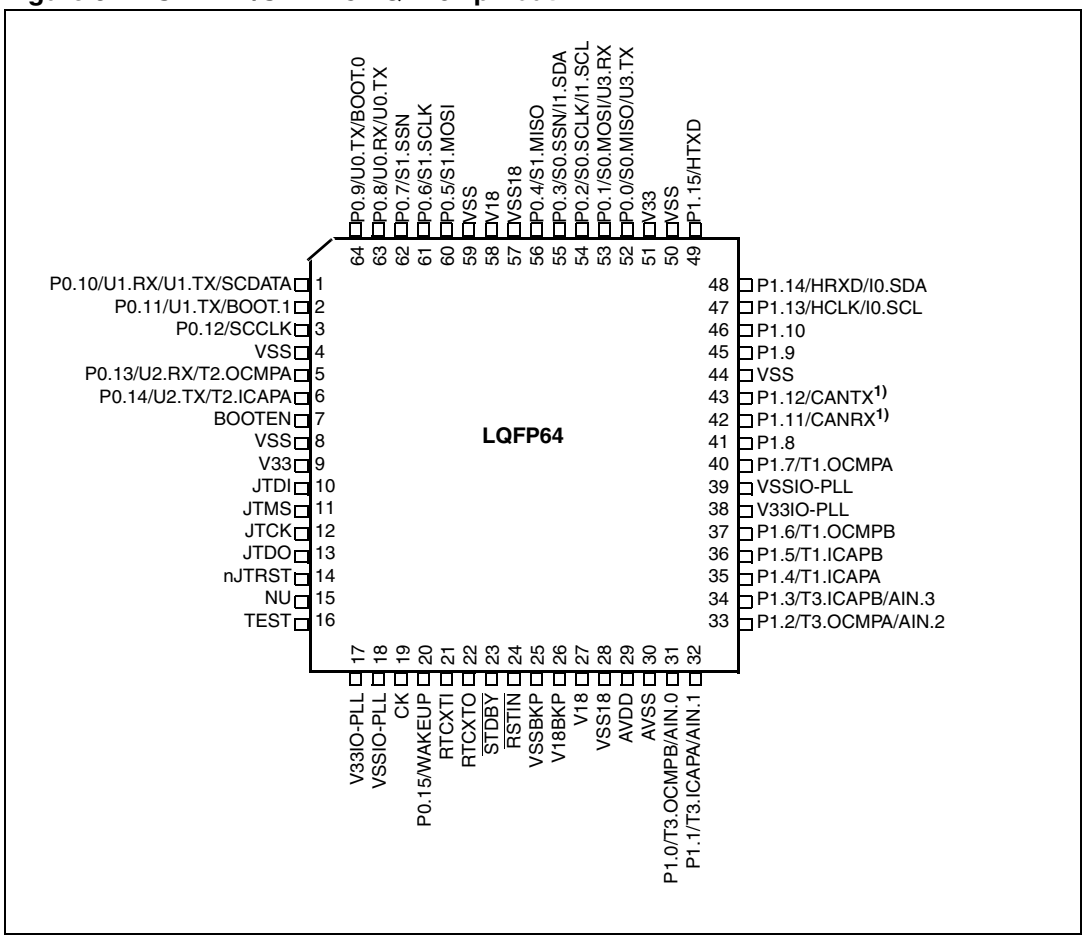
Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
59	L7	V_{SS18}	S								Stabilization for main voltage regulator.		
60	K7	N.C.									Not connected (not bonded)		
61	J7	D.0	I/O	6)			8mA				External Memory Interface: data bus		
62	H7	D.1	I/O	6)			8mA						
63	M8	D.2	I/O	6)			8mA						
64	L8	D.3	I/O	6)			8mA						
65	M10	D.4	I/O	6)			8mA						
66	M11	V_{DDA}	S								Supply voltage for A/D Converter		
67	K8	V_{SSA}	S								Ground voltage for A/D Converter		
68	J8	N.C.									Not connected (not bonded)		
69	M9	N.C.									Not connected (not bonded)		
70	L9	N.C.									Not connected (not bonded)		
71	K9	P1.0/T3.OCMPB/AIN.0	I/O	pu	C_T		4mA	X	X		Port 1.0	Timer 3: Output Compare B	ADC: Analog input 0
72	L10	P1.1/T3.ICAPA/T3.EXTCLK/AIN.1	I/O	pu	C_T		4mA	X	X		Port 1.1	Timer 3: Input Capture A or External Clock input	ADC: Analog input 1
73	M12	P1.2/T3.OCMPA/AIN.2	I/O	pu	C_T		4mA	X	X		Port 1.2	Timer 3: Output Compare A	ADC: Analog input 2
74	L11	P1.3/T3.ICAPB/AIN.3	I/O	pu	C_T		4mA	X	X		Port 1.3	Timer 3: Input Capture B	ADC: Analog input 3
75	K11	P1.4/T1.ICAPA/T1.EXTCLK	I/O	pu	C_T		4mA	X	X		Port 1.4	Timer 1: Input Capture A	Timer 1: External Clock input
76	K10	P1.5/T1.ICAPB	I/O	pu	C_T		4mA	X	X		Port 1.5	Timer 1: Input Capture B	
77	J12	P1.6/T1.OCMPB	I/O	pu	C_T		4mA	X	X		Port 1.6	Timer 1: Output Compare B	
78	J11	D.5	I/O	6)			8mA				External Memory Interface: data bus		
79	L12	D.6	I/O	6)			8mA						
80	K12	D.7	I/O	6)			8mA						
81	J10	D.8	I/O	6)			8mA						
82	J9	D.9	I/O	6)			8mA						

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
107	D10	P1.13/HCLK/ I0.SCL	I/O	pd	C_T	X	4mA	X	X		Port 1.13	HDLC: reference clock input	I2C clock
108	C11	P1.14/HRXD/ I0.SDA	I/O	pu	C_T	X	4mA	X	X		Port 1.14	HDLC: Receive data input	I2C serial data
109	B11	N.C.									Not connected (not bonded)		
110	B10	N.C.									Not connected (not bonded)		
111	C10	P1.15/HTXD	I/O	pu	C_T		4mA	X	X		Port 1.15	HDLC: Transmit data output	
112	A9	V_{SS}	S								Ground voltage for digital I/O circuitry[4]		
113	B9	V_{33}	S								Supply voltage for digital I/O circuitry[4]		
114	C9	A.5	O	[7]			8mA		X		External Memory Interface: address bus		
115	D9	A.6	O	[7]			8mA		X				
116	A11	A.7	O	[7]			8mA		X				
117	A10	A.8	O	[7]			8mA		X				
118	A8	A.9	O	[7]			8mA		X				
119	B8	A.10	O	[7]			8mA		X				
120	C8	A.11	O	[7]			8mA		X				
121	A12	A.12	O	[7]			8mA		X				
122	D8	A.13	O	[7]			8mA		X				
123	E8	P0.0/S0.MISO /U3.TX	I/O	pu	C_T		4mA	X	X		Port 0.0	SPI0 Master in/Slave out data	UART3 Transmit data output
												Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
124	B7	P0.1/S0.MOSI /U3.RX	I/O	pu	C_T	X	4mA	X	X		Port 0.1	BSPI0: Master out/Slave in data	UART3: Receive Data input
												Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	

3.4 Pin description for 64-pin packages

Figure 3. STR712/STR715 LQFP64 pinout



1. CANTX and CANRX in STR712F only, in STR715F they are general purpose I/Os.

Table 5. STR711/STR712/STR715 pin description

Pin n°	Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
1	P0.10/U1.RX/ U1.TX/ SC.DATA	I/O	pd	C_T	X	4mA	T			Port 0.10	UART1: Receive Data input	UART1: Transmit data output.
											Note: This pin may be used for Smartcard DataIn/DataOut or single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress	
2	P0.11/BOOT.1 /U1.TX	I/O	pd	C_T		4mA	X	X		Port 0.11	Select Boot Configuration input	UART1: Transmit data output.
3	P0.12/SC.CLK	I/O	pd	C_T		4mA	X	X		Port 0.12	Smartcard reference clock output	
4	V_{SS}	S								Ground voltage for digital I/Os[2]		
5	P0.13/U2.RX/ T2.OCMPA	I/O	pu	C_T	X	4mA	X	X		Port 0.13	UART2: Receive Data input	Timer2: Output Compare A output
6	P0.14/U2.TX/ T2.ICAPA	I/O	pu	C_T		4mA	X	X		Port 0.14	UART2: Transmit data output	Timer2: Input Capture A input
7	BOOTEN	I		C_T						Boot control input. Enables sampling of BOOT[1:0] pins		
8	V_{SS}	S								Ground voltage for digital I/Os[2]		
9	V_{33}	S								Supply voltage for digital I/Os[2]		
10	JTDI	I		T_T						JTAG Data input. External pull-up required.		
11	JTMS	I		T_T						JTAG Mode Selection Input. External pull-up required.		
12	JTCK	I		C						JTAG Clock Input. External pull-up or pull-down required.		
13	JTDO	O				8mA		X		JTAG Data output. **Note:** Reset state = HiZ.		
14	JTRST	I		T_T						JTAG Reset Input. External pull-up required.		
15	NU									Reserved, must be forced to ground.		
16	TEST									Reserved, must be forced to ground.		
17	$V_{33IO-PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference[2]		
18	$V_{SSIO-PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[2]		
19	CK	I		C						Reference clock input		

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1)]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
52	P0.0/S0.MISO /U3.TX	I/O	pu	C_T		4mA	X	X		Port 0.0	SPI0 Master in/Slave out data	UART3 Transmit data output
											Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
53	P0.1/S0.MOSI /U3.RX	I/O	pu	C_T	X	4mA	X	X		Port 0.1	BSPI0: Master out/Slave in data	UART3: Receive Data input
											Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
54	P0.2/S0.SCLK /I1.SCL	I/O	pu	C_T	X	4mA	X	X		Port 0.2	BSPI0: Serial Clock	I2C1: Serial clock
											Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
55	P0.3/S0.$\overline{SS}$/I1 .SDA	I/O	pu	C_T		4mA	X	X		Port 0.3	SPI0: Slave Select input active low.	I2C1: Serial Data
											Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
56	P0.4/S1.MISO	I/O	pu	C_T		4mA	X	X		Port 0.4	SPI1: Master in/Slave out data	
57	V_{SS18}	S								Stabilization for main voltage regulator.		
58	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
59	V_{SS}	S								Ground voltage for digital I/Os		
60	P0.5/S1.MOSI	I/O	pu	C_T		4mA	X	X		Port 0.5	SPI1: Master out/Slave In data	
61	P0.6/S1.SCLK	I/O	pu	C_T	X	4mA	X	X		Port 0.6	SPI1: Serial Clock	
62	P0.7/S1.$\overline{SS}$	I/O	pu	C_T		4mA	X	X		Port 0.7	SPI1: Slave Select input active low	

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n° LQFP64	Pin name	Type	Reset state[1]	Input: Input level	Input: interrupt	Output: Capability	Output: OD	Output: PP	Active in Stdby	Main function (after reset)	Alternate function	
63	P0.8/U0.RX/U0.TX	I/O	pd	C_T	X	4mA	T			Port 0.8	UART0: Receive Data input	UART0: Transmit data output.
										Note: This pin may be used for single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress		
64	P0.9/U0.TX/BOOT.0	I/O	pd	C_T		4mA	X	X		Port 0.9	Select Boot Configuration input	UART0: Transmit data output

1. The Reset configuration of the I/O Ports is IPUPD (input pull-up/pull down). Refer to *Table 6 on page 30*. The Port bit configuration at reset is PC0=1, PC1=1, PC2=0. The port data register bit (PD) value depends on the pu/pd column which specifies whether the pull-up or pull-down is enabled at reset
2. $V_{33IO\text{-}PLL}$ and V_{33} are internally connected. $V_{SSIO\text{-}PLL}$ and V_{SS} are internally connected.

3.5 External connections

Figure 5. Recommended external connection of V_{18} and V_{18BKP} pins

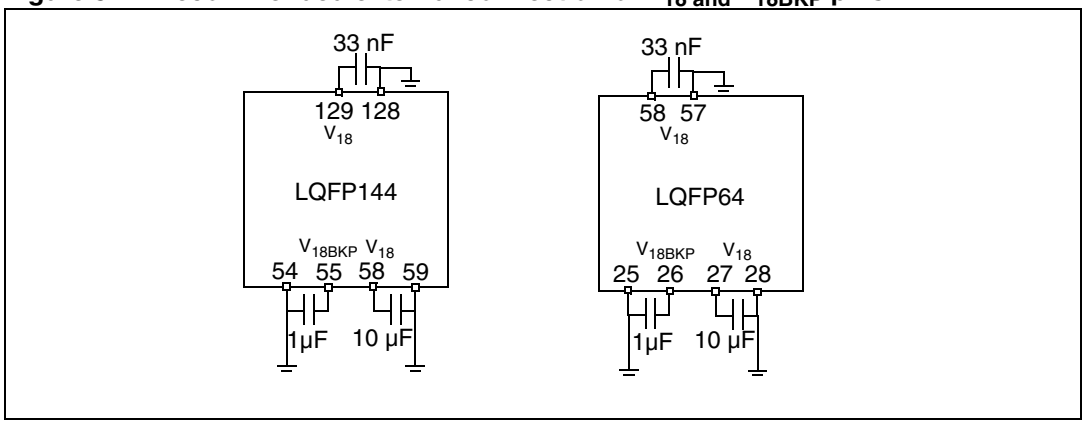


Figure 7. Mapping of Flash memory versions

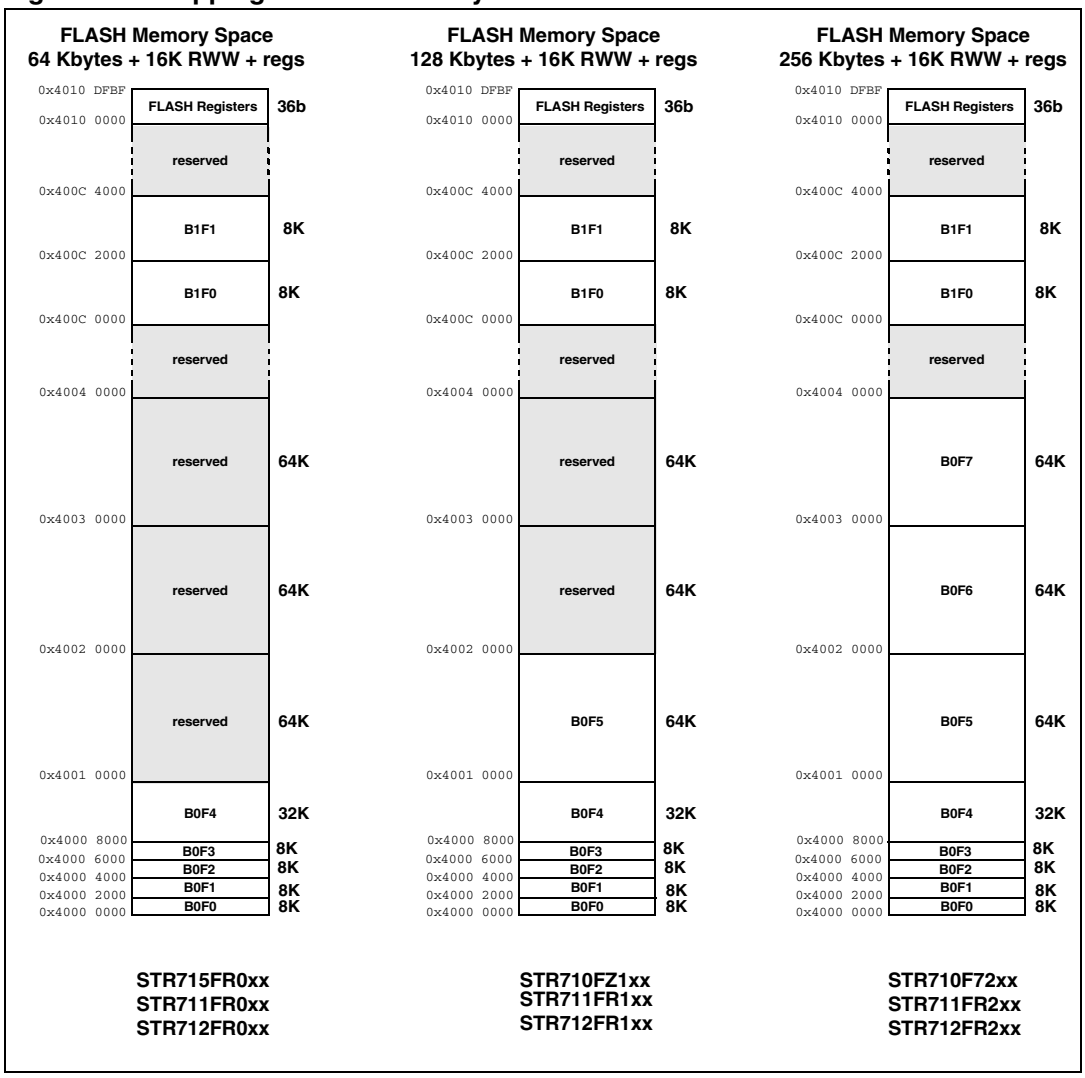


Table 7. RAM memory mapping

Part number	RAM size	Start address	End address
STR715FR0xx STR711FR0xx STR712FR0xx	16 Kbytes	0x2000 0000	0x2000 3FFF
STR710FZ1xx STR711FR1xx STR712FR1xx	32 Kbytes	0x2000 0000	0x2000 7FFF
STR710FR2xx STR710Rxx STR711FR2xx STR712FR2xx	64 Kbytes	0x2000 0000	0x2000 FFFF

4.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{33}- V_{SS}	External 3.3V Supply voltage (including AV_{DD} and $V_{33IO-PLL}$)[2]	-0.3	4.0	V
V_{18BKP} - V_{SSBKP}	Digital 1.8V Supply voltage on V_{18BKP} backup supply [2]	-0.3	2.0	
V_{IN}	Input voltage on true open drain pin (P0.10) [1]	V_{SS}-0.3	+5.5	
	Input voltage on any other pin [1]	V_{SS}-0.3	V_{33}+0.3	
$\|\Delta V_{33x}\|$	Variations between different 3.3V power pins	50	50	mV
$\|\Delta V_{18x}\|$	Variations between different 1.8V power pins [5]	25	25	
$\|V_{SSX}$ - $V_{SS}\|$	Variations between all the different ground pins	50	50	
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	see *: Absolute maximum ratings (electrical sensitivity) on page 49*		
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)			

4.3.2 Clock and timing characteristics

External clock sources

Subject to general operating conditions for V_{33}, and T_A.

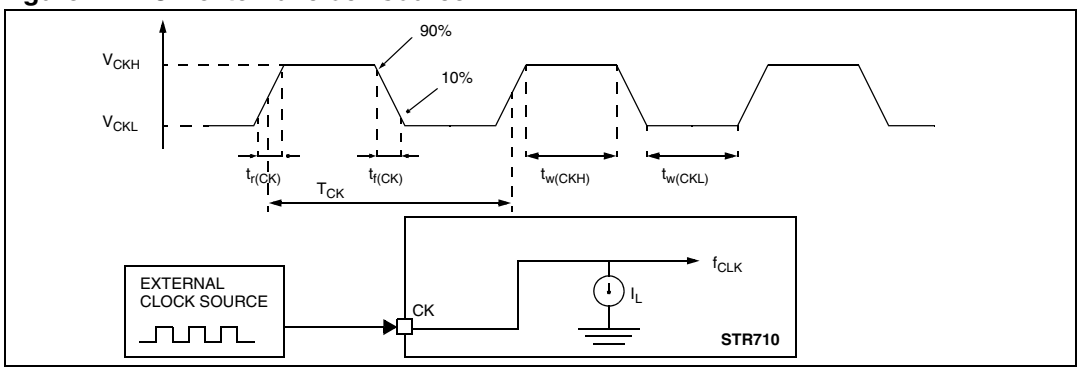
Table 16. CK external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	External clock source frequency		0		16.5	MHz
V_{CKH}	CK input pin high level voltage		$0.7xV_{33}$		V_{33}	V
V_{CKL}	CK input pin low level voltage		V_{SS}		$0.3xV_{33}$	
$t_{w(CK)}$ $t_{w(CK)}$	CK high or low time 1)		25			ns
$t_{r(CK)}$ $t_{f(CK)}$	CK rise or fall time 1)				20	
$C_{IN(CK)}$	CK input capacitance 1)			5		pF
DuCy(XT1)	Duty cycle		40		60	%
I_L	CK Input leakage current	$V_{SS} \leq V_{IN} \leq V_{33}$			±1	µA

Notes:

1. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 14. CK external clock source



4.3.5 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{33} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 27. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage 1)	CMOS ports			$0.3V_{33}$	V
V_{IH}	Input high level voltage 1)		$0.7V_{33}$			
V_{hys}	Schmitt trigger voltage hysteresis 2)			0.8		V
V_{IL}	Input low level voltage 1)	P0.15 WAKEUP		0.9	0.8	V
V_{IH}	Input high level voltage 1)		2	1.35		
V_{hys}	Schmitt trigger voltage hysteresis 2)			0.4		V
V_{IL}	Input low level voltage 1)	TTL ports			0.8	V
V_{IH}	Input high level voltage 1)		2.0			
$I_{INJ(PIN)}$	Injected Current on any I/O pin				± 4	mA
$\Sigma I_{INJ(PIN)}$ 3)	Total injected current (sum of all I/O and control pins)				± 25	
I_{lkg}	Input leakage current 4)	$V_{SS} \le V_{IN} \le V_{33}$			±1	µA
R_{PU}	Weak pull-up equivalent resistor5)	$V_{IN}=V_{SS}$	110	150	700	kΩ
R_{PD}	Weak pull-down equivalent resistor5)	$V_{IN}=V_{33}$	110	150	700	kΩ
C_{IO}	I/O pin capacitance			5		pF

Notes:

1. Data based on characterization results, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
3. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{33}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Refer to *Section 4.2 on page 35* for more details.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. The R_{PU} pull-up and R_{PD} pull-down equivalent resistor are based on a resistive transistor (corresponding I_{PU} and I_{PD} current characteristics described in *Figure 18* to *Figure 19*).

4.3.6 TIM timer characteristics

Subject to general operating conditions for V_{33}, f_{MCLK}, and T_A unless otherwise specified.

Refer to *Section 4.3.5: I/O port pin characteristics on page 51* for more details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output...).

Table 30. TIM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time		2			t_{CK_TIM}
$t_{res(TIM)}$	Timer resolution time		1			t_{PCLK2}
		f_{PCLK2} = 30 MHz	33.3			ns
f_{EXT}	Timer external clock frequency	$f_{CK\_TIM(MAX)} = f_{MCLK}$	0		$f_{CK\_TIM}/4$	MHz
		$f_{CK\_TIM} = f_{MCLK}$ = 60 MHz	0		15	MHz
Res_{TIM}	Timer resolution				16	bit
$t_{COUNTER}$	16-bit Counter clock period when internal clock is selected		1		65536	t_{PCLK2}
		f_{PCLK2} = 30 MHz	0.033		2184	µs
T_{MAX_COUNT}	Maximum Possible Count				65536x 65536	t_{PCLK}
		f_{PCLK2} = 30 MHz			143.1	s

4.3.7 EMI - external memory interface

Subject to general operating conditions for V_{DD}, f_{HCLK}, and T_A unless otherwise specified.

The tables below use a variable which is derived from the EMI_BCONn registers (described in the STR71x Reference Manual) and represents the special characteristics of the programmed memory cycle.

Table 31. EMI general characteristics

Symbol	Parameter	Value
t_{MCLK}	CPU clock period	1 / f_{MCLK}
t_C	Memory cycle time wait states	t_{MCLK} x (1 + [C_LENGTH])

Table 32. EMI read operation

Symbol	Parameter	Test Conditions	Value			Unit
			Min[1)]	Typ	Max[1)]	
t_{RCR}	Read to CSn Removal Time	MCLK=50 MHz 4 wait states 50 pf load on all pins	19	t_{MCLK}	21	ns
t_{RP}	Read Pulse Time		98	t_C	100	ns
t_{RDS}	Read Data Setup Time		22			ns
t_{RDH}	Read Data Hold Time		0			ns
t_{RAS}	Read Address Setup Time		27	$1.5*t_{MCLK}$	33	ns
t_{RAH}	Read Address Hold Time		0.65		2	ns
t_{RAT}	Read Address Turnaround Time		1.9		3.25	ns
t_{RRT}	RDn Turnaround Time		20	t_{MCLK}	21	ns

See *Figure 25*, *Figure 26*, *Figure 27* and *Figure 28* for related timing diagrams.

1. Data based on characterisation results, not tested in production.

Table 33. EMI write operation

Symbol	Parameter	Test conditions	Value			Unit
			Min[1)]	Typ	Max[1)]	
t_{WCR}	WEn to CSn Removal Time	MCLK=50 MHz 3 wait states 50 pf load on all pins	20	t_{MCLK}	22.5	ns
t_{WP}	Write Pulse Time		77.5	t_C	80	ns
t_{WDS1}	Write Data Setup Time 1		97	$t_C + t_{MCLK}$	100	ns
t_{WDS2}	Write Data Setup Time 2		77	t_C	80	ns
t_{WDH}	Write Data Hold Time		20	t_{MCLK}	23	ns
t_{WAS}	Write Address Setup Time		27	$1.5*t_{MCLK}$	33	ns
t_{WAH}	Write Address Hold Time		0.6		3	ns
t_{WAT}	Write Address Turnaround Time		1.75		4.1	ns
t_{WWT}	WEn Turnaround Time		20	t_{MCLK}	23	ns

See *Figure 29*, *Figure 30*, *Figure 31* and *Figure 32* for related timing diagrams.

1. Data based on characterisation results, not tested in production.

4.3.9 BSPI - buffered serial peripheral interface

Subject to general operating conditions for V_{DD}, T_A and f_{PCLK1} ,unless otherwise specified.

Refer to *I/O port pin characteristics on page 51* for more details on the input/output alternate function characteristics ($\overline{SS}$, SCK, MOSI, MISO).

Table 36. BSPI characteristics

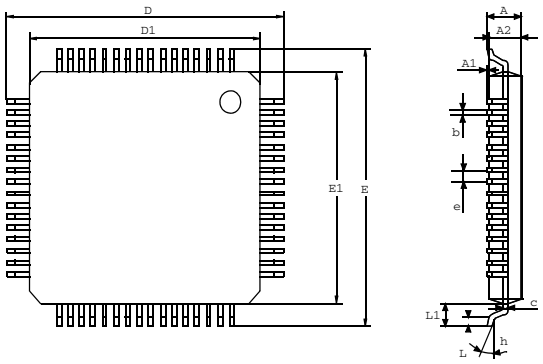
Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master	$f_{PCLK1}/254$	$f_{PCLK1}/6$ 5.5	MHz
		Slave	0	$f_{PCLK1}/8$ 3.3	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	capacitive charge C=50 pF		14	ns
$t_{su(\overline{SS})}$ (1)	$\overline{SS}$ setup time	Slave	0		
$t_{h(\overline{SS})}$ (1)	$\overline{SS}$ hold time	Slave	0		
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master f_{PCLK1}=33 MHz, presc = 6	73		
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master Slave	7 0		
$t_{h(MI)}$ 1)(2) $t_{h(SI)}$ 1)(2)	Data input hold time	Master Slave	$1xt_{PCLK1}$ $2xt_{PCLK1}$		
$t_{h(MI)}$ (1) $t_{h(SI)}$ (1)	Data input hold time	Master f_{PCLK1}=33 MHz Slave f_{PCLK1}=33 MHz	30 60		
$t_{a(SO)}$ 1)(3)	Data output access time	Slave	0	$1.5xt_{PCLK1}+42$	
		Slave f_{PCLK1}=33 MHz	0	87	
$t_{dis(SO)}$ (1)(4)	Data output disable time	Slave	0	42	
$t_{v(SO)}$ (1)(2)	Data output valid time	Slave (after enable edge)		$3xt_{PCLK1}+45$	
		f_{PCLK1}=33 MHz		135	
$t_{h(SO)}$ (1)	Data output hold time	Slave (after enable edge)	0		
$t_{v(MO)}$ (1)(2)	Data output valid time	Master (after enable edge)		$2xt_{PCLK1}+12$	
		f_{PCLK1}=33 MHz		72	
$t_{h(MO)}$ (1)	Data output hold time	Master (after enable edge)	0		

1. Data based on design simulation and/or characterisation results, not tested in production.
2. Depends on f_{PCLK1}. For example, if f_{PCLK1}=8 MHz, then t_{PCLK1} = $1/f_{PCLK1}$ =125 ns and $t_{v(MO)}$ = 255 ns.
3. Min. time is the minimum time to drive the output and the max. time is the maximum time to validate the data.
4. Min time is the minimun time to invalidate the output and the max time is the maximum time to put the data in Hi-Z.

5 Package characteristics

5.1 Package mechanical data

Figure 40. 64-Pin low profile quad flat package (10x10)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
E		12.00			0.472	
E1		10.00			0.394	
e		0.50			0.020	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	64					

Recommended footprint (dimensions in mm)

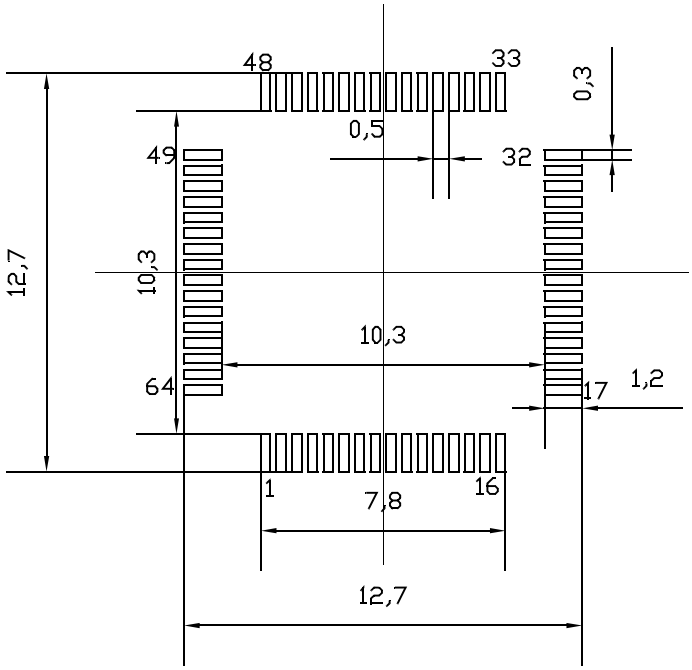


Figure 47. BGA144 STR710 version “Z”

Figure 48. BGA64 STR711 version “X”

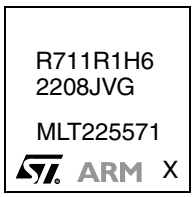
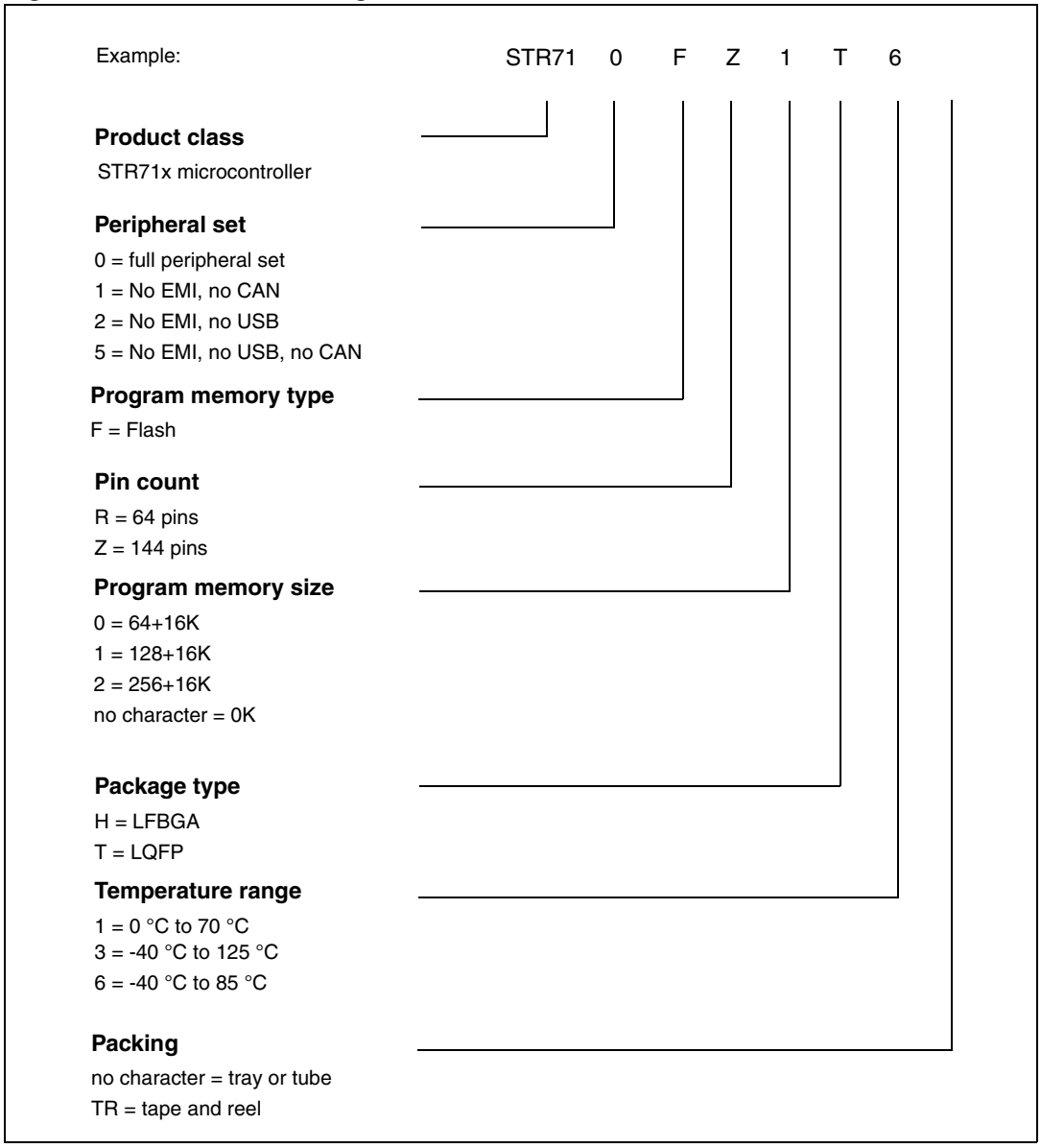


Table 43. A, Z and X version differences

Feature	A version	Z version	X version
ARM7TDMI core device Identification (ID) code register (see ARM7TDMI Technical Reference Manual)	Version bits [31:28] = 0001	Version bits [31:28] = 0010	Version bits [31:28] = 0010
Low power mode consumption in STOP mode at 25 °C	Not guaranteed Typical 49 µA	50 µA maximum at 25°C. Less than 30 µA at 25 °C for 99.730020% of parts	Same as Z.
SC.DATA pin	Not TRUE open drain When addressing 5V cards, the SCDATA Line must be connected to an open drain buffer.		Pin P0.10/U1.RX/U1.TX/SC.DATA has been modified to offer TRUE OPEN DRAIN functionality when in Smartcard mode. When addressing 5V cards, the SCDATA line can now be connected directly to the card I/O. This modification is backward compatible with previous designs, and no board modification is required.

7 Ordering information

Figure 49. STR71xF ordering information scheme



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to www.st.com or contact the ST Sales Office nearest to you.

9 Revision history

Table 44. Document revision history

Date	Revision	Changes
17-Mar-2004	1	First Release
05-Apr-2004	2	Updated “Electrical parameters” on page 34
08-Apr-2004	2.1	Corrected STR712F Pinout. Pins 43/42 swapped.
15-Apr-2004	2.2	PDF hyperlinks corrected.
7-Jul-2004	3	Corrected description of STDBY, V18, VSS18 V18BKP VSSBKP pins Added IDDrun typical data Updated BSPI max. baudrate. Updated “EMI - external memory interface” on page 56
29-Oct-2004	4	Corrected Flash sector B1F0/F1 address in *Figure 6: Memory map on page 31* Corrected *Table 5 on page 25* LQFP64 TEST pin is 16 instead of 17. Added to TQPFP64 column: pin 7 BOOTEN, pin 17 $V_{33IO-PLL}$ Changed description of JTCK from ‘External pull-down required’ to ‘External pull-up or pull down required’.
25-Jan-2005	5	Changed “Product Preview” to “Preliminary Data” on page 1 and 3 Renamed ‘PU/PD’ column to ‘Reset state’ in *Table 5 on page 25* Added reference to STR7 Flash Programming Reference Manual
19-Apr-2005	6	Added STR715F devices and modified RAM size of STR71xF1 devices Added BGA package in *Section 5* Updated ordering information in *Section 7*. Added PLL duty cycle min and max. in *PLL electrical characteristics on page 45*
13-Oct-2005	7	Updated feature description on page 1 Update overview *Section 1.1* Added OD/PP to P0.12 in *Table 5* Changed name of WFI mode to WAIT mode Changed Memory Map *Table 6*: Ext. Memory changed to 64 MB and flash register changed to 36 bytes. Added Power Consumption *Table 13* Modified BGA144 F3, F5, F12 and G12 in *Table 3* and *Table 4* Update EMI Timing *Table 24* and *Figure 29*

Table 44. Document revision history (continued)

Date	Revision	Changes
22-May-2006	8	Added Flashless device. Changed reset state of pins P1.10 and P1.13 from pu to pd, P0.15 from pu to floating and removed x in interrupt column for P1.15 and P1.12 in *Table 4* and *Table 5* Added notes under *Table 4* on EMI pin reset state. Corrected inch value for d3 in *Figure 40* Added footprint diagrams in *Figure 40* and *Figure 43* Updated *Section 4: Electrical parameters*
01-Aug-2006	9	Flash data retention changed to 20 years at 85° C. Changed note 8 on page 19 Changed note 1 on page 45
06-Nov-2006	10	Added STR715FR0T1 in *Table 42: Order codes* P0.12 corrected in *Table 5 on page 25*
20-Mar-2007	11	Added characteristics of *BSPI - buffered serial peripheral interface on page 63* Updated *Table 21: Low-power mode wakeup timing on page 46*
13-Feb-2008	12	Updated ordering information Updated USB characteristics Updated external clock characteristics
03-Apr-2013	13	Updated title (to be in line with the “device summary” table) Updated ST Logo and Disclaimer Added *Section 8: Known limitations*