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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	I²C, HDLC, SmartCard, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8 + 16K)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/str715fr0t1

Realtime clock (RTC)

The RTC provides a set of continuously running counters driven by the 32 kHz external crystal. The RTC can be used as a general timebase or clock/calendar/alarm function. When the STR71x is in Standby mode the RTC can be kept running, powered by the low power voltage regulator and driven by the 32 kHz external crystal.

UARTs

The 4 UARTs allow full duplex, asynchronous, communications with external devices with independently programmable TX and RX baud rates up to 1.25 Mb/s.

Smartcard interface

UART1 is configurable to function either as a general purpose UART or as an asynchronous Smartcard interface as defined by ISO 7816-3. It includes Smartcard clock generation and provides support features for synchronous cards.

Buffered serial peripheral interfaces (BSPI)

Each of the two SPIs allow full duplex, synchronous communications with external devices, master or slave communication at up to 5.5 Mb/s in Master mode and 4 Mb/s in Slave mode.

I^2C interfaces

The two I^2C Interfaces provide multi-master and slave functions, support normal and fast I^2C mode (400 kHz) and 7 or 10-bit addressing modes.

One I^2C Interface is multiplexed with one SPI, so either 2xSPI+1x I^2C or 1xSPI+2x I^2C may be used at a time.

HDLC interface

The High Level Data Link Controller (HDLC) unit supports full duplex operation and NRZ, NRZI, FM0 or MANCHESTER protocols. It has an internal 8-bit baud rate generator.

A/D converter

The Analog to Digital Converter, converts in single channel or up to 4 channels in single-shot or round robin mode. Resolution is 12-bit with a sampling frequency of up to 1 kHz. The input voltage range is 0-2.5V.

Watchdog

The 16-bit Watchdog Timer protects the application against hardware or software failures and ensures recovery by generating a reset.

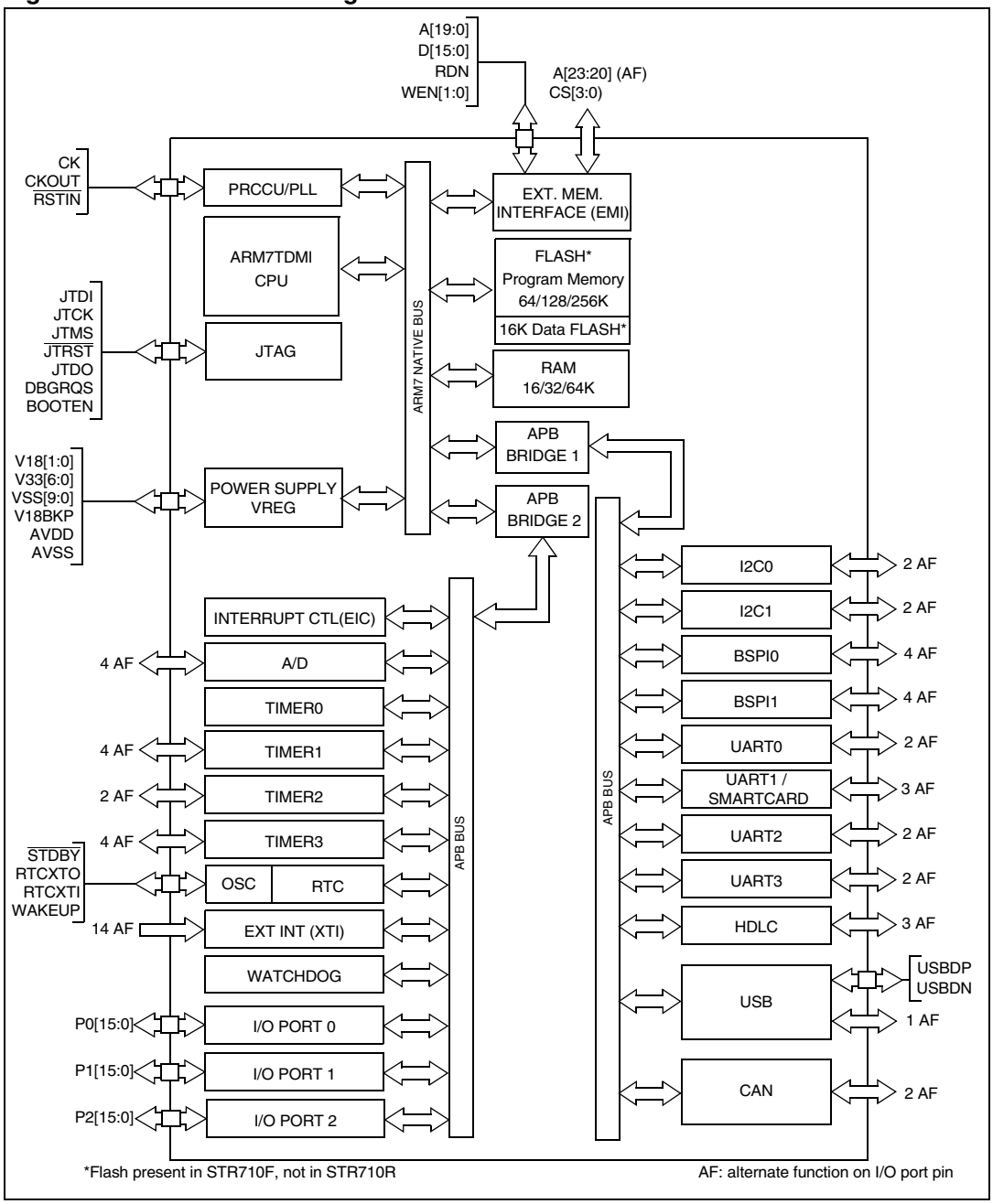
I/O ports

The 48 I/O ports are programmable as Inputs or Outputs.

External interrupts

Up to 14 external interrupts are available for application use or to wake up the application from STOP mode.

Figure 1. STR71x block diagram



3.3 Pin description for 144-pin packages

Figure 2. STR710 LQFP pinout

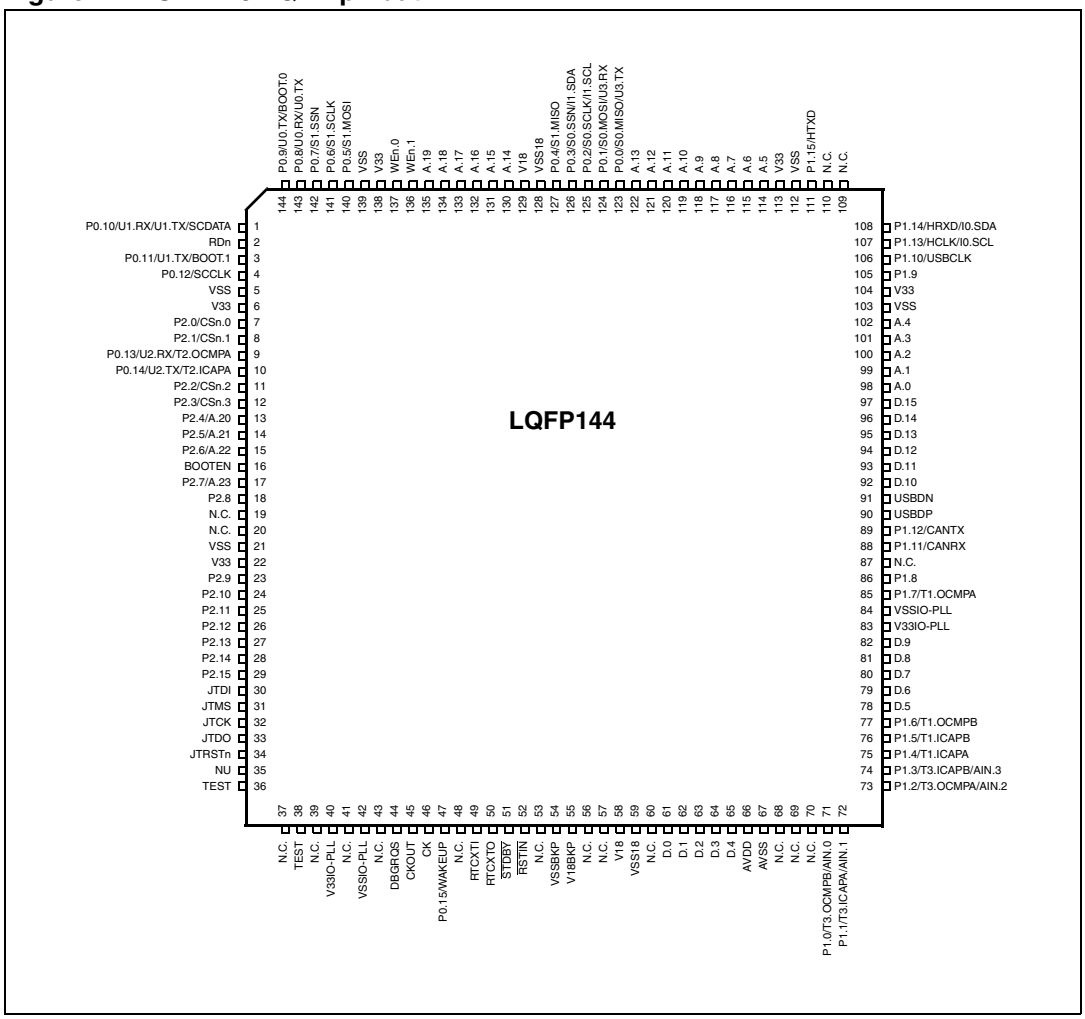


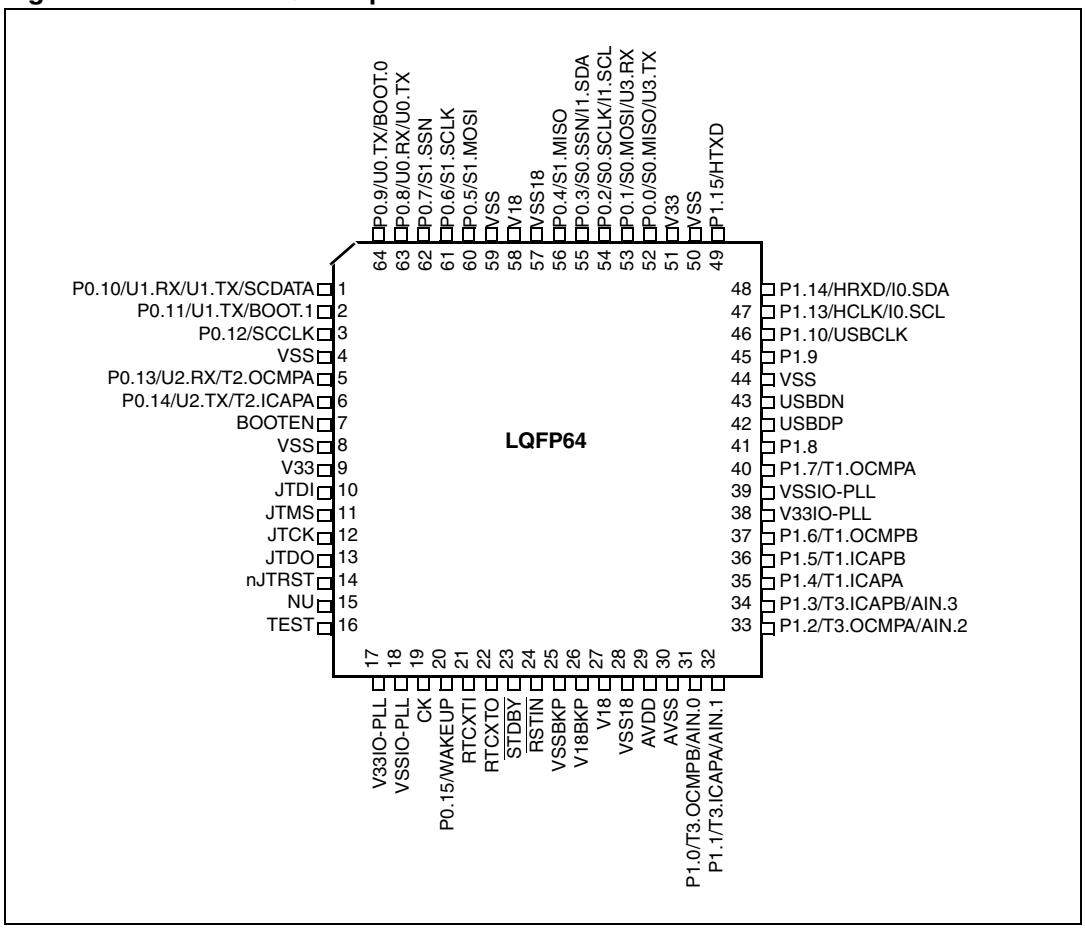
Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP			
40	K3	$V_{33IO-PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference	
41	M4	N.C.									Not connected (not bonded)	
42	L4	$V_{SSIO-PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[4]	
43	M2	N.C.									Not connected (not bonded)	
44	M3	DBGRQS	I		C_T						Debug Mode request input (active high)	
45	K4	CKOUT	O				8mA		X		Clock output (f_{PCLK2}) **Note:** Enabled by CKDIS register in APB Bridge 2	
46	J4	CK	I		C						Reference clock input	
47	M5	P0.15/ WAKEUP	I		T_T	X				X	Port 0.15	Wakeup from Standby mode input. **Note:** This port is input only.
48	L5	N.C.									Not connected (not bonded)	
49	K5	RTCXTI									Realtime Clock input and input of 32 kHz oscillator amplifier circuit	
50	J5	RTCXTO									Output of 32 kHz oscillator amplifier circuit	
51	M6	$\overline{STDBY}$	I/O		C_T		4mA	X		X	Input: Hardware Standby mode entry input active low. **Caution:** External pull-up to V_{33} required to select normal mode. Output: Standby mode active low output following Software Standby mode entry. **Note**: In Standby mode all pins are in high impedance except those marked Active in Stdby	
52	M7	$\overline{RSTIN}$	I		C_T					X	Reset input	
53	H5	N.C.									Not connected (not bonded)	
54	L6	V_{SSBKP}			S					X	Stabilization for low power voltage regulator.	
55	K6	V_{18BKP}			S					X	Stabilization for low power voltage regulator. Requires external capacitors of at least 1µF between V_{18BKP} and $V_{SS18BKP}$. See *Figure 5*. **Note:** If the low power voltage regulator is bypassed, this pin can be connected to an external 1.8V supply.	
56	J6	N.C.									Not connected (not bonded)	
57	H6	N.C.									Not connected (not bonded)	
58	G6	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.	

Table 4. STR710 pin description

Pin n°		Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP144	BGA144				Input level	interrupt	Capability	OD	PP				
125	A7	P0.2/S0.SCLK /I1.SCL	I/O	pu	C_T	X	4mA	X	X		Port 0.2	BSPI0: Serial Clock	I2C1: Serial clock
												Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
126	A6	P0.3/S0.$\overline{SS}$/ I1.SDA	I/O	pu	C_T		4mA	X	X		Port 0.3	SPI0: Slave Select input active low.	I2C1: Serial Data
												Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
127	C7	P0.4/S1.MISO	I/O	pu	C_T		4mA	X	X		Port 0.4	SPI1: Master in/Slave out data	
128	D7	V_{SS18}	S								Stabilization for main voltage regulator.		
129	E7	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
130	F7	A.14	O	7)			8mA		X		External Memory Interface: address bus		
131	B6	A.15	O	7)			8mA		X				
132	C6	A.16	O	7)			8mA		X				
133	D6	A.17	O	7)			8mA		X				
134	E6	A.18	O	7)			8mA		X				
135	A5	A.19	O	7)			8mA		X				
136	B5	$\overline{WE}$.1	O	5)			8mA		X		External Memory Interface: active low MSB write enable output		
137	C5	$\overline{WE}$.0	O	5)			8mA		X		External Memory Interface: active low LSB write enable output		
138	A3	V_{33}	S								Supply voltage for digital I/Os[4]		
139	A2	V_{SS}	S								Ground voltage for digital I/Os[4]		
140	D5	P0.5/S1.MOSI	I/O	pu	C_T		4mA	X	X		Port 0.5	SPI1: Master out/Slave In data	
141	A4	P0.6/S1.SCLK	I/O	pu	C_T	X	4mA	X	X		Port 0.6	SPI1: Serial Clock	
142	B4	P0.7/S1.$\overline{SS}$	I/O	pu	C_T		4mA	X	X		Port 0.7	SPI1: Slave Select input active low	

Figure 4. STR711 LQFP64 pinout



Legend / abbreviations for *Table 5*:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: C = CMOS $0.3V_{DD}/0.7V_{DD}$
C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger
T_T= TTL 0.8V / 2V with input trigger
C/T = Programmable levels: CMOS $0.3V_{DD}/0.7V_{DD}$ or TTL 0.8V / 2V

Port and control configuration:

Input: pu/pd= software enabled internal pull-up or pull down
pu= in reset state, the internal 100kΩ weak pull-up is enabled.
pd = in reset state, the internal 100kΩ weak pull-down is enabled.

Output: OD = open drain (logic level)
PP = push-pull
T = true OD, (P-Buffer and protection diode to V_{DD} not implemented), 5V tolerant.

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1)]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
20	P0.15/ WAKEUP	I		T_T	X				X	Port 0.15	Wakeup from Standby mode input.	
										Note: This port is input only.		
21	RTCXTI									Realtime Clock input and input of 32 kHz oscillator amplifier circuit		
22	RTCXTO									Output of 32 kHz oscillator amplifier circuit		
23	$\overline{STDBY}$	I/O		C_T		4mA	X		X	Input: Hardware Standby mode entry input active low. **Caution:** External pull-up to V_{33} required to select normal mode. Output: Standby mode active low output following Software Standby mode entry. **Note**: In Standby mode all pins are in high impedance except those marked Active in Stdby.		
24	$\overline{RSTIN}$	I		C_T					X	Reset input		
25	V_{SSBKP}			S					X	Stabilization for low power voltage regulator.		
26	V_{18BKP}			S					X	Stabilization for low power voltage regulator. Requires external capacitors of at least 1µF between V_{18BKP} and $V_{SS18BKP}$. See *Figure 5*. **Note:** If the low power voltage regulator is bypassed, this pin can be connected to an external 1.8V supply.		
27	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
28	V_{SS18}	S								Stabilization for main voltage regulator.		
29	V_{DDA}	S								Supply voltage for A/D Converter		
30	V_{SSA}	S								Ground voltage for A/D Converter		
31	P1.0/T3.OCMPB/AIN.0	I/O	pu	C_T		4mA	X	X		Port 1.0	Timer 3: Output Compare B	ADC: Analog input 0
32	P1.1/T3.ICAPA/T3.EXTCLK/AIN.1	I/O	pu	C_T		4mA	X	X		Port 1.1	Timer 3: Input Capture A or External Clock input	ADC: Analog input 1
33	P1.2/T3.OCMPA/AIN.2	I/O	pu	C_T		4mA	X	X		Port 1.2	Timer 3: Output Compare A	ADC: Analog input 2
34	P1.3/T3.ICAPB/AIN.3	I/O	pu	C_T		4mA	X	X		Port 1.3	Timer 3: Input Capture B	ADC: Analog input 3
35	P1.4/T1.ICAPA/T1.EXTCLK	I/O	pu	C_T		4mA	X	X		Port 1.4	Timer 1: Input Capture A	Timer 1: External Clock input

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
36	P1.5/T1.ICAPB	I/O	pu	C_T		4mA	X	X		Port 1.5	Timer 1: Input Capture B	
37	P1.6/T1.OCMPB	I/O	pu	C_T		4mA	X	X		Port 1.6	Timer 1: Output Compare B	
38	$V_{33IO-PLL}$	S								Supply voltage for digital I/O circuitry and for PLL reference[2]		
39	$V_{SSIO-PLL}$	S								Ground voltage for digital I/O circuitry and for PLL reference[2]		
40	P1.7/T1.OCMPA	I/O	pu	C_T		4mA	X	X		Port 1.7	Timer 1: Output Compare A	
41	P1.8	I/O	pd	C_T		4mA	X	X		Port 1.8		
42	P1.11/CANRX	I/O	pu	C_T	X	4mA	X	X		Port 1.11	CAN: receive data input **Note:** On STR710 and STR712 only	
43	P1.12/CANTX	I/O	pu	C_T		4mA	X	X		Port 1.12	CAN: Transmit data output **Note:** On STR710 and STR712 only	
42	USBDP	I/O		C_T						USB bidirectional data (data +). Reset state = HiZ **Note:** On STR710 and STR711 only This pin requires an external pull-up to V_{33} to maintain a high level.		
43	USBDN	I/O		C_T						USB bidirectional data (data -). Reset state = HiZ **Note:** On STR710 and STR711 only.		
44	V_{SS}	S								Ground voltage for digital I/O circuitry[2]		
45	P1.9	I/O	pd	C_T		4mA	X	X		Port 1.9		
46	P1.10/USBCLK	I/O	pd	C/T		4mA	X	X		Port 1.10	USB: 48 MHZ clock input	
47	P1.13/HCLK/I0.SCL	I/O	pd	C_T	X	4mA	X	X		Port 1.13	HDLC: reference clock input	I2C clock
48	P1.14/HRXD/I0.SDA	I/O	pu	C_T	X	4mA	X	X		Port 1.14	HDLC: Receive data input	I2C serial data
49	P1.15/HTXD	I/O	pu	C_T		4mA	X	X		Port 1.15	HDLC: Transmit data output	
50	V_{SS}	S								Ground voltage for digital I/O circuitry[2]		
51	V_{33}	S								Supply voltage for digital I/O circuitry[2]		

Table 5. STR711/STR712/STR715 pin description (continued)

Pin n°	Pin name	Type	Reset state[1)]	Input		Output			Active in Stdby	Main function (after reset)	Alternate function	
LQFP64				Input level	interrupt	Capability	OD	PP				
52	P0.0/S0.MISO /U3.TX	I/O	pu	C_T		4mA	X	X		Port 0.0	SPI0 Master in/Slave out data	UART3 Transmit data output
											Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
53	P0.1/S0.MOSI /U3.RX	I/O	pu	C_T	X	4mA	X	X		Port 0.1	BSPI0: Master out/Slave in data	UART3: Receive Data input
											Note: Programming AF function selects UART by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
54	P0.2/S0.SCLK /I1.SCL	I/O	pu	C_T	X	4mA	X	X		Port 0.2	BSPI0: Serial Clock	I2C1: Serial clock
											Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
55	P0.3/S0.$\overline{SS}$/I1 .SDA	I/O	pu	C_T		4mA	X	X		Port 0.3	SPI0: Slave Select input active low.	I2C1: Serial Data
											Note: Programming AF function selects I2C by default. BSPI must be enabled by SPI_EN bit in the BOOTCR register.	
56	P0.4/S1.MISO	I/O	pu	C_T		4mA	X	X		Port 0.4	SPI1: Master in/Slave out data	
57	V_{SS18}	S								Stabilization for main voltage regulator.		
58	V_{18}	S								Stabilization for main voltage regulator. Requires external capacitors of at least 10µF + 33nF between V_{18} and V_{SS18}. See *Figure 5*.		
59	V_{SS}	S								Ground voltage for digital I/Os		
60	P0.5/S1.MOSI	I/O	pu	C_T		4mA	X	X		Port 0.5	SPI1: Master out/Slave In data	
61	P0.6/S1.SCLK	I/O	pu	C_T	X	4mA	X	X		Port 0.6	SPI1: Serial Clock	
62	P0.7/S1.$\overline{SS}$	I/O	pu	C_T		4mA	X	X		Port 0.7	SPI1: Slave Select input active low	

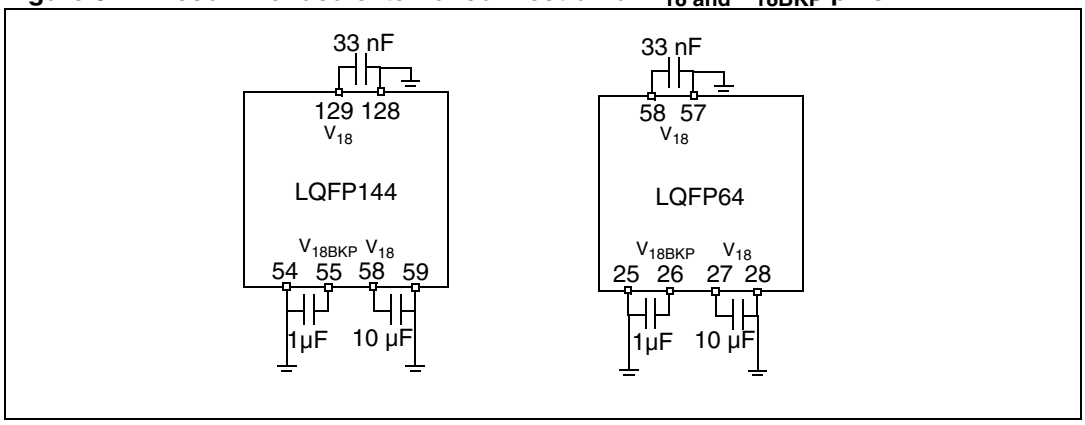
Table 5. STR711/STR712/STR715 pin description (continued)

Pin n° LQFP64	Pin name	Type	Reset state[1]	Input: Input level	Input: interrupt	Output: Capability	Output: OD	Output: PP	Active in Stdby	Main function (after reset)	Alternate function	
63	P0.8/U0.RX/U0.TX	I/O	pd	C_T	X	4mA	T			Port 0.8	UART0: Receive Data input	UART0: Transmit data output.
										Note: This pin may be used for single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress		
64	P0.9/U0.TX/BOOT.0	I/O	pd	C_T		4mA	X	X		Port 0.9	Select Boot Configuration input	UART0: Transmit data output

1. The Reset configuration of the I/O Ports is IPUPD (input pull-up/pull down). Refer to *Table 6 on page 30*. The Port bit configuration at reset is PC0=1, PC1=1, PC2=0. The port data register bit (PD) value depends on the pu/pd column which specifies whether the pull-up or pull-down is enabled at reset
2. $V_{33IO\text{-}PLL}$ and V_{33} are internally connected. $V_{SSIO\text{-}PLL}$ and V_{SS} are internally connected.

3.5 External connections

Figure 5. Recommended external connection of V_{18} and V_{18BKP} pins



3.6 I/O port configuration

Table 6. Port bit configuration table

Configuration mode		Input buffer	PxD register		PxC2 register	PxC1 register	PxC0 register
			Read access	Write access			
INPUT	TTL Input Floating	TTL floating	I/O pin	don't care	0	0	1
	CMOS Input Floating	CMOS floating	I/O pin	don't care	0	1	0
	CMOS Input Pull-Down (IPUPD)	CMOS Pull-Down	I/O pin	0	0	1	1
	CMOS Input Pull-Up (IPUPD)	CMOS Pull-Up	I/O pin	1	0	1	1
	Analog input	AIN	0	don't care	0	0	0
OUTPUT	Output Open-Drain	N.A.	I/O pin	0 or 1	1	0	0
	Output Push-Pull	N.A.	last value written	0 or 1	1	0	1
	Alternate Function Open-Drain	CMOS floating	I/O pin	don't care	1	1	0
	Alternate Function Push-Pull	CMOS floating	I/O pin	don't care	1	1	1

Legend:

AIN: Analog Input

CMOS: CMOS Input levels

IPUPD: Input Pull Up /Pull Down

TTL: TTL Input levels

N.A.: not applicable. In Output mode, a read access to the port gets the output latch value.

Figure 8. External memory map

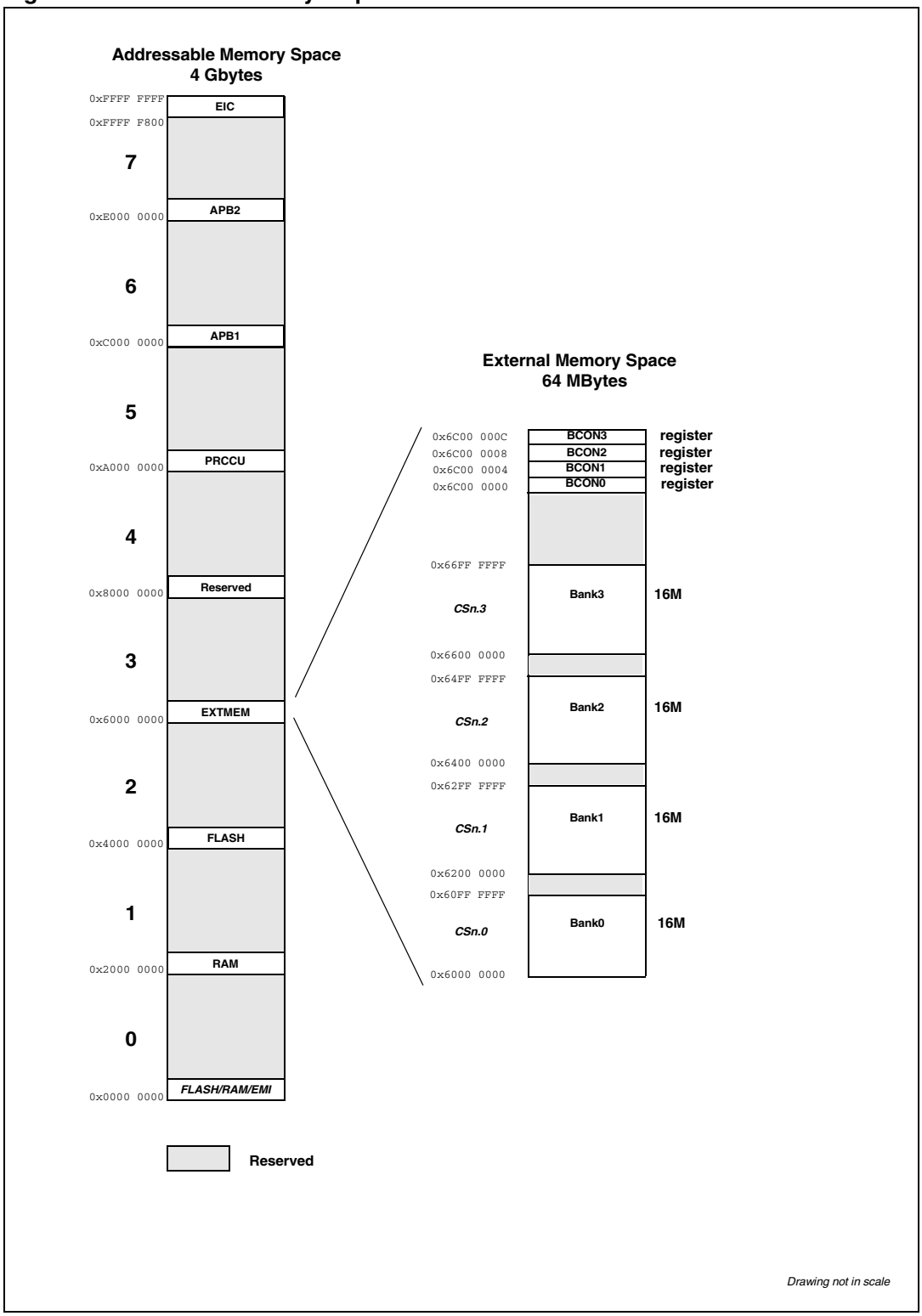


Table 14. Typical power consumption data

Symbol	Parameter		Conditions	Typical current on V33	Unit
I_{DDRUN}	RUN mode current from RAM	All periphs ON	MCLK = 16 MHz, PCLK1 = PCLK2 = 16 MHz	23	mA
			MCLK = 32 MHz, PCLK1 = PCLK2 = 32 MHz	40	
			MCLK = 48 MHz, PCLK1 = PCLK2 = 24 MHz	50	
			MCLK = 64 MHz, PCLK1 = PCLK2 = 32 MHz	63	
		All periphs OFF	MCLK = 16 MHz	16	
			MCLK = 32 MHz	26	
			MCLK = 48 MHz	39	
			MCLK = 64 MHz	48	
	RUN mode current from FLASH	All periphs ON	MCLK = 16 MHz, PCLK1 = PCLK2 = 16 MHz	27	
			MCLK = 32 MHz, PCLK1 = PCLK2 = 32 MHz	47	
			MCLK = 48 MHz, PCLK1 = PCLK2 = 24 MHz	62	
		All periphs OFF	MCLK = 16 MHz	21	
			MCLK = 32 MHz	36	
			MCLK = 48 MHz	53	
I_{DDSLOW}	SLOW mode current		MCLK = CK_AF (32 kHz), MVR off	1.7	
I_{DDWAIT}	WAIT mode current (all periphs ON)		PCLK1 = PCLK2 = 1 MHz	13	
$I_{DDLPWAIT}$	LPWAIT mode current		CK_AF (32 kHz), Main VReg off, FLASH in power-down	37	µA
I_{DDSTOP}	STOP mode current		Main VReg off, FLASH in power down, RTC on	18	
			Main VReg off, FLASH in power down, RTC off	10	
I_{DDSB}	STANDBY mode current		LP VReg on, LVD on, RTC on	10	
			LP VReg off (ext 1.8V on V18BKP), LVD on, RTC on	9	
			LP VReg off (ext1.8V on V18BKP), LVD off, RTC on	5	
			LP VReg off (ext 1.8V on V18BKP), LVD off, RTC off	1	

On-chip peripherals

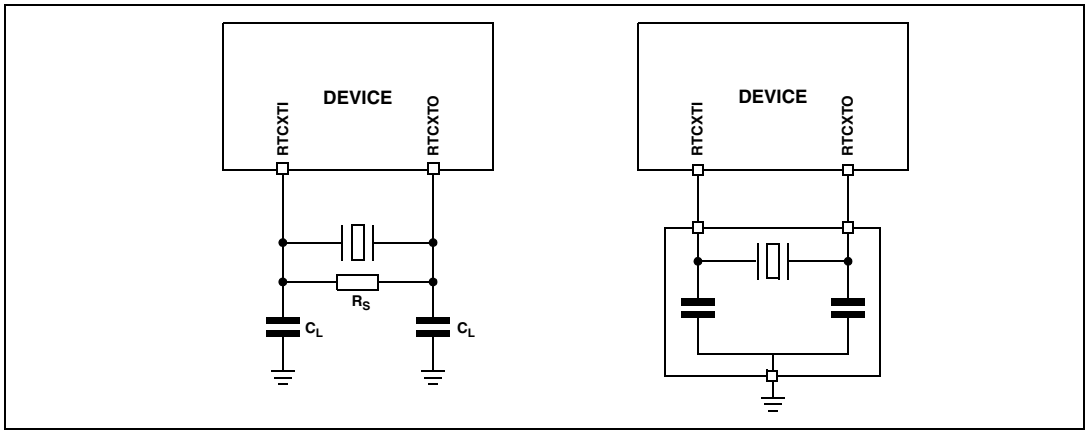
Table 15. Peripheral current consumption

Symbol	Parameter	Conditions	Typ	Unit
$I_{DD(PLL1)}$	PLL1 supply current	T_A= 25°C	3.42	mA
$I_{DD(PLL2)}$	PLL2 supply current		5.81	
$I_{DD(TIM)}$	TIM Timer supply current [1]	T_A= 25°C, f_{PCLK1}= f_{PCLK2}=33 MHz	0.88	
$I_{DD(BSPI)}$	BSPI supply current [2]		1.1	
$I_{DD(UART)}$	UART supply current [2]		1.05	
$I_{DD(I2C)}$	I2C supply current [2]		0.45	
$I_{DD(ADC)}$	ADC supply current when converting [5]		1.89	
$I_{DD(HDLC)}$	HDLC supply current [2]		1.82	
$I_{DD(USB)}$	USB supply current [2]		2.08	
$I_{DD(CAN)}$	CAN supply current [2]		1.11	

Notes:

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16MHz. No IC/OC programmed (no I/O pads toggling).
2. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

Figure 16. RTC crystal oscillator and resonator



PLL electrical characteristics

V_{33} = 3.0 to 3.6V, $V_{33IOPLL}$ = 3.0 to 3.6V, T_A = -40 / 85 °C unless otherwise specified.

Table 19. PLL1 characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
$f_{PLLCLK1}$	PLL multiplier output clock				165	MHz
f_{PLL1}	PLL input clock	FREF_RANGE = 0	1.5		3.0	MHz
		FREF_RANGE = 1 MX[1:0]='00' or '01'	3.0		8.25	MHz
		FREF_RANGE = 1 MX[1:0]='10' or '11'	3.0		6	MHz
	PLL input clock duty cycle		25		75	%
f_{FREE1}	PLL free running frequency	FREF_RANGE = 0 MX[1:0]='01' or '11'		125		kHz
		FREF_RANGE = 0 MX[1:0]='00' or '10'		250		kHz
		FREF_RANGE = 1 MX[1:0]='01' or '11'		250		kHz
		FREF_RANGE = 1 MX[1:0]='00' or '10'		500		kHz
t_{LOCK1}	PLL lock time	FREF_RANGE = 0 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			300	µs
		FREF_RANGE = 1 Stable Input Clock Stable $V_{33IOPLL}$, V_{18}			600	µs

Table 32. EMI read operation

Symbol	Parameter	Test Conditions	Value			Unit
			Min[1)]	Typ	Max[1)]	
t_{RCR}	Read to CSn Removal Time	MCLK=50 MHz 4 wait states 50 pf load on all pins	19	t_{MCLK}	21	ns
t_{RP}	Read Pulse Time		98	t_C	100	ns
t_{RDS}	Read Data Setup Time		22			ns
t_{RDH}	Read Data Hold Time		0			ns
t_{RAS}	Read Address Setup Time		27	$1.5*t_{MCLK}$	33	ns
t_{RAH}	Read Address Hold Time		0.65		2	ns
t_{RAT}	Read Address Turnaround Time		1.9		3.25	ns
t_{RRT}	RDn Turnaround Time		20	t_{MCLK}	21	ns

See *Figure 25*, *Figure 26*, *Figure 27* and *Figure 28* for related timing diagrams.

1. Data based on characterisation results, not tested in production.

Table 33. EMI write operation

Symbol	Parameter	Test conditions	Value			Unit
			Min[1)]	Typ	Max[1)]	
t_{WCR}	WEn to CSn Removal Time	MCLK=50 MHz 3 wait states 50 pf load on all pins	20	t_{MCLK}	22.5	ns
t_{WP}	Write Pulse Time		77.5	t_C	80	ns
t_{WDS1}	Write Data Setup Time 1		97	$t_C + t_{MCLK}$	100	ns
t_{WDS2}	Write Data Setup Time 2		77	t_C	80	ns
t_{WDH}	Write Data Hold Time		20	t_{MCLK}	23	ns
t_{WAS}	Write Address Setup Time		27	$1.5*t_{MCLK}$	33	ns
t_{WAH}	Write Address Hold Time		0.6		3	ns
t_{WAT}	Write Address Turnaround Time		1.75		4.1	ns
t_{WWT}	WEn Turnaround Time		20	t_{MCLK}	23	ns

See *Figure 29*, *Figure 30*, *Figure 31* and *Figure 32* for related timing diagrams.

1. Data based on characterisation results, not tested in production.

Figure 33. Typical application with I²C bus and timing diagram

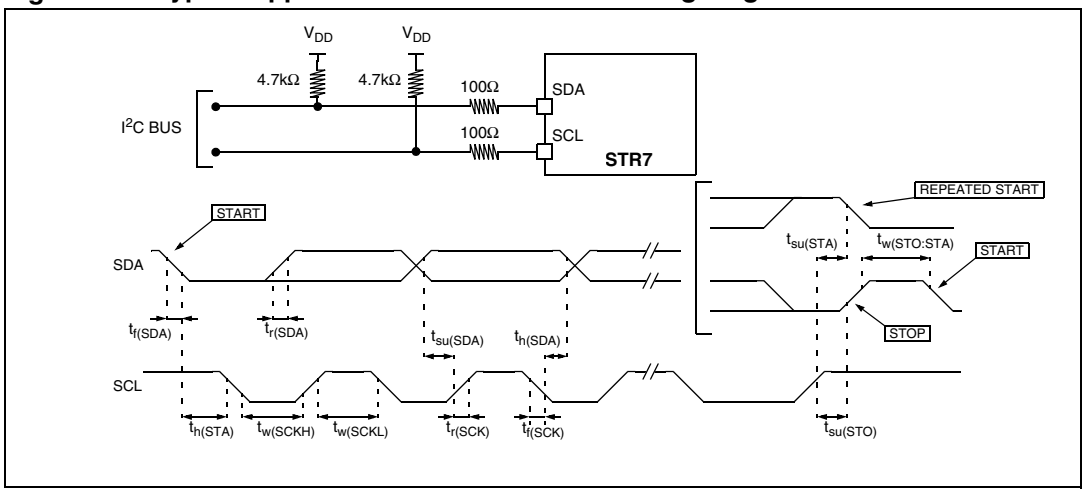


Table 35. SCL Frequency Table (f_{PCLK1}=8 MHz.,V_{33} = 3.3 V)

f_{SCL} (kHz)	I2CCCR Value
	R_P=4.7kΩ
400	83
300	85h
200	8Ah
100	24h
50	4Ch
20	C4h

Legend:

R_P = External pull-up resistance

f_{SCL} = I²C speed

NA = Not achievable

Note: For speeds around 200 kHz, achieved speed can have ± 5% tolerance

For other speed ranges, achieved speed can have ± 2% tolerance

The above variations depend on the accuracy of the external components used.

4.3.11 ADC characteristics

Subject to general operating conditions for AV_{DD}, f_{PCLK2}, and T_A unless otherwise specified.

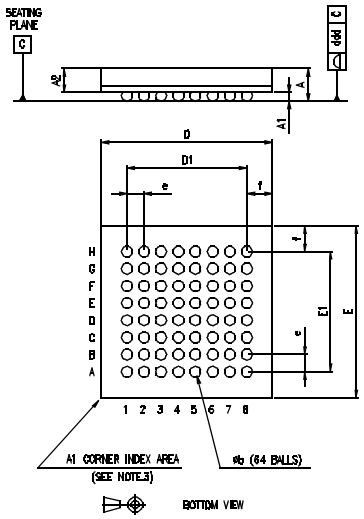
Table 40. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
f_{MOD}	Modulator Oversampling frequency				2.1	MHz
V_{AIN}	Conversion voltage range [2][3]		0		2.5	V
I_{lkg}	Negative input leakage current on analog pins	$V_{IN}<V_{SS}$, $\lvert I_{IN} \rvert <$ 400µA on adjacent analog pin		5	6	µA
PBR	Passband Ripple				0.1	dB
SINAD	S/N and Distortion		56	63		dB
THD	Total Harmonic Distortion		60	74		dB
Z_{IN}	Input Impedance	f_{MOD} = 2 MHz	1			MΩ
C_{ADC}	Internal sample and hold capacitor				3.2	pF
t_{CONV}	Total Conversion time (including sampling time)		2048/ f_{MOD} (max)			
I_{ADC}	Normal mode	T_A = 27 °C		2.5	3.0	mA
	Standby mode	T_A = 27 °C			1	µA

Notes:

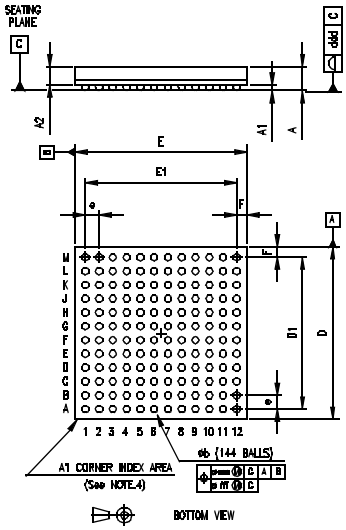
1. Unless otherwise specified, typical data are based on T_A=25°C and AV_{DD}-AV_{SS}=3.3V. They are given only as design guidelines and are not tested.
2. Any added external serial resistor will downgrade the ADC accuracy (especially for resistance greater than 10kΩ). Data based on characterization results, not tested in production.
3. Calibration is needed once after each power-up.

Figure 42. 64-Low profile fine pitch ball grid array package



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	1.210		1.700	0.048		0.067
A1	0.270			0.011		
A2		1.120			0.044	
b	0.450	0.500	0.550	0.018	0.020	0.022
D	7.750	8.000	8.150	0.305	0.315	0.321
D1		5.600			0.220	
E	7.750	8.000	8.150	0.305	0.315	0.321
E1		5.600			0.220	
e	0.720	0.800	0.880	0.028	0.031	0.035
f	1.050	1.200	1.350	0.041	0.047	0.053
ddd			0.120			0.005
	Number of Pins					
N	64					

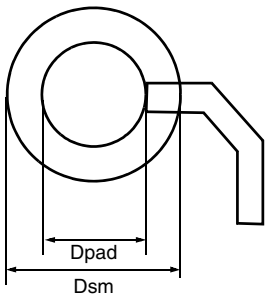
Figure 43. 144-low profile fine pitch ball grid array package



Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	1.21		1.70	0.0476		0.0669
A1	0.21			0.0083		
A2		1.085			0.0427	
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
D	9.85	10.00	10.15	0.3878	0.3937	0.3996
D1		8.80			0.3465	
E	9.85	10.00	10.15	0.3878	0.3937	0.3996
E1		8.80			0.3465	
e		0.80			0.0315	
F		0.60			0.0236	
ddd			0.10			0.0039
eee			0.15			0.0059
fff			0.08			0.0031
	Number of Pins					
N	144					

[1]Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. Recommended PCB design rules (0.80/0.75mm pitch BGA)



Dpad	0.37 mm
Dsm	0.52 mm typ. (depends on solder mask registration tolerance
Solder paste	0.37 mm aperture diameter
– Non solder mask defined pads are recommended – 4 to 6 mils screen print	

8 Known limitations

Description

If an IRQ or FIQ interrupt is pending and the Interrupt vector register (EIC_IVR) is not yet read, the HALT bit in the RCCU_SMR register can not be written. Therefore a software reset can not be generated.

Workaround

To generate a software reset when an IRQ or FIQ line is pending, either:

- reset the EIC peripheral by setting bit 14 in the APB2_SWRES register, or
- read the EIC_IVR register prior to generating a software reset.