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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM7® |
| Core Size | 32-Bit Single-Core |
| Speed | 66MHz |
| Connectivity | I²C, HDLC, SmartCard, SPI, UART/USART |
| Peripherals | PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | 64KB (64K x 8 + 16K) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 4x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/str715fr0t6 |

# 2 Description

### ARM® core with embedded Flash and RAM

The STR71x series is a family of ARM-powered 32-bit microcontrollers with embedded Flash and RAM. It combines the high performance ARM7TDMI CPU with an extensive range of peripheral functions and enhanced I/O capabilities. STR71xF devices have on-chip high-speed single voltage FLASH memory and high-speed RAM. STR710R devices have high-speed RAM but no internal Flash. The STR71x family has an embedded ARM core and is therefore compatible with all ARM tools and software.

### Extensive tools support

STMicroelectronics' 32-bit, ARM core-based microcontrollers are supported by a complete range of high-end and low-cost development tools to meet the needs of application developers. This extensive line of hardware/software tools includes starter kits and complete development packages all tailored for ST's ARM core-based MCUs. The range of development packages includes third-party solutions that come complete with a graphical development environment and an in-circuit emulator/programmer featuring a JTAG application interface. These support a range of embedded operating systems (OS), while several royalty-free OSs are also available.

For more information, please refer to ST MCU site http://www.st.com/mcu

**Table 3. STR710 BGA ball connections**

| | A | B | C | D | E | F | G | H | J | K | L | M |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **1** | P0.10 | P2.0 | P2.1 | VSS | P2.2 | P2.6 | BOOT EN | P2.12 | P2.13 | P2.15 | JTDI | N.C. |
| **2** | VSS | RDn | P0.11 | V33 | P2.3 | P2.8 | P2.9 | JTMS | JTRSTn | TEST | TEST | N.C. |
| **3** | V33 | P0.9 | P0.12 | P0.13 | P2.4 | N.C. | P2.10 | JTCK | NU | V33 | N.C. | DBG RQS |
| **4** | P0.6 | P0.7 | P0.8 | P0.14 | P2.5 | N.C. | P2.11 | JTDO | CK | CKOUT | VSSIO-PLL | N.C. |
| **5** | A.19 | WEn.1 | WEn.0 | P0.5 | P2.7 | VSS | P2.14 | N.C. | RTCX-TO | RTCXTI | N.C. | P0.15 |
| **6** | P0.3 | A.15 | A.16 | A.17 | A.18 | V33 | V18 | N.C. | N.C. | V18BKP | VSS BKP | $\overline{\text{STDBY}}$ |
| **7** | P0.2 | P0.1 | P0.4 | VSS18 | V18 | A.14 | D.12 | D.1 | D.0 | nc | VSS18 | $\overline{\text{RSTIN}}$ |
| **8** | A.9 | A.10 | A.11 | A.13 | P0.0 | A.0 | D.11 | P1.12/ CANTX | N.C. | AVSS | D.3 | D.2 |
| **9** | VSS | V33 | A.5 | A.6 | V33 | D.15 | D.10 | P1.8 | D.9 | P1.0 | N.C. | N.C. |
| **10** | A.8 | N.C. | P1.15 | P1.13 | VSS | D.14 | USBDN | P1.7 | D.8 | P1.5 | P1.1 | D.4 |
| **11** | A.7 | N.C. | P1.14 | P1.10 | A.2 | D.13 | USBDP | VSS | D.5 | P1.4 | P1.3 | AVDD |
| **12** | A.12 | A.4 | A.3 | P1.9 | A.1 | P1.11/ CANRX | N.C. | V33IO-PLL | P1.6 | D.7 | D.6 | P1.2 |

**Legend / abbreviations for** *Table 4*:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: C = CMOS $0.3V_{DD}/0.7V_{DD}$
$C_T$= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger
$T_T$= TTL 0.8 V/2 V with input trigger
C/T = Programmable levels: CMOS $0.3V_{DD}/0.7V_{DD}$ or TTL 0.8 V / 2 V

Port and control configuration:

Input: pu/pd= software enabled internal pull-up or pull down
pu= in reset state, the internal 100kΩ weak pull-up is enabled.
pd = in reset state, the internal 100kΩ weak pull-down is enabled.

Output: OD = open drain (logic level)
PP = push-pull
T = true OD, (P-Buffer and protection diode to $V_{DD}$ not implemented), 5 V tolerant.

**Table 4. STR710 pin description**

| Pin n° | | Pin name | Type | Reset state[1] | Input | | Output | | | Active in Stdby | Main function (after reset) | Alternate function | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP144 | BGA144 | | | | Input level | interrupt | Capability | OD | PP | | | | |
| 1 | A1 | P0.10/U1.RX/ U1.TX/ SC.DATA | I/O | pd | $C_T$ | X | 4mA | T | | | Port 0.10 | UART1: Receive Data input | UART1: Transmit data output. |
| | | | | | | | | | | | | **Note:** This pin may be used for Smartcard DataIn/DataOut or single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress | |
| 2 | B2 | $\overline{RD}$ | O | 5) | | | | | X | | External Memory Interface: Active low read signal for external memory. It maps to the OE_N input of the external components. | | |
| 3 | C2 | P0.11/BOOT.1 /U1.TX | I/O | pd | $C_T$ | | 4mA | X | X | | Port 0.11 | Select Boot Configuration input | UART1: Transmit data output. |
| 4 | C3 | P0.12/SC.CLK | I/O | pd | $C_T$ | | 4mA | X | X | | Port 0.12 | Smartcard reference clock output | |
| 5 | D1 | $V_{SS}$ | S | | | | | | | | Ground voltage for digital I/Os[4] | | |
| 6 | D2 | $V_{33}$ | S | | | | | | | | Supply voltage for digital I/Os[4] | | |
| 7 | B1 | P2.0/$\overline{CS}$.0 | I/O | 8) | $C_T$ | | 8mA | X | X | | Port 2.0 | External Memory Interface: Select Memory Bank 0 output<br>**Note:** This pin is forced to output push-pull 1 mode at reset to allow boot from external memory | |
| 8 | C1 | P2.1/$\overline{CS}$.1 | I/O | pu 2) | $C_T$ | | 8mA | X | X | | Port 2.1 | External Memory Interface: Select Memory Bank 1 output | |
| 9 | D3 | P0.13/U2.RX/ T2.OCMPA | I/O | pu | $C_T$ | X | 4mA | X | X | | Port 0.13 | UART2: Receive Data input | Timer2: Output Compare A output |
| 10 | D4 | P0.14/U2.TX/ T2.ICAPA | I/O | pu | $C_T$ | | 4mA | X | X | | Port 0.14 | UART2: Transmit data output | Timer2: Input Capture A input |
| 11 | E1 | P2.2/$\overline{CS}$.2 | I/O | pu 2) | $C_T$ | | 8mA | X | X | | Port 2.2 | External Memory Interface: Select Memory Bank 2 output | |
| 12 | E2 | P2.3/$\overline{CS}$.3 | I/O | pu 2) | $C_T$ | | 8mA | X | X | | Port 2.3 | External Memory Interface: Select Memory Bank 3 output | |

**Table 5. STR711/STR712/STR715 pin description**

| Pin n° | Pin name | Type | Reset state[1] | Input | | Output | | | Active in Stdby | Main function (after reset) | Alternate function | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | | | | Input level | interrupt | Capability | OD | PP | | | | |
| 1 | P0.10/U1.RX/ U1.TX/ SC.DATA | I/O | pd | $C_T$ | X | 4mA | T | | | Port 0.10 | UART1: Receive Data input | UART1: Transmit data output. |
| | | | | | | | | | | | **Note:** This pin may be used for Smartcard DataIn/DataOut or single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress | |
| 2 | P0.11/BOOT.1 /U1.TX | I/O | pd | $C_T$ | | 4mA | X | X | | Port 0.11 | Select Boot Configuration input | UART1: Transmit data output. |
| 3 | P0.12/SC.CLK | I/O | pd | $C_T$ | | 4mA | X | X | | Port 0.12 | Smartcard reference clock output | |
| 4 | $V_{SS}$ | S | | | | | | | | Ground voltage for digital I/Os[2] | | |
| 5 | P0.13/U2.RX/ T2.OCMPA | I/O | pu | $C_T$ | X | 4mA | X | X | | Port 0.13 | UART2: Receive Data input | Timer2: Output Compare A output |
| 6 | P0.14/U2.TX/ T2.ICAPA | I/O | pu | $C_T$ | | 4mA | X | X | | Port 0.14 | UART2: Transmit data output | Timer2: Input Capture A input |
| 7 | BOOTEN | I | | $C_T$ | | | | | | Boot control input. Enables sampling of BOOT[1:0] pins | | |
| 8 | $V_{SS}$ | S | | | | | | | | Ground voltage for digital I/Os[2] | | |
| 9 | $V_{33}$ | S | | | | | | | | Supply voltage for digital I/Os[2] | | |
| 10 | JTDI | I | | $T_T$ | | | | | | JTAG Data input. External pull-up required. | | |
| 11 | JTMS | I | | $T_T$ | | | | | | JTAG Mode Selection Input. External pull-up required. | | |
| 12 | JTCK | I | | C | | | | | | JTAG Clock Input. External pull-up or pull-down required. | | |
| 13 | JTDO | O | | | | 8mA | | X | | JTAG Data output. **Note:** Reset state = HiZ. | | |
| 14 | JTRST | I | | $T_T$ | | | | | | JTAG Reset Input. External pull-up required. | | |
| 15 | NU | | | | | | | | | Reserved, must be forced to ground. | | |
| 16 | TEST | | | | | | | | | Reserved, must be forced to ground. | | |
| 17 | $V_{33IO-PLL}$ | S | | | | | | | | Supply voltage for digital I/O circuitry and for PLL reference[2] | | |
| 18 | $V_{SSIO-PLL}$ | S | | | | | | | | Ground voltage for digital I/O circuitry and for PLL reference[2] | | |
| 19 | CK | I | | C | | | | | | Reference clock input | | |

**Table 5. STR711/STR712/STR715 pin description (continued)**

| Pin n° | Pin name | Type | Reset state[1] | Input | | Output | | | Active in Stdby | Main function (after reset) | Alternate function | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | | | | Input level | interrupt | Capability | OD | PP | | | | |
| 36 | P1.5/T1.ICAPB | I/O | pu | $C_T$ | | 4mA | X | X | | Port 1.5 | Timer 1: Input Capture B | |
| 37 | P1.6/T1.OCMPB | I/O | pu | $C_T$ | | 4mA | X | X | | Port 1.6 | Timer 1: Output Compare B | |
| 38 | $V_{33IO-PLL}$ | S | | | | | | | | Supply voltage for digital I/O circuitry and for PLL reference[2] | | |
| 39 | $V_{SSIO-PLL}$ | S | | | | | | | | Ground voltage for digital I/O circuitry and for PLL reference[2] | | |
| 40 | P1.7/T1.OCMPA | I/O | pu | $C_T$ | | 4mA | X | X | | Port 1.7 | Timer 1: Output Compare A | |
| 41 | P1.8 | I/O | pd | $C_T$ | | 4mA | X | X | | Port 1.8 | | |
| 42 | P1.11/CANRX | I/O | pu | $C_T$ | X | 4mA | X | X | | Port 1.11 | CAN: receive data input **Note:** On STR710 and STR712 only | |
| 43 | P1.12/CANTX | I/O | pu | $C_T$ | | 4mA | X | X | | Port 1.12 | CAN: Transmit data output **Note:** On STR710 and STR712 only | |
| 42 | USBDP | I/O | | $C_T$ | | | | | | USB bidirectional data (data +). Reset state = HiZ **Note:** On STR710 and STR711 only This pin requires an external pull-up to $V_{33}$ to maintain a high level. | | |
| 43 | USBDN | I/O | | $C_T$ | | | | | | USB bidirectional data (data -). Reset state = HiZ **Note:** On STR710 and STR711 only. | | |
| 44 | $V_{SS}$ | S | | | | | | | | Ground voltage for digital I/O circuitry[2] | | |
| 45 | P1.9 | I/O | pd | $C_T$ | | 4mA | X | X | | Port 1.9 | | |
| 46 | P1.10/USBCLK | I/O | pd | C/T | | 4mA | X | X | | Port 1.10 | USB: 48 MHZ clock input | |
| 47 | P1.13/HCLK/I0.SCL | I/O | pd | $C_T$ | X | 4mA | X | X | | Port 1.13 | HDLC: reference clock input | I2C clock |
| 48 | P1.14/HRXD/I0.SDA | I/O | pu | $C_T$ | X | 4mA | X | X | | Port 1.14 | HDLC: Receive data input | I2C serial data |
| 49 | P1.15/HTXD | I/O | pu | $C_T$ | | 4mA | X | X | | Port 1.15 | HDLC: Transmit data output | |
| 50 | $V_{SS}$ | S | | | | | | | | Ground voltage for digital I/O circuitry[2] | | |
| 51 | $V_{33}$ | S | | | | | | | | Supply voltage for digital I/O circuitry[2] | | |

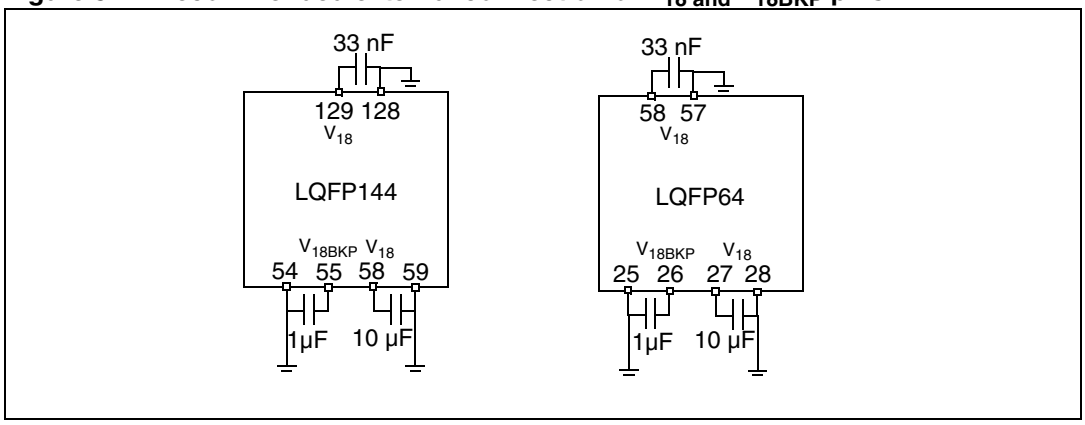
**Table 5. STR711/STR712/STR715 pin description (continued)**

| Pin n° LQFP64 | Pin name | Type | Reset state[1] | Input: Input level | Input: interrupt | Output: Capability | Output: OD | Output: PP | Active in Stdby | Main function (after reset) | Alternate function | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 63 | P0.8/U0.RX/U0.TX | I/O | pd | $C_T$ | X | 4mA | T | | | Port 0.8 | UART0: Receive Data input | UART0: Transmit data output. |
| | | | | | | | | | | **Note:** This pin may be used for single wire UART (half duplex) if programmed as Alternate Function Output. The pin will be tri-stated except when UART transmission is in progress | | |
| 64 | P0.9/U0.TX/BOOT.0 | I/O | pd | $C_T$ | | 4mA | X | X | | Port 0.9 | Select Boot Configuration input | UART0: Transmit data output |

1. The Reset configuration of the I/O Ports is IPUPD (input pull-up/pull down). Refer to *Table 6 on page 30*. The Port bit configuration at reset is PC0=1, PC1=1, PC2=0. The port data register bit (PD) value depends on the pu/pd column which specifies whether the pull-up or pull-down is enabled at reset
2. $V_{33IO\text{-}PLL}$ and $V_{33}$ are internally connected. $V_{SSIO\text{-}PLL}$ and $V_{SS}$ are internally connected.

## 3.5 External connections

**Figure 5. Recommended external connection of $V_{18}$ and $V_{18BKP}$ pins**



## 3.7 Memory mapping

**Figure 6. Memory map**

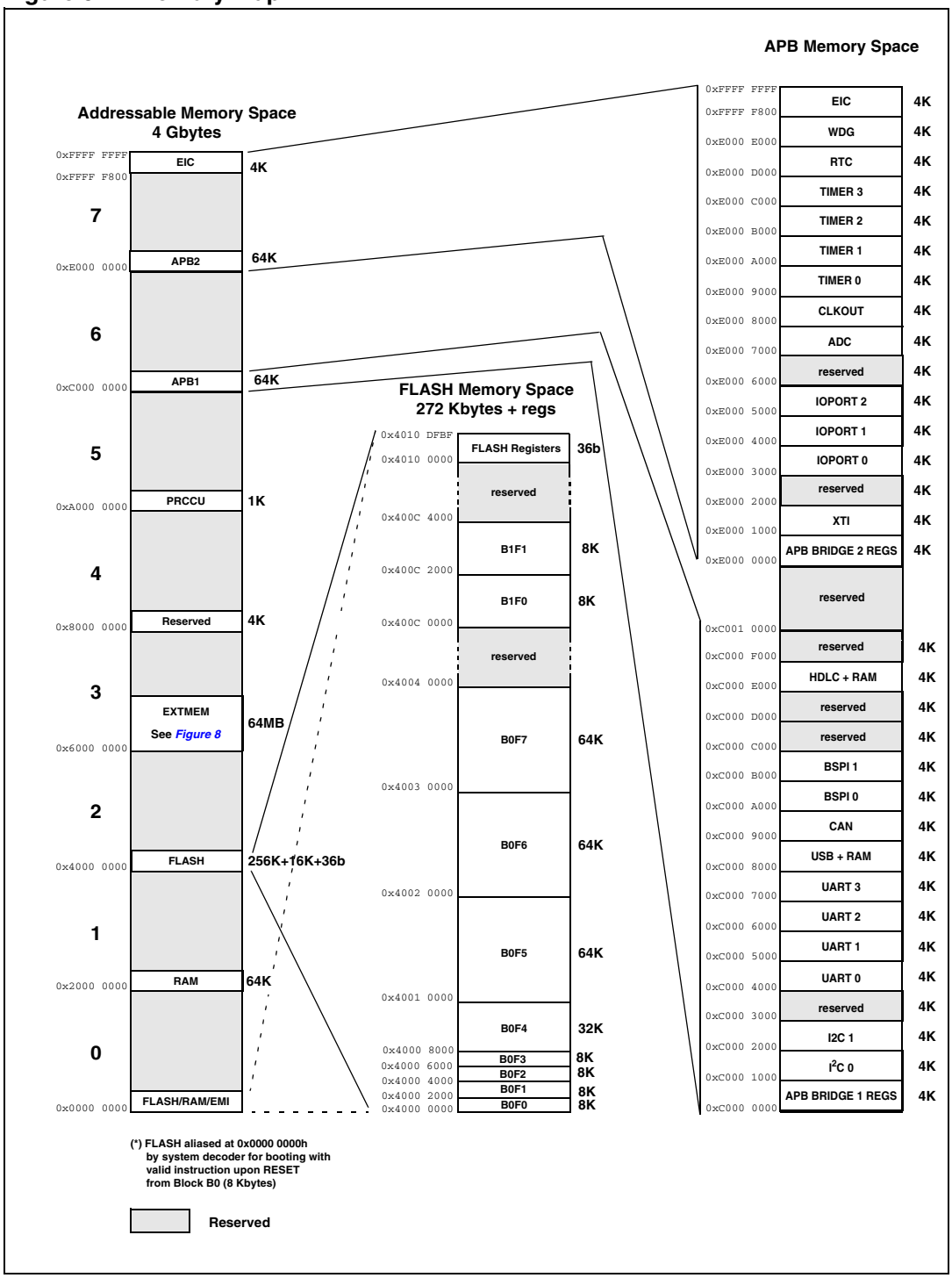


**Figure 8. External memory map**

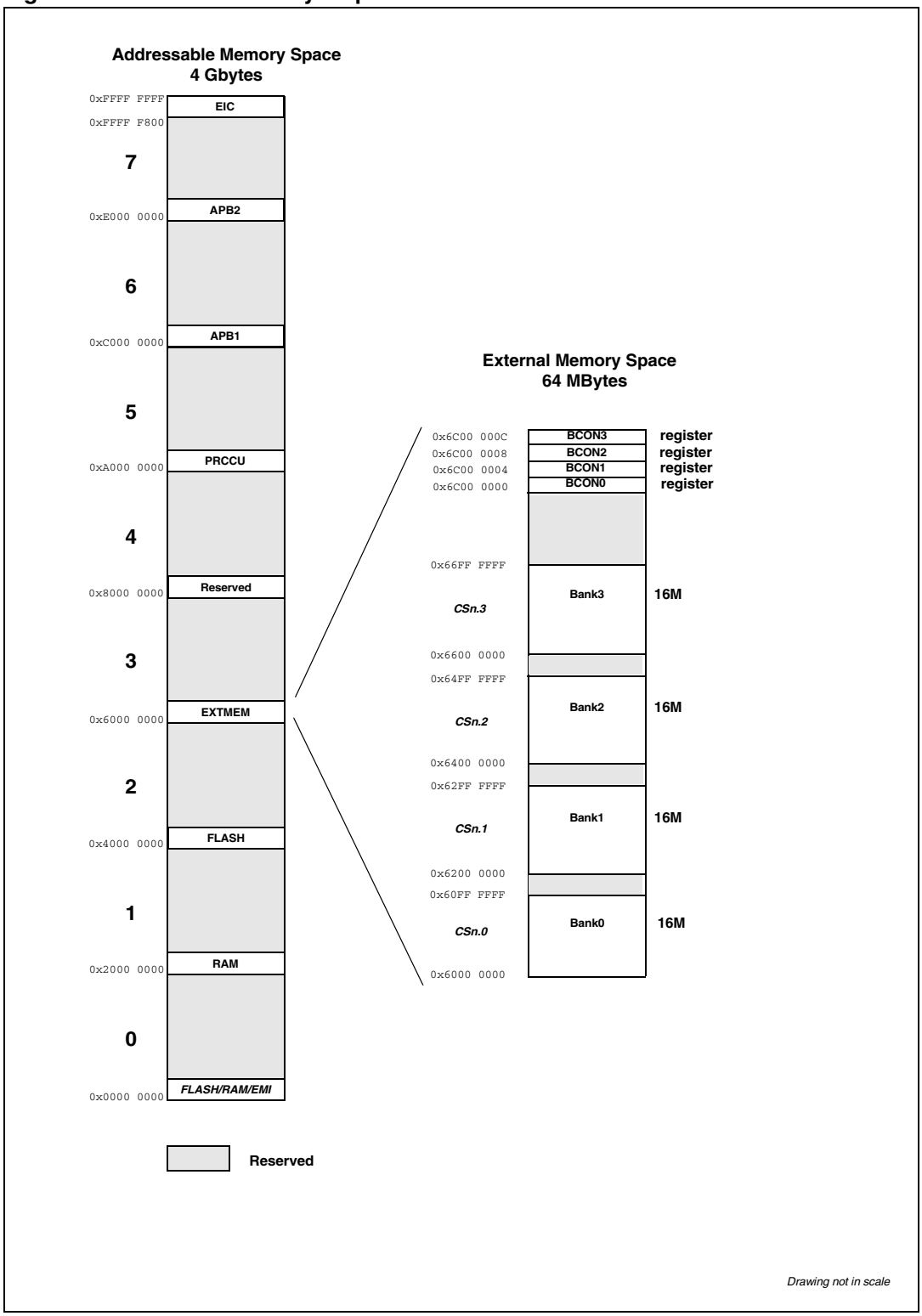


**Figure 11. STOP $I_{DD}$ vs. $V_{33}$**

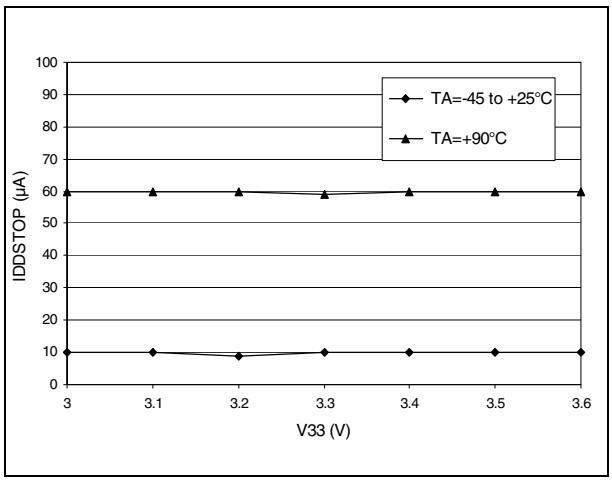



**Figure 12. STANDBY $I_{DD}$ vs. $V_{33}$**

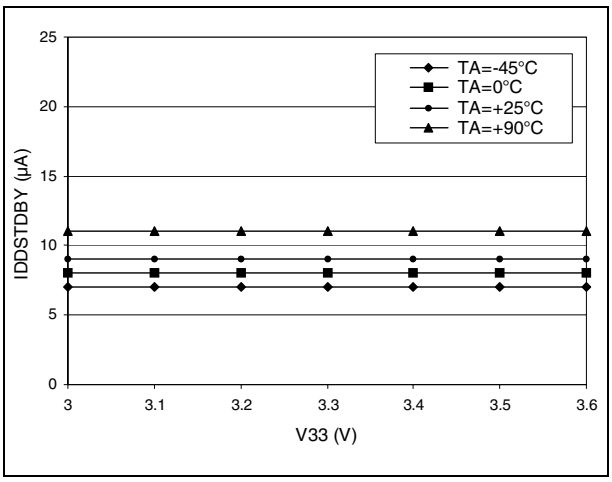



**Figure 13. WFI $I_{DD}$ vs. $V_{33}$**

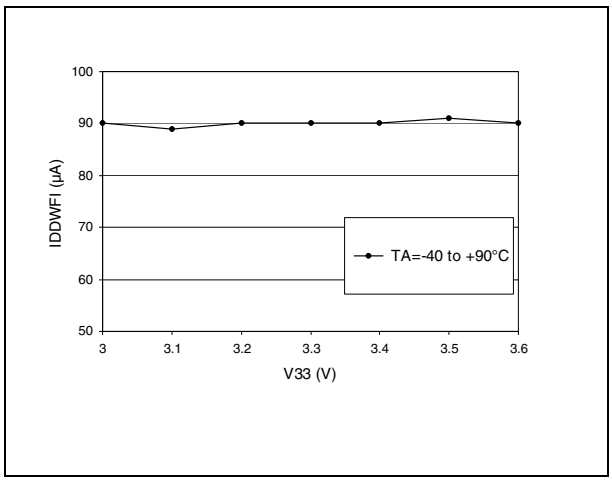


**Table 19. PLL1 characteristics (continued)**

| Symbol | Parameter | Test conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $\Delta t_{JITTER1}$ | PLL jitter (peak to peak) | $t_{PLL}$ = 4 MHz, MX[1:0]='11' Global Output division = 32 (Output Clock = 2 MHz) | | 0.7 | 2 | ns |

**Table 20. PLL2 characteristics**

| Symbol | Parameter | Test conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $f_{PLLCLK2}$ | PLL multiplier output clock | | | | 140 | MHz |
| $f_{PLL2}$ | PLL input clock | FREF_RANGE = 0 | 1.5 | | 3.0 | MHz |
| | | FREF_RANGE = 1 | 3.0 | | 5 | MHz |
| $t_{LOCK2}$ | PLL lock time | FREF_RANGE = 0 Stable Input Clock Stable $V_{33IOPLL}$, $V_{18}$ | | | 300 | µs |
| | | FREF_RANGE = 1 Stable Input Clock Stable $V_{33IOPLL}$, $V_{18}$ | | | 600 | µs |
| $\Delta t_{JITTER2}$ | PLL jitter (peak to peak) | $t_{PLL}$ = 4 MHz, MX[1:0]='11' Global Output division = 32 (Output Clock = 2 MHz) | | 0.7 | 2 | ns |

**Table 21. Low-power mode wakeup timing**

| Symbol | Parameter | Typ | Unit |
|---|---|---|---|
| $t_{WULPWFI}$ | Wakeup from LPWFI mode | 26(1) | µs |
| $t_{WUSTOP}$ | Wakeup from STOP mode | 2048 | CLK Cycles (2) |
| $t_{WUSTBY}$ | Wakeup from STANDBY mode | 2048 CLK Cycles + 8 CLK2 Cycles(3) | Cycles |

1. Clock selected is CK2_16, Main VReg OFF and Flash in power-down
2. The CLK clock is derived from the external oscillator.
3. Refer to Figure 7. Reset General Timing in the STR71xF Reference Manual (UM0084)

## 4.3.5 I/O port pin characteristics

### General characteristics

Subject to general operating conditions for $V_{33}$ and $T_A$ unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

**Table 27. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage 1) | CMOS ports | | | $0.3V_{33}$ | V |
| $V_{IH}$ | Input high level voltage 1) | | $0.7V_{33}$ | | | |
| $V_{hys}$ | Schmitt trigger voltage hysteresis 2) | | | 0.8 | | V |
| $V_{IL}$ | Input low level voltage 1) | P0.15 WAKEUP | | 0.9 | 0.8 | V |
| $V_{IH}$ | Input high level voltage 1) | | 2 | 1.35 | | |
| $V_{hys}$ | Schmitt trigger voltage hysteresis 2) | | | 0.4 | | V |
| $V_{IL}$ | Input low level voltage 1) | TTL ports | | | 0.8 | V |
| $V_{IH}$ | Input high level voltage 1) | | 2.0 | | | |
| $I_{INJ(PIN)}$ | Injected Current on any I/O pin | | | | ± 4 | mA |
| $\Sigma I_{INJ(PIN)}$ 3) | Total injected current (sum of all I/O and control pins) | | | | ± 25 | |
| $I_{lkg}$ | Input leakage current 4) | $V_{SS} \le V_{IN} \le V_{33}$ | | | ±1 | µA |
| $R_{PU}$ | Weak pull-up equivalent resistor5) | $V_{IN}=V_{SS}$ | 110 | 150 | 700 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor5) | $V_{IN}=V_{33}$ | 110 | 150 | 700 | kΩ |
| $C_{IO}$ | I/O pin capacitance | | | 5 | | pF |

**Notes**:

1. Data based on characterization results, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
3. When the current limitation is not possible, the $V_{IN}$ absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{33}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Refer to *Section 4.2 on page 35* for more details.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. The $R_{PU}$ pull-up and $R_{PD}$ pull-down equivalent resistor are based on a resistive transistor (corresponding $I_{PU}$ and $I_{PD}$ current characteristics described in *Figure 18* to *Figure 19*).

**Figure 22. Typical $V_{OL}$ vs. $V_{33}$**

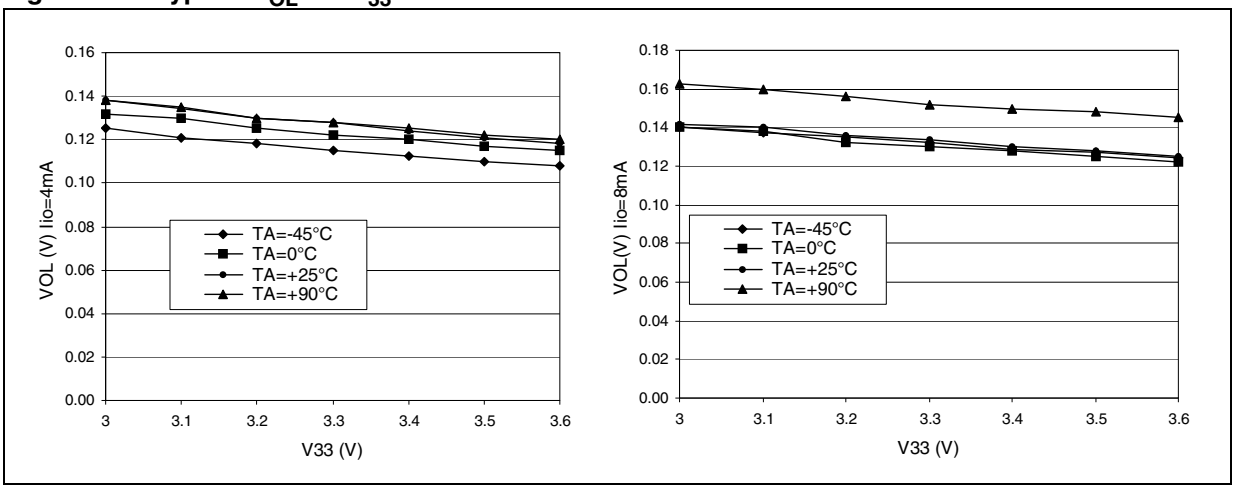
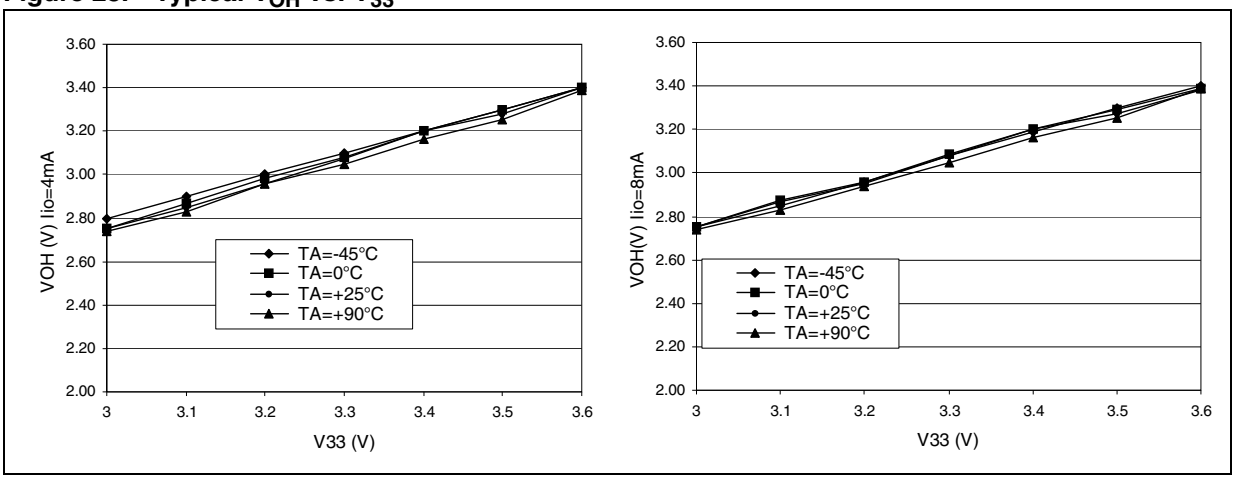



**Figure 23. Typical $V_{OH}$ vs. $V_{33}$**



### $\overline{\text{RSTIN}}$ pin

The $\overline{\text{RSTIN}}$ pin input driver is CMOS. A permanent pull-up is present which is the same as as $R_{PU}$ (see *Table 27 on page 51*)

Subject to general operating conditions for $V_{33}$ and $T_A$ unless otherwise specified.

**Table 29. $\overline{\text{RESET}}$ pin characteristics**

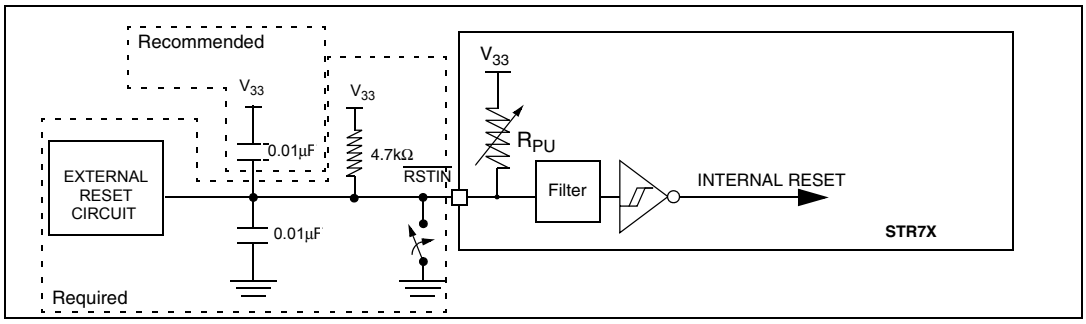
| Symbol | Parameter | Conditions | Min | Typ [1] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(RSTINn)}$ | $\overline{\text{RSTIN}}$ Input low level voltage [1] | | | | 0.8 | V |
| $V_{IH(RSTINn)}$ | $\overline{\text{RSTIN}}$ Input high level voltage [1] | | 2 | | | |
| $V_{F(RSTINn)}$ | $\overline{\text{RSTIN}}$ Input filtered pulse[2] | | | | 500 | ns |
| $V_{NF(RSTINn)}$ | $\overline{\text{RSTIN}}$ Input not filtered pulse[2] | | 1.2 | | | µs |

**Notes:**

1. Data based on characterization results, not tested in production.

2) Data guaranteed by design, not tested in production.

**Figure 24. Recommended $\overline{\text{RSTIN}}$ pin protection.[1]**




Notes:

1. The $R_{PU}$ pull-up equivalent resistor is based on a resistive transistor (corresponding $I_{PU}$ current characteristics described in *Figure 18*).
2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the $\overline{\text{RSTIN}}$ pin can go below the $V_{IL(RSTINn)}$ max. level specified in *Table 29*. Otherwise the reset will not be taken into account internally.

### 4.3.9 BSPI - buffered serial peripheral interface

Subject to general operating conditions for $V_{DD}$, $T_A$ and $f_{PCLK1}$ ,unless otherwise specified.

Refer to *I/O port pin characteristics on page 51* for more details on the input/output alternate function characteristics ($\overline{SS}$, SCK, MOSI, MISO).

**Table 36. BSPI characteristics**

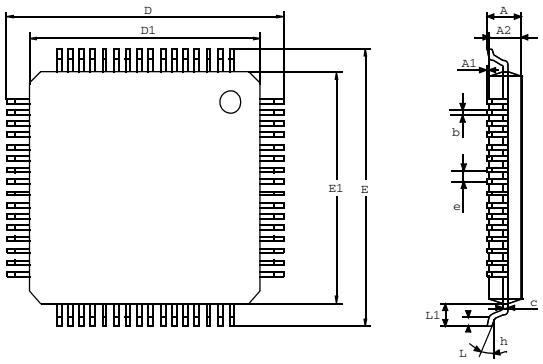
| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master | $f_{PCLK1}/254$ | $f_{PCLK1}/6$<br>5.5 | MHz |
| | | Slave | 0 | $f_{PCLK1}/8$<br>3.3 | |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$ | SPI clock rise and fall time | capacitive charge<br>C=50 pF | | 14 | ns |
| $t_{su(\overline{SS})}$ (1) | $\overline{SS}$ setup time | Slave | 0 | | |
| $t_{h(\overline{SS})}$ (1) | $\overline{SS}$ hold time | Slave | 0 | | |
| $t_{w(SCKH)}$ (1)<br>$t_{w(SCKL)}$ (1) | SCK high and low time | Master $f_{PCLK1}$=33 MHz,<br>presc = 6 | 73 | | |
| $t_{su(MI)}$ (1)<br>$t_{su(SI)}$ (1) | Data input setup time | Master<br>Slave | 7<br>0 | | |
| $t_{h(MI)}$ 1)(2)<br>$t_{h(SI)}$ 1)(2) | Data input hold time | Master<br>Slave | $1xt_{PCLK1}$<br>$2xt_{PCLK1}$ | | |
| $t_{h(MI)}$ (1)<br>$t_{h(SI)}$ (1) | Data input hold time | Master $f_{PCLK1}$=33 MHz<br>Slave $f_{PCLK1}$=33 MHz | 30<br>60 | | |
| $t_{a(SO)}$ 1)(3) | Data output access time | Slave | 0 | $1.5xt_{PCLK1}+42$ | |
| | | Slave $f_{PCLK1}$=33 MHz | 0 | 87 | |
| $t_{dis(SO)}$ (1)(4) | Data output disable time | Slave | 0 | 42 | |
| $t_{v(SO)}$ (1)(2) | Data output valid time | Slave (after enable edge) | | $3xt_{PCLK1}+45$ | |
| | | $f_{PCLK1}$=33 MHz | | 135 | |
| $t_{h(SO)}$ (1) | Data output hold time | Slave (after enable edge) | 0 | | |
| $t_{v(MO)}$ (1)(2) | Data output valid time | Master (after enable edge) | | $2xt_{PCLK1}+12$ | |
| | | $f_{PCLK1}$=33 MHz | | 72 | |
| $t_{h(MO)}$ (1) | Data output hold time | Master (after enable edge) | 0 | | |

1. Data based on design simulation and/or characterisation results, not tested in production.
2. Depends on $f_{PCLK1}$. For example, if $f_{PCLK1}$=8 MHz, then $t_{PCLK1}$ = $1/f_{PCLK1}$ =125 ns and $t_{v(MO)}$ = 255 ns.
3. Min. time is the minimum time to drive the output and the max. time is the maximum time to validate the data.
4. Min time is the minimun time to invalidate the output and the max time is the maximum time to put the data in Hi-Z.

# 5 Package characteristics

## 5.1 Package mechanical data

**Figure 40. 64-Pin low profile quad flat package (10x10)**




| Dim. | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.17 | 0.22 | 0.27 | 0.007 | 0.009 | 0.011 |
| c | 0.09 | | 0.20 | 0.004 | | 0.008 |
| D | | 12.00 | | | 0.472 | |
| D1 | | 10.00 | | | 0.394 | |
| E | | 12.00 | | | 0.472 | |
| E1 | | 10.00 | | | 0.394 | |
| e | | 0.50 | | | 0.020 | |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | | 1.00 | | | 0.039 | |
| | Number of Pins | | | | | |
| N | 64 | | | | | |

Recommended footprint (dimensions in mm)

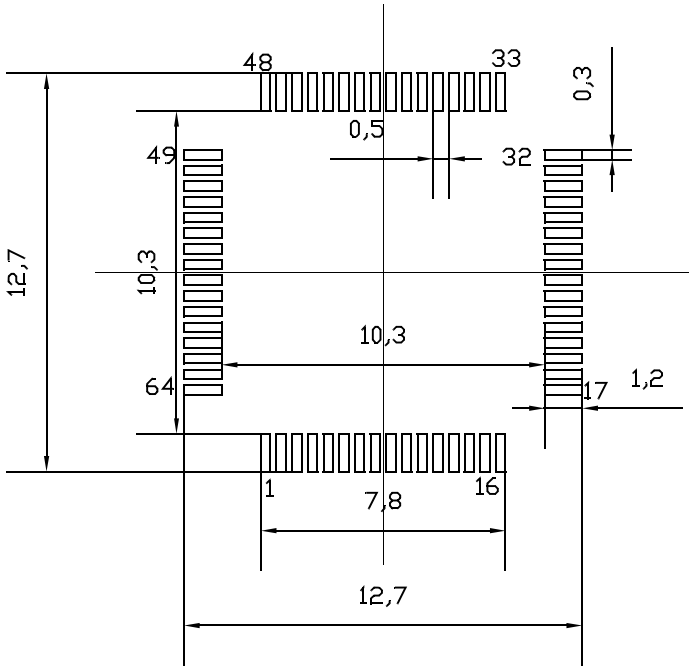
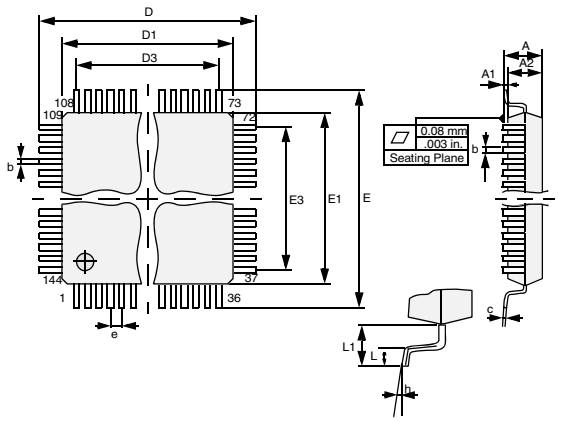


**Figure 41. 144-Pin low profile quad flat package**




| Dim. | mm | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | | 0.057 |
| b | 0.17 | 0.22 | 0.27 | 0.007 | | 0.011 |
| c | 0.09 | | 0.20 | 0.004 | | 0.008 |
| D | 21.80 | 22.00 | 22.20 | 0.858 | 0.867 | 0.874 |
| D1 | 19.80 | 20.00 | 20.20 | 0.780 | 0.787 | 0.795 |
| D3 | | 17.50 | | | 0.689 | |
| E | 21.80 | 22.00 | 22.20 | 0.858 | 0.867 | 0.874 |
| E1 | 19.80 | 20.00 | 20.20 | 0.780 | 0.787 | 0.795 |
| E3 | | 17.50 | | | 0.689 | |
| e | | 0.50 | | | 0.020 | |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | | 1.00 | | | 0.039 | |
| | Number of Pins | | | | | |
| N | 144 | | | | | |

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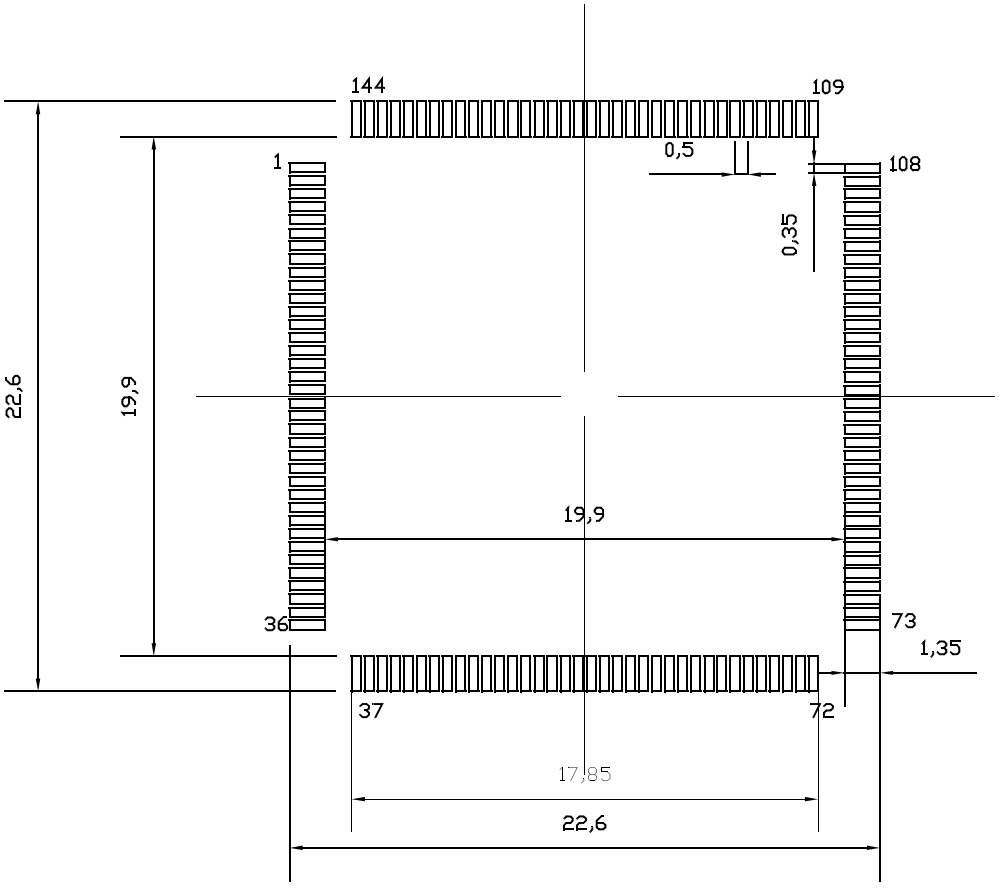
1.Values in inches are converted from mm and rounded to 3 decimal digits.

Recommended footprint (dimensions in mm)



# 6 Product history

There are three versions of the STR710F series products. All versions are functionally identical and differ only with the points listed below.

Version "A" was the first version produced and delivered. Version "Z" was the second in production replacing version "A". Version "Z" has lower power consumption in STOP mode.

Version "X" is the latest introduced.

**Marking**

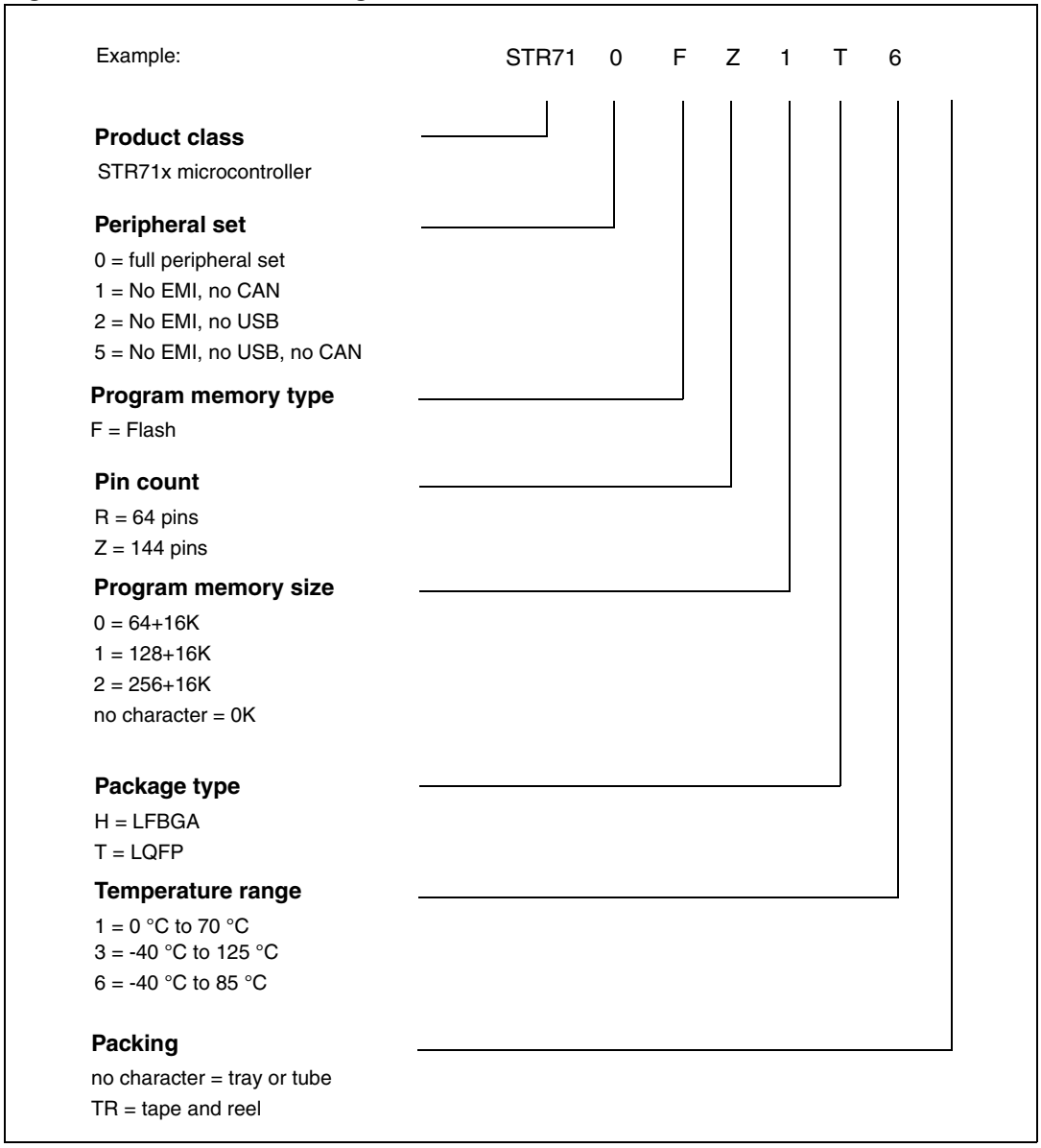
The difference between versions is visible on the marking of the product as shown in the four examples in *Figure 45* through *Figure 48*.

**Figure 45. LQFP144 STR710 version “A”**


**Figure 46. LQFP64 STR712 version “Z”**

# 7 Ordering information

**Figure 49. STR71xF ordering information scheme**




1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to www.st.com or contact the ST Sales Office nearest to you.

# 8 Known limitations

## Description

If an IRQ or FIQ interrupt is pending and the Interrupt vector register (EIC_IVR) is not yet read, the HALT bit in the RCCU_SMR register can not be written. Therefore a software reset can not be generated.

## Workaround

To generate a software reset when an IRQ or FIQ line is pending, either:

- reset the EIC peripheral by setting bit 14 in the APB2_SWRES register, or
- read the EIC_IVR register prior to generating a software reset.

# 9 Revision history

**Table 44. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 17-Mar-2004 | 1 | First Release |
| 05-Apr-2004 | 2 | Updated “Electrical parameters” on page 34 |
| 08-Apr-2004 | 2.1 | Corrected STR712F Pinout. Pins 43/42 swapped. |
| 15-Apr-2004 | 2.2 | PDF hyperlinks corrected. |
| 7-Jul-2004 | 3 | Corrected description of STDBY, V18, VSS18 V18BKP VSSBKP pins<br>Added IDDrun typical data<br>Updated BSPI max. baudrate.<br>Updated “EMI - external memory interface” on page 56 |
| 29-Oct-2004 | 4 | Corrected Flash sector B1F0/F1 address in *Figure 6: Memory map on page 31*<br>Corrected *Table 5 on page 25* LQFP64 TEST pin is 16 instead of 17. Added to TQPFP64 column: pin 7 BOOTEN, pin 17 $V_{33IO-PLL}$<br>Changed description of JTCK from ‘External pull-down required’ to ‘External pull-up or pull down required’. |
| 25-Jan-2005 | 5 | Changed “Product Preview” to “Preliminary Data” on page 1 and 3<br>Renamed ‘PU/PD’ column to ‘Reset state’ in *Table 5 on page 25*<br>Added reference to STR7 Flash Programming Reference Manual |
| 19-Apr-2005 | 6 | Added STR715F devices and modified RAM size of STR71xF1 devices<br>Added BGA package in *Section 5*<br>Updated ordering information in *Section 7*.<br>Added PLL duty cycle min and max. in *PLL electrical characteristics on page 45* |
| 13-Oct-2005 | 7 | Updated feature description on page 1<br>Update overview *Section 1.1*<br>Added OD/PP to P0.12 in *Table 5*<br>Changed name of WFI mode to WAIT mode<br>Changed Memory Map *Table 6*: Ext. Memory changed to 64 MB and flash register changed to 36 bytes.<br>Added Power Consumption *Table 13*<br>Modified BGA144 F3, F5, F12 and G12 in *Table 3* and *Table 4*<br>Update EMI Timing *Table 24* and *Figure 29* |