Renesas Electronics America Inc - UPD78F8040K8(R)-9B4-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	78K/0
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-WFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f8040k8-r-9b4-ax

5.4.7 Based addressing

[Function]

Based addressing uses the contents of a register pair specified with the instruction word as a base address, and 8-bit immediate data or 16-bit immediate data as offset data. The sum of these values is used to specify the target address.

[Operand format]

Identifier	Description
–	[HL + byte], [DE + byte], [SP + byte] (only the space from F0000H to FFFFFH is specifiable)
–	word[B], word[C] (only the space from F0000H to FFFFFH is specifiable)
–	word[BC] (only the space from F0000H to FFFFFH is specifiable)
–	ES:[HL + byte], ES:[DE + byte] (higher 4-bit addresses are specified by the ES register)
–	ES:word[B], ES:word[C] (higher 4-bit addresses are specified by the ES register)
–	ES:word[BC] (higher 4-bit addresses are specified by the ES register)

Figure 5-29. Example of [SP+byte]

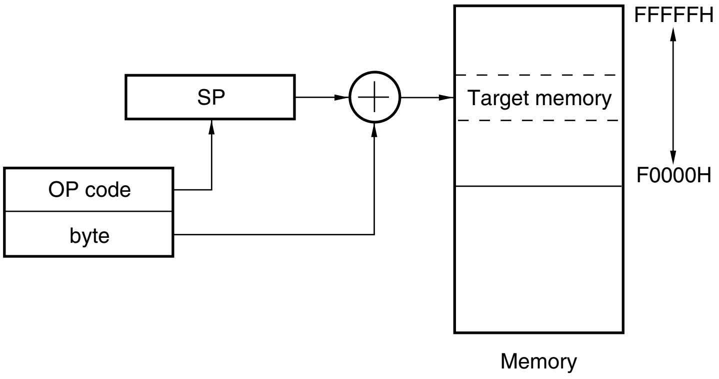


Table 6-2. Port Functions (2/2)

Function Name	I/O	Function	After Reset	Alternate Function
P142	I/O	Port 14. 3-bit I/O port. Input of P142 and P143 can be set to TTL input buffer. Output of P142 to P144 can be set to the N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{\text{SCK20}}$/SCL20
P143				SI20/RxD2/SDA20
P144				SO20/TxD2
P150 to P153	I/O	Port 15. 4-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI8 to ANI11

6.2 Port Configuration

Ports include the following hardware.

Table 6-3. Port Configuration

Item	Configuration
Control registers	Port mode registers (PM0 to PM7, PM11, PM12, PM14, PM15) Port registers (P0 to P7, P11, P12, P14, P15) Pull-up resistor option registers (PU0, PU1, PU3 to PU6, PU12, PU14) Port input mode register 14 (PIM14) Port output mode register 14 (POM14) A/D port configuration register (ADPC)
Port	Total: 26 (CMOS I/O: 23, CMOS input: 1, N-ch open drain I/O: 2)
Pull-up resistor	Total: 18

6.5 Settings of Port Mode Register, and Output Latch When Using Alternate Function

To use the alternate function of a port pin, set the port mode register, and output latch as shown in Table 6-6.

Table 6-6. Settings of Port Mode Register, and Output Latch When Using Alternate Function

Pin Name	Alternate Function		PM××	P××
	Function Name	I/O		
P05	TI05	Input	1	×
	TO05	Output	0	0
P11	RxD0	Input	1	×
P13	TxD3	Output	0	1
P14	RxD3	Input	1	×
P16	TI01	Input	1	×
	TO01	Output	0	0
	INTP5	Input	1	×
P17	TI02	Input	1	×
	TO02	Output	0	0
P26, P27[Note]	ANI6, ANI7[Note]	Input	1	×
P31	TI03	Input	1	×
	TO03	Output	0	0
	INTP4	Input	1	×
P40	TOOL0	I/O	×	×
P41	TOOL1	Output	×	×
P50	INTP1	Input	1	×
P51	INTP2	Input	1	×
P60	SCL0	I/O	0	0
P61	SDA0	I/O	0	0
P65	TI11	Input	1	×
	TO11	Output	0	0
P67	TI13	Input	1	×
	TO13	Output	0	0
P120	INTP0	Input	1	×
	EXLVI	Input	1	×
P142	$\overline{\text{SCK20}}$	Input	1	×
		Output	0	1
	SCL20	I/O	0	1
P143	SI20	Input	1	×
	RxD2	Input	1	×
	SDA20	I/O	0	1
P144	SO20	Output	0	1
	TxD2	Output	0	1
P150 to P153[Note]	ANI8 to ANI11[Note]	Input	1	×

Note The functions of the ANI6/P26, ANI7/P27, and ANI8/P150 to ANI11/P153 pins can be selected by using the A/D port configuration register (ADPC), the analog input channel specification register (ADS), and port mode registers 2, 15 (PM2, PM15).

Table 6-7. Setting Functions of ANI6/P26, ANI7/P27, and ANI8/P150 to ANI11/P153 Pins

ADPC	PM2, PM15	ADS	ANI6/P26, ANI7/P27, ANI8/P150 to ANI11/P153 Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

Remark ×: don’t care

PM××: Port mode register

P××: Port output latch

Remark

f_X:	X1 clock oscillation frequency
f_{IH}:	Internal high-speed oscillation clock frequency
f_{IH20}:	20 MHz internal high-speed oscillation clock frequency
f_{EX}:	External main system clock frequency
f_{MX}:	High-speed system clock frequency
f_{MAIN}:	Main system clock frequency
f_{CLK}:	CPU/peripheral hardware clock frequency
f_{IL}:	Internal low-speed oscillation clock frequency

7.3 Registers Controlling Clock Generator

The following eight registers are used to control the clock generator.

- Clock operation mode control register (CMC)
- Clock operation status control register (CSC)
- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)
- System clock control register (CKC)
- 20 MHz internal high-speed oscillation control register (DSCCTL)
- Peripheral enable register 0 (PER0)
- Operation speed mode control register (OSMC)

(1) Clock operation mode control register (CMC)

This register is used to set the operation mode of the X1/P121 and X2/EXCLK pins, and to select a gain of the oscillator.

CMC can be written only once by an 8-bit memory manipulation instruction after reset release. This register can be read by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-8. Format of Peripheral Enable Register 0 (PER0) (2/2)

Address: F00F0H After reset: 00H R/W

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>
PER0	0	0	ADCEN	IICAEN	SAU1EN	SAU0EN	TAU1EN	TAU0EN

TAU1EN	Control of timer array unit 1 input clock supply
0	Stops input clock supply. • SFR used by timer array unit 1 cannot be written. • Timer array unit 1 is in the reset status.
1	Supplies input clock. • SFR used by timer array unit 1 can be read and written.

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply. • SFR used by timer array unit 0 cannot be written. • Timer array unit 0 is in the reset status.
1	Supplies input clock. • SFR used by timer array unit 0 can be read and written.

Caution Be sure to clear bits 6 and 7 to 0.

Notes 1. The internal reset processing time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

2. When releasing a reset, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC).

3. The microcontroller operates on the 8 MHz internal high-speed oscillation clock if 8 MHz or 20 MHz is selected for the internal high-speed oscillator by using the option byte or on the 1 MHz internal high-speed oscillation clock if 1 MHz is selected.

4. If the internal high-speed oscillator is set to 1 MHz by using the option byte, the 20 MHz internal high-speed oscillation clock cannot be used.

Cautions 1. A voltage stabilization time (about 2.12 to 5.84 ms) is required after the supply voltage reaches 1.61 V (TYP.). If the time for the supply voltage to rise from 1.61 V (TYP.) to 2.07 V (TYP.) is shorter than the voltage stabilization time, reset processing is entered after the voltage stabilization time elapses.

2. It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK pin is used.

(1) Timer counter register mn (TCRmn)

The TCRmn register is a 16-bit read-only register and is used to count clocks.

The value of this counter is incremented or decremented in synchronization with the rising edge of a count clock.

Whether the counter is incremented or decremented depends on the operation mode that is selected by the MDmn3 to MDmn0 bits of timer mode register mn (TMRmn) (refer to **8.3 (3) Timer mode register mn (TMRmn)**).

Figure 8-4. Format of Timer Counter Register mn (TCRmn)

Address: F0180H, F0181H (TCR00) to F018EH, F018FH (TCR07) After reset: FFFFH R
F01C0H, F01C1H (TCR10) to F01C6H, F01C7H (TCR13)

	F0181H (TCR00)								F0180H (TCR00)							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCRmn																

The count value can be read by reading TCRmn.

The count value is set to FFFFH in the following cases.

- When the reset signal is generated
- When the TAU0EN bit (in case of TAU0) or TAU1EN bit (in case of TAU1) of peripheral enable register 0 (PER0) is cleared
- When counting of the slave channel has been completed in the PWM output mode
- When counting of the master/slave channel has been completed in the one-shot pulse output mode
- When counting of the slave channel has been completed in the multiple PWM output mode

The count value is cleared to 0000H in the following cases.

- When the start trigger is input in the capture mode
- When capturing has been completed in the capture mode

Caution The count value is not captured to timer data register mn (TDRmn) even when the TCRmn register is read.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7),
mn = 00 to 07, 10 to 13

The TCRmn register read value differs as follows according to operation mode changes and the operating status.

Table 8-2. Timer/counter Register mn (TCRmn) Read Value in Various Operation Modes

Operation Mode	Count Mode	Timer/counter register mn (TCRmn) Read Value[Note]			
		Value if the operation mode was changed after releasing reset	Value if the operation mode was changed after count operation paused (TTmn = 1)	Value if the Operation was restarted after count operation paused (TTmn = 1)	Value when waiting for a start trigger after one count
Interval timer mode	Count down	FFFFH	Undefined	Stop value	–
Capture mode	Count up	0000H	Undefined	Stop value	–
Event counter mode	Count down	FFFFH	Undefined	Stop value	–
One-count mode	Count down	FFFFH	Undefined	Stop value	FFFFH
Capture & one-count mode	Count up	0000H	Undefined	Stop value	Capture value of TDRmn register + 1

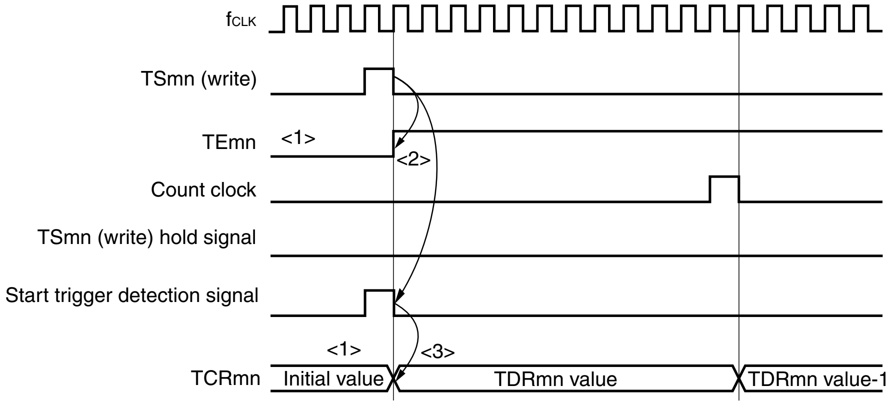
Note This indicates the value read from the TCRmn register when channel n has stopped operating as a timer (TEmn = 0) and has been enabled to operate as a counter (TSmn = 1). The read value is held in the TCRmn register until the count operation starts.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7), mn = 00 to 07, 10 to 13

(b) Start timing in event counter mode

<1> Timer/counter register mn (TCRmn) holds its initial value while operation is stopped (TEmn = 0).
<2> Operation is enabled (TEmn = 1) by writing 1 to the TSmn.
<3> As soon as 1 has been written to the TSmn bit and 1 has been set to the TEmn bit, the value of timer data register mn (TDRmn) is loaded to the TCRmn to start counting.
<4> After that, the TCRmn register value is counted down according to the count clock.

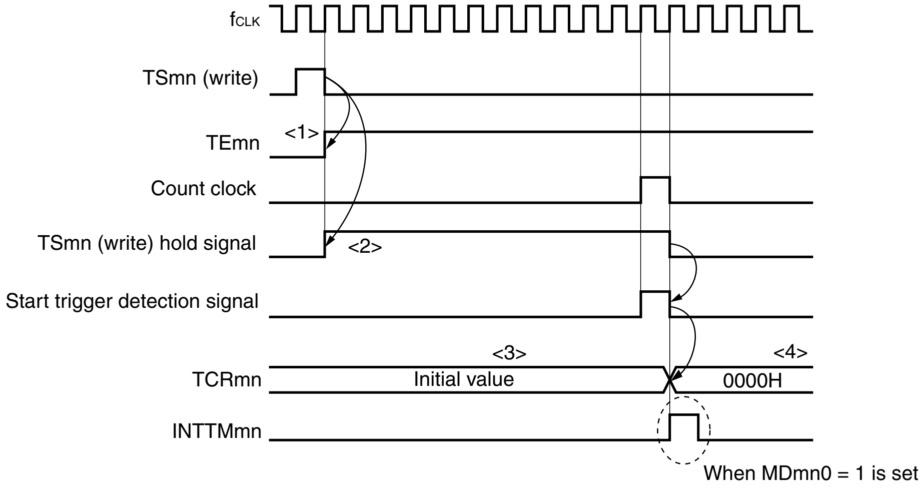
Figure 8-13. Start Timing (In Event Counter Mode)



(c) Start timing in capture mode

<1> Operation is enabled (TEmn = 1) by writing 1 to the TSmn.
<2> The write data to the TSmn is held until count clock generation.
<3> Timer/counter register mn (TCRmn) holds the initial value until count clock generation.
<4> On generation of count clock, 0000H is loaded to the TCRmn register and count starts.

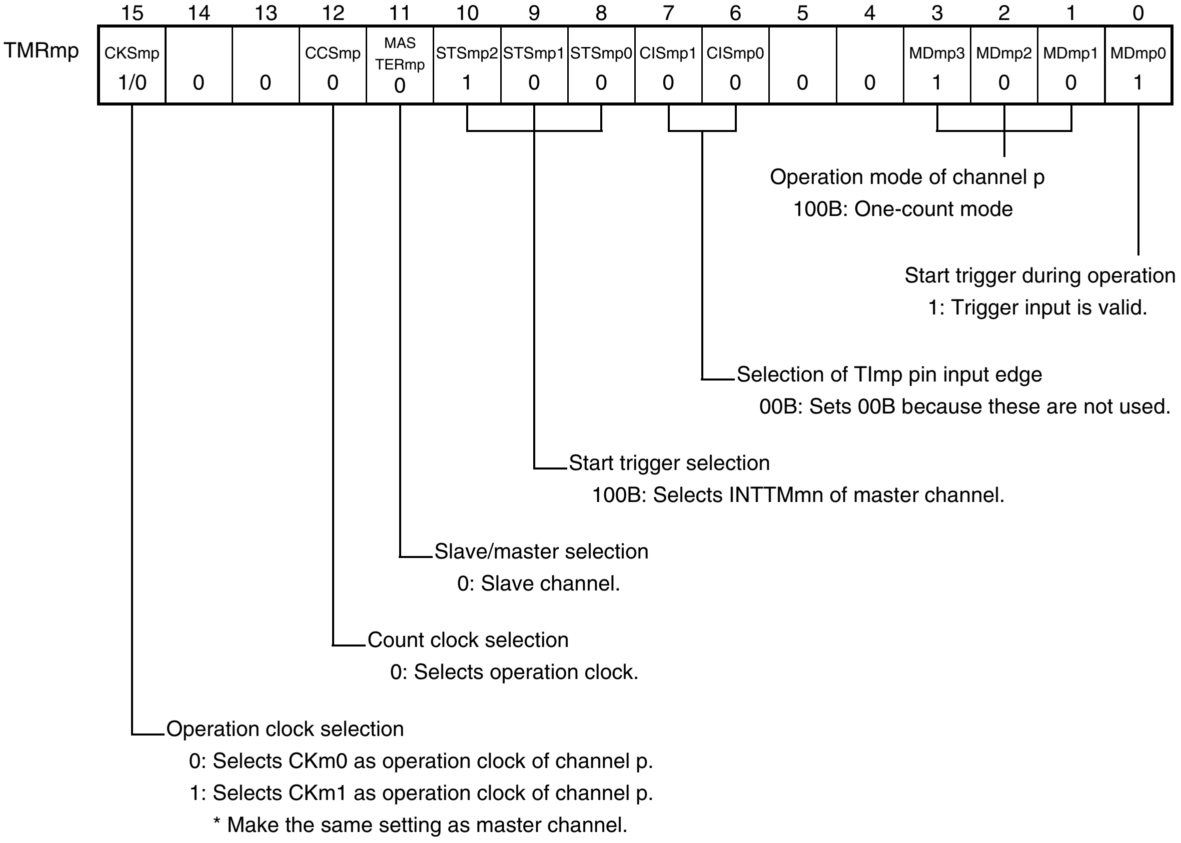
Figure 8-14. Start Timing (In Capture Mode)



Caution In the first cycle operation of count clock after writing TSmn, an error at a maximum of one clock is generated since count start delays until count clock has been generated. When the information on count start timing is necessary, an interrupt can be generated at count start by setting MDmn0 = 1.

Figure 8-61. Example of Set Contents of Registers When PWM Function (Slave Channel) Is Used

(a) Timer mode register mp (TMRmp)



	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmp	CKSmp 1/0	 0	 0	CCSmp 0	MAS TERmp 0	STSmp2 1	STSmp1 0	STSmp0 0	CISmp1 0	CISmp0 0	 0	 0	MDmp3 1	MDmp2 0	MDmp1 0	MDmp0 1

Operation mode of channel p
100B: One-count mode

Start trigger during operation
1: Trigger input is valid.

Selection of TImp pin input edge
00B: Sets 00B because these are not used.

Start trigger selection
100B: Selects INTTMmn of master channel.

Slave/master selection
0: Slave channel.

Count clock selection
0: Selects operation clock.

Operation clock selection
0: Selects CKm0 as operation clock of channel p.
1: Selects CKm1 as operation clock of channel p.
* Make the same setting as master channel.

(b) Timer output register m (TOm)

	Bit p
TOm	TOmp 1/0

0: Outputs 0 from TOmp.
1: Outputs 1 from TOmp.

(c) Timer output enable register m (TOEm)

	Bit p
TOEm	TOEmp 1/0

0: Stops the TOmp output operation by counting operation.
1: Enables the TOmp output operation by counting operation.

(d) Timer output level register m (TOLm)

	Bit p
TOLm	TOLmp 1/0

0: Positive logic output (active-high)
1: Inverted output (active-low)

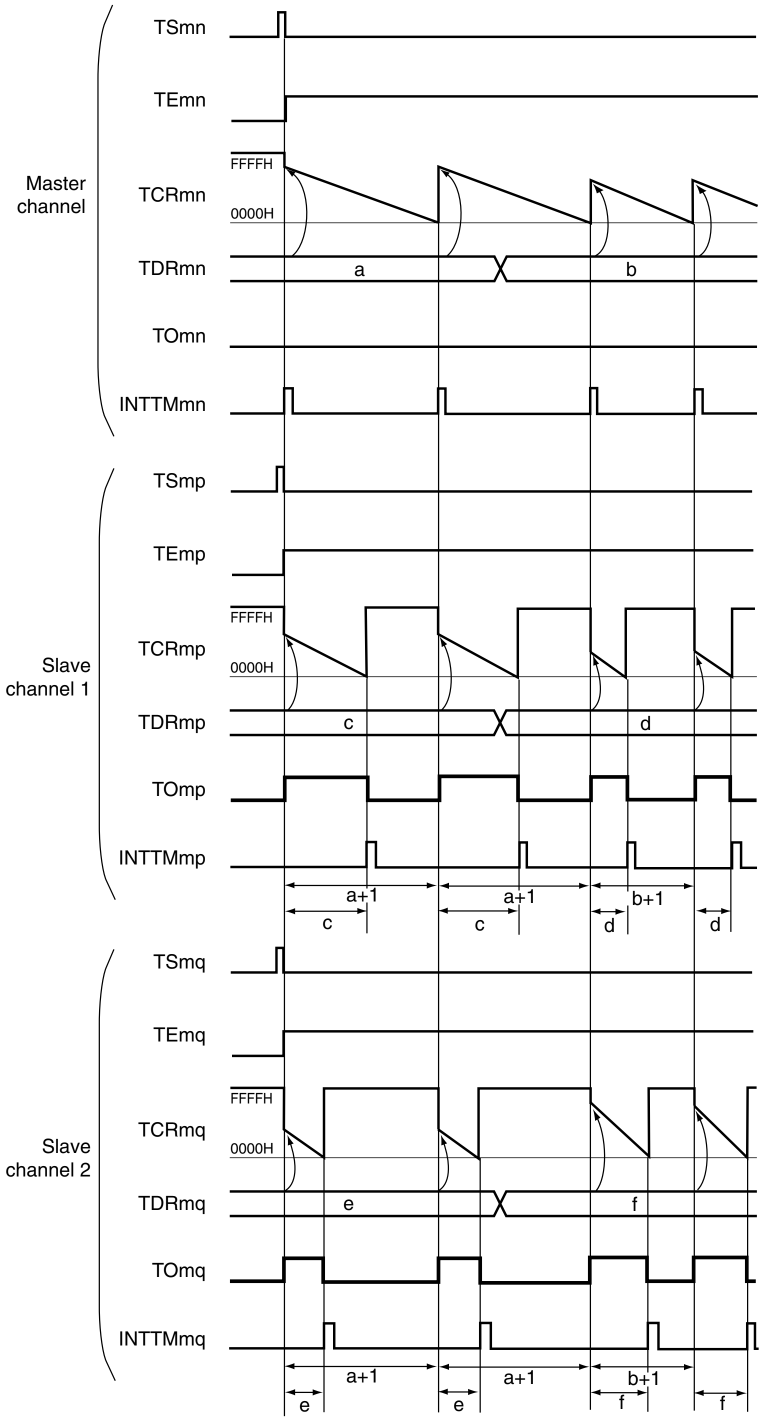
(e) Timer output mode register m (TOMm)

	Bit p
TOMm	TOMmp 1

1: Sets the slave channel output mode.

Remark m: Unit number, n: Channel number, p: Slave channel number (p = n+1),
When m = 0: n = 0, 2, 4, When m = 1: n = 0, 2
However, mp = 01 to 03, 05, 11, and 13 in the case of the timer output pin (TOmp).

Figure 8-64. Example of Basic Timing of Operation as Multiple PWM Output Function (output two types of PWMs) (1/2)



(**Remarks** are listed on the next page.)

12.5.7 Canceling wait

The I^{2}C usually cancels a wait state by the following processing.

- Writing data to IICA shift register (IICA)
- Setting bit 5 (WREL) of IICA control register 0 (IICCTL0) (canceling wait)
- Setting bit 1 (STT) of IICCTL0 register (generating start condition)[Note]
- Setting bit 0 (SPT) of IICCTL0 register (generating stop condition)[Note]

Note Master only

When the above wait canceling processing is executed, the I^{2}C cancels the wait state and communication is resumed.

To cancel a wait state and transmit data (including addresses), write the data to IICA register.

To receive data after canceling a wait state, or to complete data transmission, set bit 5 (WREL) of IICCTL0 register to 1.

To generate a restart condition after canceling a wait state, set bit 1 (STT) of IICCTL0 register to 1.

To generate a stop condition after canceling a wait state, set bit 0 (SPT) of IICCTL0 register to 1.

Execute the canceling processing only once for one wait state.

If, for example, data is written to IICA register after canceling a wait state by setting WREL bit to 1, an incorrect value may be output to SDA0 line because the timing for changing the SDA0 line conflicts with the timing for writing IICA register.

In addition to the above, communication is stopped if IICE bit is cleared to 0 when communication has been aborted, so that the wait state can be canceled.

If the I^{2}C bus has deadlocked due to noise, processing is saved from communication by setting bit 6 (LREL) of IICCTL0 register, so that the wait state can be canceled.

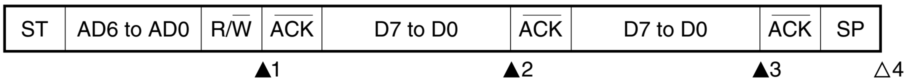
Caution If a processing to cancel a wait state is executed when WUP = 1, the wait state will not be canceled.

(3) Slave device operation (when receiving extension code)

The device is always participating in communication when it receives an extension code.

(a) Start ~ Code ~ Data ~ Data ~ Stop

(i) When WTIM = 0



▲1: IICS = 0010×010B

▲2: IICS = 0010×000B

▲3: IICS = 0010×000B

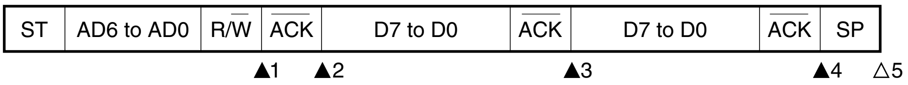
△4: IICS = 00000001B

Remark ▲: Always generated

△: Generated only when SPIE = 1

×: Don’t care

(ii) When WTIM = 1



▲1: IICS = 0010×010B

▲2: IICS = 0010×110B

▲3: IICS = 0010×100B

▲4: IICS = 0010××00B

△5: IICS = 00000001B

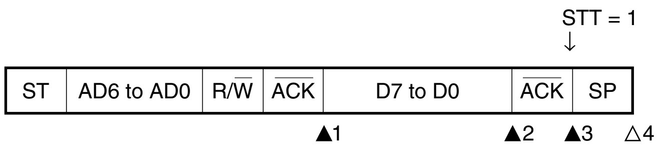
Remark ▲: Always generated

△: Generated only when SPIE = 1

×: Don’t care

(g) When arbitration loss occurs due to a stop condition when attempting to generate a restart condition

(i) When WTIM = 0



▲1: IICS = 1000×110B

▲2: IICS = 1000×000B (Sets WTIM bit to 1)

▲3: IICS = 1000××00B (Sets STT bit to 1)

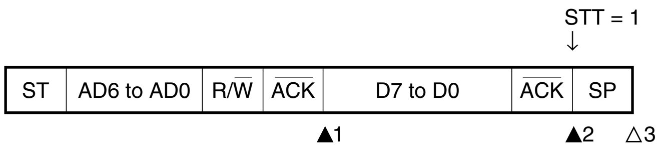
△4: IICS = 01000001B

Remark ▲: Always generated

△: Generated only when SPIE = 1

×: Don’t care

(ii) When WTIM = 1



▲1: IICS = 1000×110B

▲2: IICS = 1000××00B (Sets STT bit to 1)

△3: IICS = 01000001B

Remark ▲: Always generated

△: Generated only when SPIE = 1

×: Don’t care

Table 15-1. Interrupt Source List (1/2)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Maskable	0	INTWDTI	Watchdog timer interval[Note 3] (75% of overflow time)	Internal	0004H	(A)
	1	INTLVI	Low-voltage detection[Note 4]		0006H	
	2	INTP0	Pin input edge detection	External	0008H	(B)
	3	INTP1	Oercurrents detection of IO-Link[Note 5]		000AH	
	4	INTP2	Wakeup signal detection of IO-Link[Note 5]		000CH	
	5	INTP4	Pin input edge detection		0010H	
	6	INTP5			0012H	
	7	INTST3	UART3 transmission transfer end or buffer empty interrupt	Internal	0014H	(A)
	8	INTSR3	UART3 reception transfer end		0016H	
	9	INTSRE3	UART3 reception communication error occurrence		0018H	
	10	INTDMA0	End of DMA0 transfer		001AH	
	11	INTDMA1	End of DMA1 transfer		001CH	
	12	INTST0	UART0 transmission transfer end or buffer empty interrupt		001EH	
	13	INTSR0	UART0 reception transfer end		0020H	
	14	INTSRE0	UART0 reception communication error occurrence		0022H	
	15	INTIICA	End of IICA communication		002AH	
	16	INTTM00	End of timer array unit 0 channel 0 count or capture		002CH	
	17	INTTM01	End of timer array unit 0 channel 1 count or capture		002EH	
	18	INTTM02	End of timer array unit 0 channel 2 count or capture		0030H	
	19	INTTM03	End of timer array unit 0 channel 3 count or capture		0032H	
	20	INTAD	End of A/D conversion		0034H	
	21	INTST2 /INTCSI20 /INTIIC20	UART2 transmission transfer end or buffer empty interrupt/CSI20 transfer end or buffer empty interrupt/IIC20 transfer end		003CH	

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 32 indicates the lowest priority.

2. Basic configuration types (A) to (C) correspond to (A) to (C) in Figure 15-1.

3. When bit 7 (WDTINT) of the option byte (000C0H) is set to 1.

4. When bit 1 (LVIMD) of the low-voltage detection register (LVIM) is cleared to 0.

5. INTP1/P50 and INTP2/P51 are used for IO-Link communication.

16.2.2 STOP mode

(1) STOP mode setting and operating statuses

The STOP mode is set by executing the STOP instruction, and it can be set only when the external main system clock.

Cautions 1. Because the interrupt request signal is used to release the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately released if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction and the system returns to the operating mode as soon as the wait time set using the oscillation stabilization time select register (OSTS) has elapsed.

2. The STOP instruction cannot be executed when the CPU operates on the 20 MHz internal high-speed oscillation clock. Be sure to execute the STOP instruction after shifting to internal high-speed oscillation clock operation.

The operating statuses in the STOP mode are shown below.

Figure 21-1. Format of User Option Byte (000C0H/010C0H) (2/2)

Address: 000C0H/010C0H[Note 1]

7	6	5	4	3	2	1	0
WDTINIT	WINDOW1	WINDOW0	WDTON	WDCS2	WDCS1	WDCS0	WDSTBYON

WDSTBYON	Operation control of watchdog timer counter (HALT/STOP mode)
0	Counter operation stopped in HALT/STOP mode[Note 2]
1	Counter operation enabled in HALT/STOP mode

Notes 1. Set the same value as 000C0H to 010C0H when the boot swap operation is used because 000C0H is replaced by 010C0H.

2. The window open period is 100% when WDSTBYON = 0, regardless the value of WINDOW1 and WINDOW0.

Caution The watchdog timer continues its operation during self-programming of the flash memory and EEPROM emulation. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

Remark f_{IL}: Internal low-speed oscillation clock frequency

Figure 21-2. Format of User Option Byte (000C1H/010C1H)

Address: 000C1H/010C1H[Note 1]

7	6	5	4	3	2	1	0
1	1	1	1	1	FRQSEL2	FRQSEL1	LVIOFF

FRQSEL2	FRQSEL1	Internal high-speed oscillator frequency
0	1	8 MHz/20 MHz [Note 2]
1	0	1 MHz [Note 3]
Other than the above		Setting prohibited

LVIOFF	Setting of LVI on power application
0	LVI is ON by default (LVI default start function enabled) upon reset release (upon power application)
1	LVI is OFF by default (LVI default start function stopped) upon reset release (upon power application)

Notes 1. Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

2. When 8 MHz or 20 MHz has been selected, the 8 MHz internal high-speed oscillator automatically starts oscillating after reset release. To use the 20 MHz internal high-speed oscillator to operate the microcontroller, oscillation is started by setting bit 0 (DSCON) of the 20 MHz internal high-speed oscillation control register (DSCCTL) to 1 with $V_{DD} \geq 3.0$ V. The circuit cannot be changed to a 1 MHz internal high-speed oscillator while the microcontroller operates.

3. When 1 MHz has been selected, the microcontroller operates on the 1 MHz internal high-speed oscillator after reset release. The circuit cannot be changed to an 8 MHz or 20 MHz internal highspeed oscillator while the microcontroller operates.

(**Cautions** are listed on the next page.)

(3) During communication at same potential (CSI mode) (slave mode, $\overline{\text{SCK20}}$... external clock input)

(T_A = –40 to +85°C, 3.0 V ≤ V_{DD}/EV_{DD} = V_{DD_IO} ≤ 5.5 V, 4.75 V ≤ IV_{DD} ≤ 5.25 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}/EV_{DD}, V_{SS}/EV_{SS} = AV_{SS} = GND1 = GND2 = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK20}}$ cycle time	t_{KCY2}	4.0 V ≤ V_{DD}/EV_{DD} ≤ 5.5 V		6/f_{MCK}			ns
		3.0 V ≤ V_{DD}/EV_{DD} < 4.0 V	16 MHz < f_{MCK}	8/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}			ns
$\overline{\text{SCK20}}$ high-/low-level width	t_{KH2}, t_{KL2}			f_{KCY2}/2			ns
SI20 setup time (to $\overline{\text{SCK20}}$↑) Note 1	t_{SIK2}			80			ns
SI20 hold time (from $\overline{\text{SCK20}}$↑) Note 1	t_{KSI2}			1/f_{MCK}+50			ns
Delay time from $\overline{\text{SCK20}}$↓ to SO20 output Note 2	t_{KSO2}	C = 30 pF Note 3	4.0 V ≤ V_{DD}/EV_{DD} ≤ 5.5 V			2/f_{MCK}+45	ns
			3.0 V ≤ V_{DD}/EV_{DD} < 4.0 V			2/f_{MCK}+57	ns

Notes 1. When DAP10 = 0 and CKP10 = 0, or DAP10 = 1 and CKP10 = 1. The SI20 setup time becomes “to $\overline{\text{SCK20}}$↓” when DAP10 = 0 and CKP10 = 1, or DAP10 = 1 and CKP10 = 0.

2. When DAP10 = 0 and CKP10 = 0, or DAP10 = 1 and CKP10 = 1. The delay time to SO20 output becomes “from $\overline{\text{SCK20}}$↑” when DAP10 = 0 and CKP10 = 1, or DAP10 = 1 and CKP10 = 0.

3. C is the load capacitance of the SO20 output lines.

Caution Select the normal input buffer for SI20 and $\overline{\text{SCK20}}$ and the normal output mode for SO20 by using the PIM14 and POM14 registers.

Remark f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS10 bit of the SMR10 register.)

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