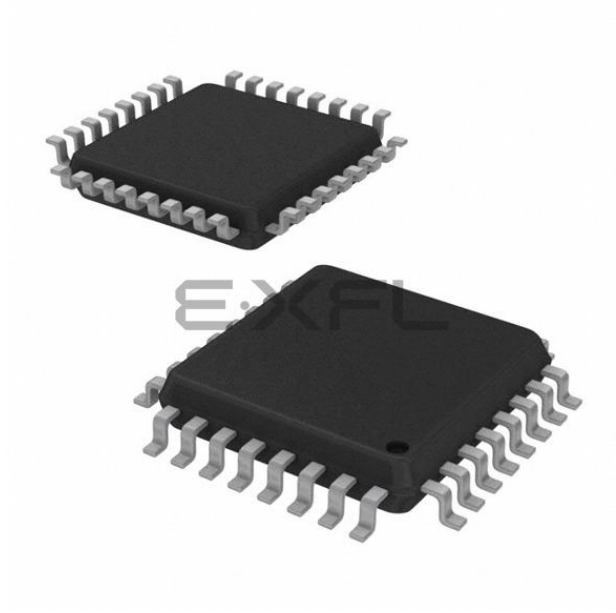

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	30
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3136tcy

1 Introduction

This document describes the features, pinout, mechanical data and ordering information of the medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x devices (microcontrollers with up to 32-Kbyte Flash memory density). These devices are referred to as medium-density devices in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031) and in STM8L and STM8AL Flash programming manual (PM0054).

For more details on the whole STMicroelectronics ultra-low-power family please refer to *Section 3: Functional overview on page 13*.

For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).

For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

Note: The medium-density devices provide the following benefits:

- Integrated system
  - Up to 32 Kbytes of medium-density embedded Flash program memory
  - 1 Kbytes of data EEPROM
  - Internal high speed and low-power low speed RC.
  - Embedded reset
- Ultra-low power consumption
  - 195 µA/MHZ + 440 µA (consumption)
  - 0.9 µA with LSI in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for Low power wait mode and Low power run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access.
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Wide choice of development tools

All devices offer 12-bit ADC, DAC, two comparators, Real-time clock three 16-bit timers, one 8-bit timer as well as standard communication interface such as SPI, I2C and USART. A 4x28-segment LCD is available on the medium-density STM8AL3Lxx line. *Table 2: Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x low-power device features and peripheral counts* and *Section 3: Functional overview* give an overview of the complete range of peripherals proposed in this family.

Figure 1 shows the general block diagram of the device family.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

Bootloader

A bootloader is available to reprogram the Flash memory using the USART1 interface. The reference document for the bootloader is *UM0560: STM8 bootloader user manual*.

Table 5. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48	VFQFPN32	LQFP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	5	5	PA5/TIM3_BKIN/ *[TIM3_ETR]*(4)/ LCD_COM1(2)/ADC1_IN1 /COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port A5	Timer 3 - break input / *[Timer 3 - trigger]* / LCD_COM 1 / ADC1 input 1 / Comparator 1 positive input
7	6	6	PA6/*[ADC1_TRIG]*(4)/ LCD_COM2(2)/ADC1_IN0 /COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port A6	*[ADC1 - trigger]* / LCD_COM2 / ADC1 input 0 / Comparator 1 positive input
8	-	-	PA7/LCD_SEG0(2)(5)	I/O	FT	X	X	X	HS	X	X	Port A7	LCD segment 0
24	13	13	PB0(6)/TIM2_CH1/ LCD_SEG10(2)/ ADC1_IN18/COMP1_INP	I/O	TT(3)	X(6)	X(6)	X	HS	X	X	Port B0	Timer 2 - channel 1 / LCD segment 10 / ADC1_IN18 / Comparator 1 positive input
25	14	14	PB1/TIM3_CH1/ LCD_SEG11(2)/ ADC1_IN17/COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port B1	Timer 3 - channel 1 / LCD segment 11 / ADC1_IN17 / Comparator 1 positive input
26	15	15	PB2/ TIM2_CH2/ LCD_SEG12(2)/ ADC1_IN16/COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port B2	Timer 2 - channel 2 / LCD segment 12 / ADC1_IN16/ Comparator 1 positive input
27	-	-	PB3/TIM2_ETR/ LCD_SEG13(2)/ ADC1_IN15/COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port B3	Timer 2 - trigger / LCD segment 13 /ADC1_IN15 / Comparator 1 positive input
-	16	16	PB3/*[TIM2_ETR]*(4)/ TIM1_CH2N/LCD_SEG13 (2)/ADC1_IN15/ COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port B3	*[Timer 2 - trigger]* / Timer 1 inverted channel 2 / LCD segment 13 / ADC1_IN15 / Comparator 1 positive input

Table 6. Flash and RAM boundary addresses

Memory area	Size	Start address	End address
RAM	2 Kbyte	0x00 0000	0x00 07FF
Flash program memory	8 Kbyte	0x00 8000	0x00 9FFF
	16 Kbyte		0x00 BFFF
	32 Kbyte		

5.2 Register map

Table 7. Factory conversion registers

Address	Block	Register label	Register name	Reset status
0x00 4910	-	VREFINT_Factory_CONV(1)	Internal reference voltage factory conversion	0xXX
0x00 4911	-	TS_Factory_CONV_V125(2)	Temperature sensor output voltage	0xXX

1. The VREFINT_Factory_CONV byte represents the 8 LSB of the result of the VREFINT 12-bit ADC conversion performed in factory. The MSB have a fixed value: 0x6.
2. The TS_Factory_CONV_V125 byte represents the 8 LSB of the result of the V125 12-bit ADC conversion performed in factory. The 2 MSB have a fixed value: 0x3.

Table 8. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x01
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 507F	DMA1	DMA1_C1CR	DMA1 channel 1 configuration register	0x00
0x00 5080		DMA1_C1SPR	DMA1 channel 1 status & priority register	0x00
0x00 5081		DMA1_C1NDTR	DMA1 number of data to transfer register (channel 1)	0x00
0x00 5082		DMA1_C1PARH	DMA1 peripheral address high register (channel 1)	0x52
0x00 5083		DMA1_C1PARL	DMA1 peripheral address low register (channel 1)	0x00
0x00 5084		Reserved area (1 byte)		
0x00 5085		DMA1_C1M0ARH	DMA1 memory 0 address high register (channel 1)	0x00
0x00 5086		DMA1_C1M0ARL	DMA1 memory 0 address low register (channel 1)	0x00
0x00 5087 0x00 5088		Reserved area (2 bytes)		
0x00 5089		DMA1_C2CR	DMA1 channel 2 configuration register	0x00
0x00 508A		DMA1_C2SPR	DMA1 channel 2 status & priority register	0x00
0x00 508B		DMA1_C2NDTR	DMA1 number of data to transfer register (channel 2)	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 508C	DMA1	DMA1_C2PARH	DMA1 peripheral address high register (channel 2)	0x52
0x00 508D		DMA1_C2PARL	DMA1 peripheral address low register (channel 2)	0x00
0x00 508E		Reserved area (1 byte)		
0x00 508F		DMA1_C2M0ARH	DMA1 memory 0 address high register (channel 2)	0x00
0x00 5090		DMA1_C2M0ARL	DMA1 memory 0 address low register (channel 2)	0x00
0x00 5091 0x00 5092		Reserved area (2 bytes)		
0x00 5093		DMA1_C3CR	DMA1 channel 3 configuration register	0x00
0x00 5094		DMA1_C3SPR	DMA1 channel 3 status & priority register	0x00
0x00 5095		DMA1_C3NDTR	DMA1 number of data to transfer register (channel 3)	0x00
0x00 5096		DMA1_C3PARH_ C3M1ARH	DMA1 peripheral address high register (channel 3)	0x40
0x00 5097		DMA1_C3PARL_ C3M1ARL	DMA1 peripheral address low register (channel 3)	0x00
0x00 5098		Reserved area (1 byte)		
0x00 5099		DMA1_C3M0ARH	DMA1 memory 0 address high register (channel 3)	0x00
0x00 509A		DMA1_C3M0ARL	DMA1 memory 0 address low register (channel 3)	0x00
0x00 509B to 0x00 509D		Reserved area (3 bytes)		
0x00 509E	SYSCFG	SYSCFG_RMPCR1	Remapping register 1	0x00
0x00 509F		SYSCFG_RMPCR2	Remapping register 2	0x00
0x00 50A0	ITC - EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF1	External interrupt port select register 1	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8		WFE_CR3	WFE control register 3	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 540C	LCD	LCD_RAM0	LCD display memory 0	0x00
0x00 540D		LCD_RAM1	LCD display memory 1	0x00
0x00 540E		LCD_RAM2	LCD display memory 2	0x00
0x00 540F		LCD_RAM3	LCD display memory 3	0x00
0x00 5410		LCD_RAM4	LCD display memory 4	0x00
0x00 5411		LCD_RAM5	LCD display memory 5	0x00
0x00 5412		LCD_RAM6	LCD display memory 6	0x00
0x00 5413		LCD_RAM7	LCD display memory 7	0x00
0x00 5414		LCD_RAM8	LCD display memory 8	0x00
0x00 5415		LCD_RAM9	LCD display memory 9	0x00
0x00 5416		LCD_RAM10	LCD display memory 10	0x00
0x00 5417		LCD_RAM11	LCD display memory 11	0x00
0x00 5418		LCD_RAM12	LCD display memory 12	0x00
0x00 5419		LCD_RAM13	LCD display memory 13	0x00
0x00 541A to 0x00 542F	Reserved area (22 bytes)			
0x00 5430	RI	Reserved area (1 byte)		0x00
0x00 5431		RI_ICR1	Timer input capture routing register 1	0x00
0x00 5432		RI_ICR2	Timer input capture routing register 2	0x00
0x00 5433		RI_IOIR1	I/O input register 1	undefined
0x00 5434		RI_IOIR2	I/O input register 2	undefined
0x00 5435		RI_IOIR3	I/O input register 3	undefined
0x00 5436		RI_IOCMR1	I/O control mode register 1	0x00
0x00 5437		RI_IOCMR2	I/O control mode register 2	0x00
0x00 5438		RI_IOCMR3	I/O control mode register 3	0x00
0x00 5439		RI_IOSR1	I/O switch register 1	0x00
0x00 543A		RI_IOSR2	I/O switch register 2	0x00
0x00 543B		RI_IOSR3	I/O switch register 3	0x00
0x00 543C		RI_IOGCR	I/O group control register	0x3F
0x00 543D		RI_ASCR1	Analog switch register 1	0x00
0x00 543E		RI_ASCR2	Analog switch register 2	0x00
0x00 543F		RI_RCR	Resistor control register 1	0x00

Table 13. Option byte description (continued)

Option byte no.	Option description
OPT5	**BOR_ON**: 0: Brownout reset off 1: Brownout reset on
	BOR_TH[3:1]: Brownout reset thresholds. Refer to *Table 20* for details on the thresholds according to the value of BOR_TH bits.
OPTBL	**OPTBL[15:0]**: This option is checked by the boot ROM code after reset. Depending on the content of addresses Ox00 480B, Ox00 480C and 0x8000 (reset vector) the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 bootloader user manual for more details.

Table 16. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by IR_TIM pin (with high sink LED driver capability)	80	
	Output current sunk by any other I/O and control pin	25	
	Output current sourced by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$	Injected current on true open-drain pins (PC0 and PC1)(1)	- 5/+0	
	Injected current on five-volt tolerant (FT) pins (PA7 and PE0)(1)	- 5/+0	
	Injected current on 3.6 V tolerant (TT) pins(1)	- 5/+0	
	Injected current on any other pin(2)	- 5/+5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(3)	± 25	

1. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15* for maximum allowed input voltage values.
2. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15* for maximum allowed input voltage values.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	° C
T_J	Maximum junction temperature	150	

Table 18. Operating lifetime (OLF)(1)

Symbol	Ratings	Value	Unit
OLF	Conforming to AEC-Q100	-40 to 125 °C	Grade 1

1. For detailed mission profile analysis, please contact the local ST Sales Office.

Table 24. Total current consumption in low-power wait mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions(1)			Typ	Max	Unit
$I_{DD(LPW)}$	Supply current in Low power wait mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	3.00	3.30(2)	µA
				T_A = 85 °C	4.40	9(3)	
				T_A = 125 °C	11.00	18(3)	
		LSE external clock(4) (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	2.35	2.70(2)	
				T_A = 85 °C	3.10	3.70(2)	
				T_A = 125 °C	7.20	11.00(2)	

1. No floating I/Os.
2. Guaranteed by characterization results.
3. Tested at 85°C for temperature range A or 125°C for temperature range C.
4. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 33*.

Table 25. Total current consumption and timing in active-halt mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions (1)			Typ	Max(2)	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSI RC (at 38 kHz)	LCD OFF(3)	T_A = -40 °C to 25 °C	0.90	2.10	µA
				T_A = 85 °C	1.50	3.40	
				T_A = 125 °C	5.10	12.00	
			LCD ON (static duty/ external V_{LCD}) (4)	T_A = -40 °C to 25 °C	1.40	3.10	
				T_A = 85 °C	1.90	4.30	
				T_A = 125 °C	5.50	13.00	
			LCD ON (1/4 duty/ external V_{LCD}) (5)	T_A = -40 °C to 25 °C	1.90	4.30	
				T_A = 85 °C	2.40	5.40	
				T_A = 125 °C	6.00	15.00	
			LCD ON (1/4 duty/ internal V_{LCD}) (6)	T_A = -40 °C to 25 °C	3.90	8.75	
				T_A = 85 °C	4.50	10.20	
				T_A = 125 °C	6.80	16.30	

Table 26. Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal

Symbol	Parameter	Condition[1]		Typ	Unit
$I_{DD(AH)}$[2]	Supply current in Active-halt mode	V_{DD} = 1.8 V	LSE	1.15	µA
			LSE/32[3]	1.05	
		V_{DD} = 3 V	LSE	1.30	
			LSE/32[3]	1.20	
		V_{DD} = 3.6 V	LSE	1.45	
			LSE/32[3]	1.35	

1. No floating I/O, unless otherwise specified.
2. Data based on measurements on bench, including 32.768 kHz external crystal oscillator consumption.
3. RTC clock is LSE divided by 32.

Table 27. Total current consumption and timing in Halt mode at V_{DD} = 1.65 to 3.6 V

Symbol	Parameter	Condition[1]	Typ	Max	Unit
$I_{DD(Halt)}$	Supply current in Halt mode (ultra low power ULP bit =1 in the PWR_CSR2 register)	T_A = -40 °C to 25 °C	0.4	0.9[4]	µA
		T_A = 85 °C	0.9	2.8[2]	
		T_A = 125 °C	4.4	13[2]	
$I_{DD(WUHalt)}$	Supply current during wakeup time from Halt mode (using HSI)	-	2.4	-	mA
$t_{WU\_HSI(Halt)}$[3][5]	Wakeup time from Halt to Run mode (using HSI)	-	4.7	7[4]	µs
$t_{WU\_LSI(Halt)}$[3][5]	Wakeup time from Halt mode to Run mode (using LSI)	-	150	-	

1. T_A = -40 to 125 °C, no floating I/O, unless otherwise specified.
2. Tested at 85°C for temperature range A or 125°C for temperature range C.
3. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.
4. Guaranteed by characterization results.
5. Wakeup time until start of interrupt vector fetch. The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.

HSE crystal/ceramic resonator oscillator

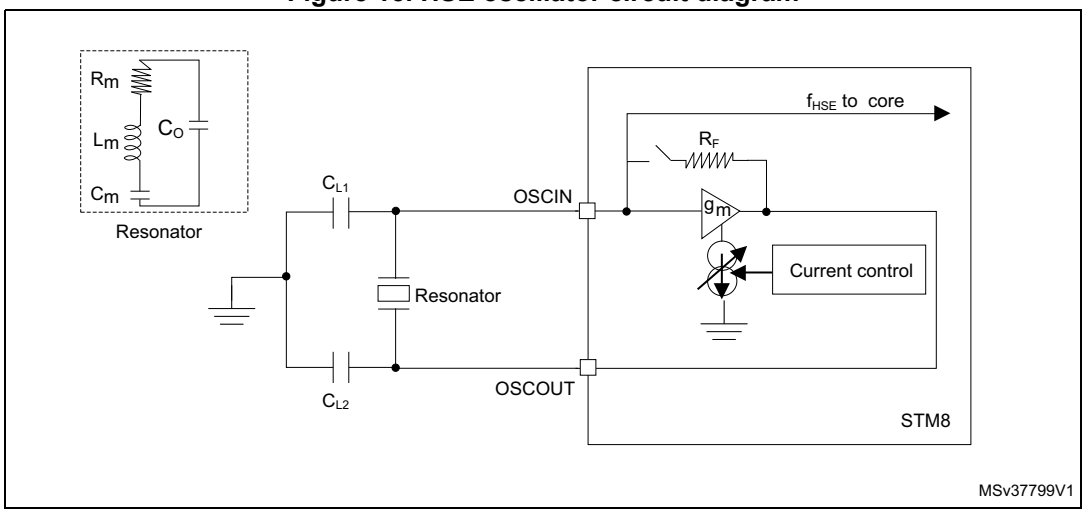
The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 32. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	High speed external oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$C^{(1)}$	Recommended load capacitance $^{(2)}$	-	-	20	-	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)$^{(3)}$	mA
		C = 10 pF, f_{OSC} =16 MHz	-	-	2.5 (startup) 0.46 (stabilized)$^{(3)}$	
g_m	Oscillator transconductance	-	3.5$^{(3)}$	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

1. $C=C_{L1}=C_{L2}$ is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Guaranteed by design.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 15. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

Figure 22. Typical pull-up current I_{pu} vs V_{DD} with $V_{IN}=V_{SS}$

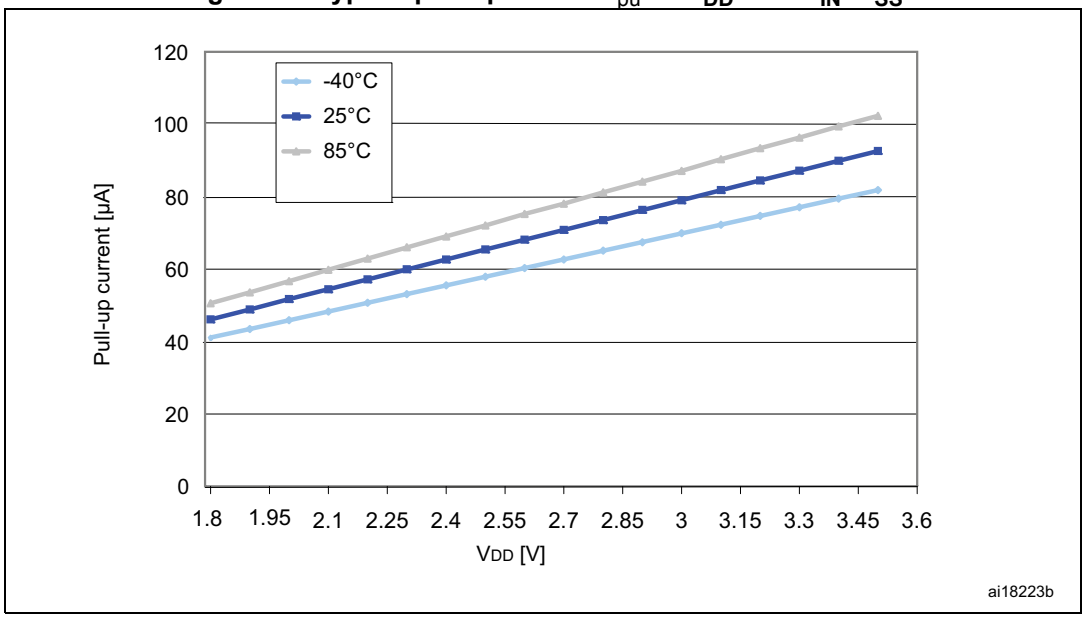


Figure 23. Typ. V_{OL} @ V_{DD} = 3.0 V (high sink ports)

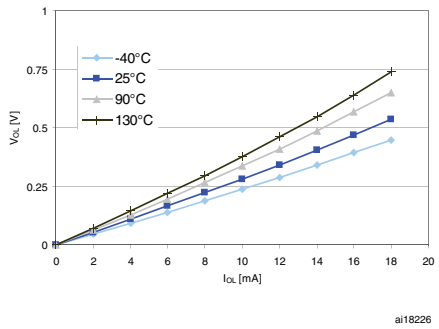


Figure 24. Typ. V_{OL} @ V_{DD} = 1.8 V (high sink ports)

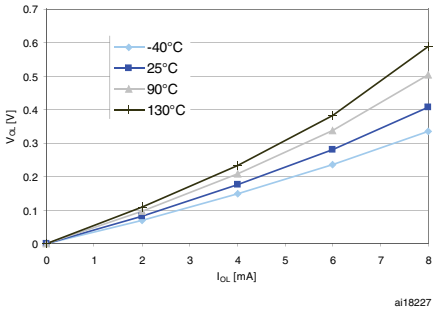


Figure 25. Typ. V_{OL} @ V_{DD} = 3.0 V (true open drain ports)

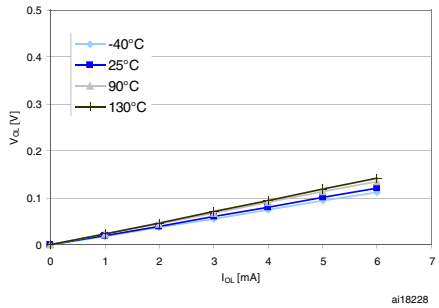


Figure 26. Typ. V_{OL} @ V_{DD} = 1.8 V (true open drain ports)

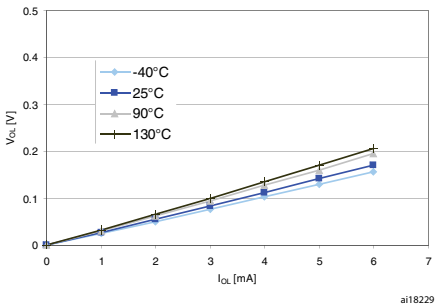


Figure 27. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.0 V (high sink ports)

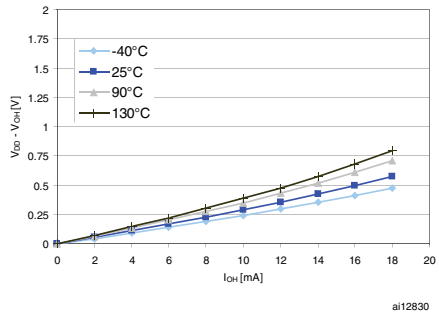


Figure 28. Typ. V_{DD} - V_{OH} @ V_{DD} = 1.8 V (high sink ports)

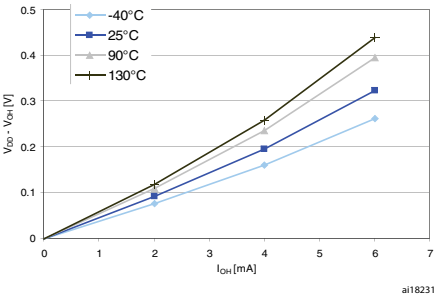


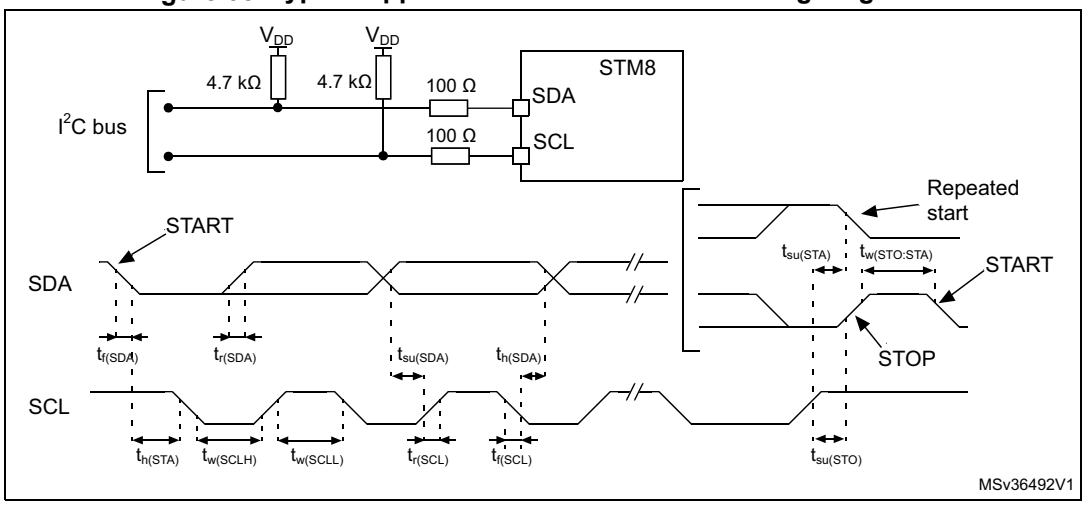
Table 47. I²C characteristics (continued)

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max (2)	Min (2)	Max (2)	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0		0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{SYSCLK} must be at least equal to 8 MHz to achieve max fast I²C speed (400 kHz).
2. Data based on standard I²C protocol requirements, not tested in production.

Note: For speeds around 200 kHz, the achieved speed can have a ± 5% tolerance
For other speed ranges, the achieved speed can have a ± 2% tolerance
The above variations depend on the accuracy of the external components used.

Figure 35. Typical application with I²C bus and timing diagram(1)



1. Measurement points are done at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}

In the following table, data are guaranteed by design, not tested in production unless otherwise specified.

Table 52. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
T_A	Temperature range	-	-40	-	125	°C
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	µs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay in slow mode(2)	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	1.8	3.5	
		2.7 V ≤ V_{DDA} ≤ 3.6 V		2.5	6	
$t_{d\ fast}$	Propagation delay in fast mode(2)	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	0.8	2	
		2.7 V ≤ V_{DDA} ≤ 3.6 V		1.2	4	
V_{offset}	Comparator offset error	-	-	±4	±20	mV
I_{COMP2}	Current consumption(3)	Fast mode	-	3.5	5	µA
		Slow mode		0.5	2	

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

9.3.13 12-bit DAC characteristics

In the following table, data are guaranteed by design, not tested in production.

Table 53. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	-	1.8	-	V_{DDA}	

Static latch-up

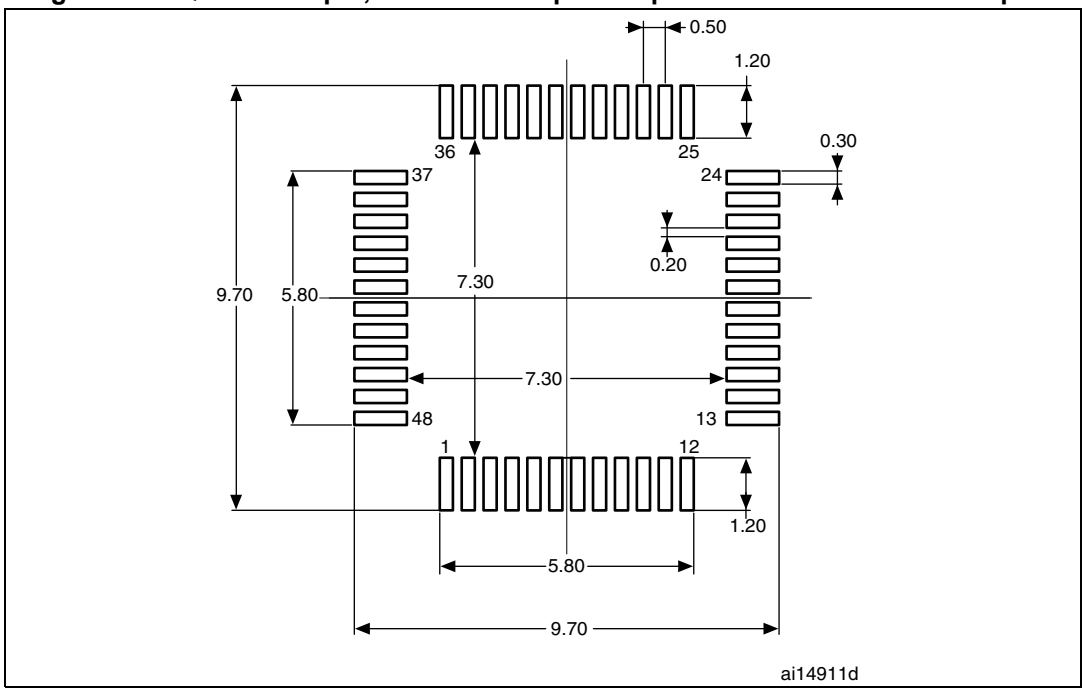
- **LU**: three complementary static tests are required on 6 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 64. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A = 125 °C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

Figure 42. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint

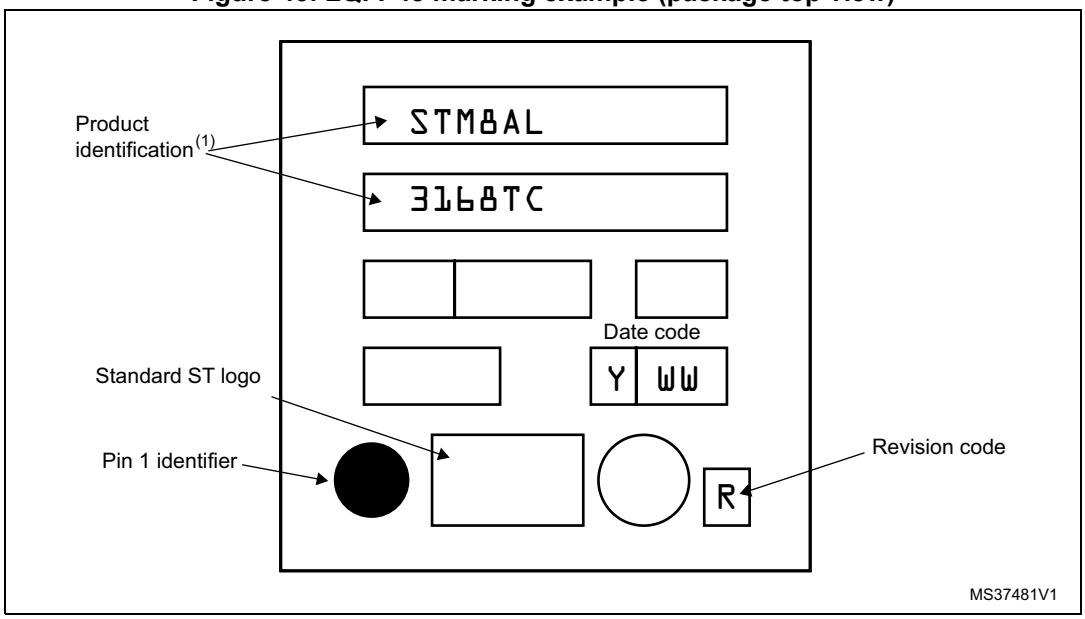


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 43. LQFP48 marking example (package top view)



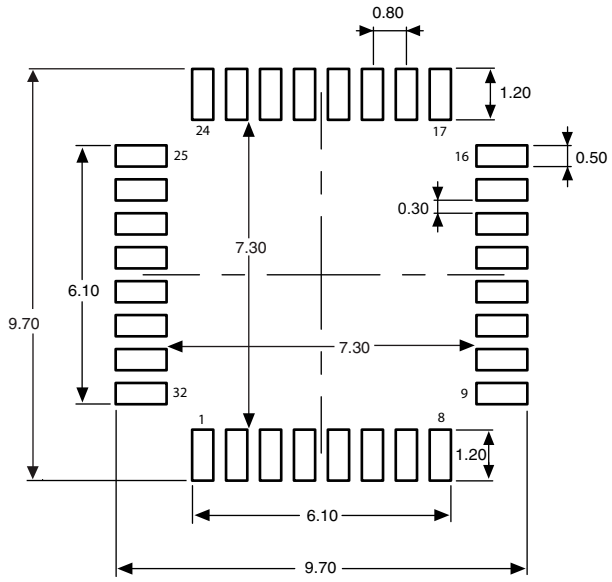
1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Table 66. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 45. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat recommended footprint



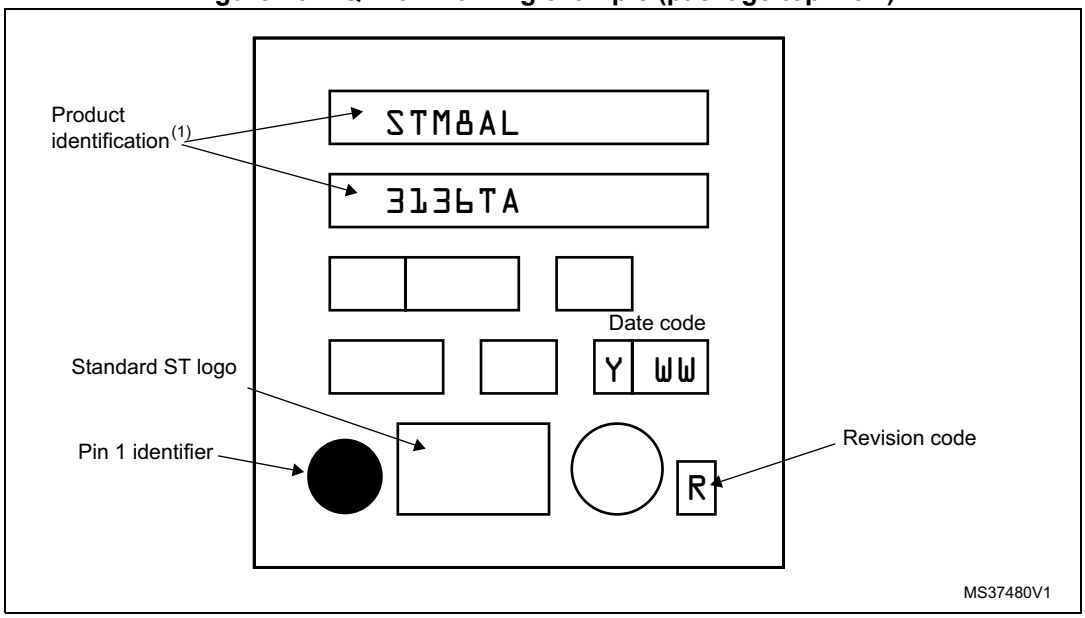
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 46. LQFP32 marking example (package top view)



1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.