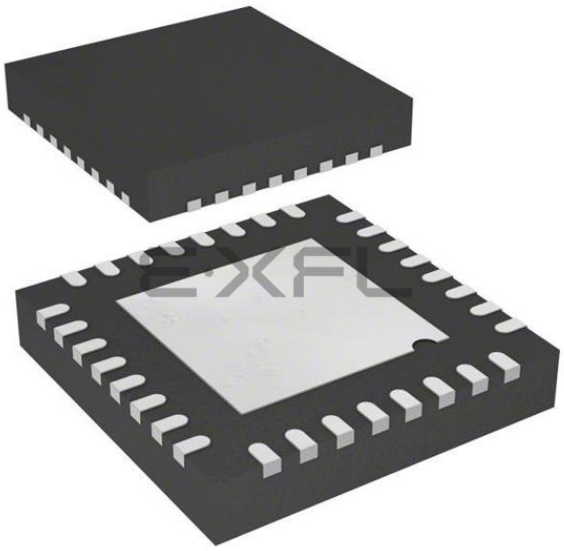

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	30
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3146ucy

- Development support
  - Fast on-chip programming and non intrusive debugging with SWIM
  - Bootloader using USART
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM8AL313x/4x/6x (without LCD)	STM8AL3136, STM8AL3138, STM8AL3146, STM8AL3148, STM8AL3166, STM8AL3168
STM8AL3L4x/6x (with LCD)	STM8AL3L46, STM8AL3L48, STM8AL3L66, STM8AL3L68

3.13.3 8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow or for DAC trigger generation.

3.14 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

3.14.1 Window watchdog timer

The window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

3.14.2 Independent watchdog timer

The independent watchdog peripheral (IWDG) can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

3.15 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

3.16 Communication interfaces

3.16.1 SPI

The serial peripheral interface (SPI1) provides half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s ($f_{SYSCLK}/2$) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

Note: SPI1 can be served by the DMA1 Controller.

3.16.2 I²C

The I^2C bus interface (I^2C1) provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz
- 7-bit and 10-bit addressing modes
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: I^2C1 can be served by the DMA1 Controller.

3.16.3 USART

The USART interface (USART1) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- SmartCard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Note: USART1 can be served by the DMA1 Controller.

USART1 can be used to implement LIN slave communication, with LIN Break detection on the framing error flag (FE in USART_SR register) with a value of 0 in the USART data register (USART_DR).

3.17 Infrared (IR) interface

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.18 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment.
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Figure 7. STM8AL31x6U 32-pin pinout (without LCD)

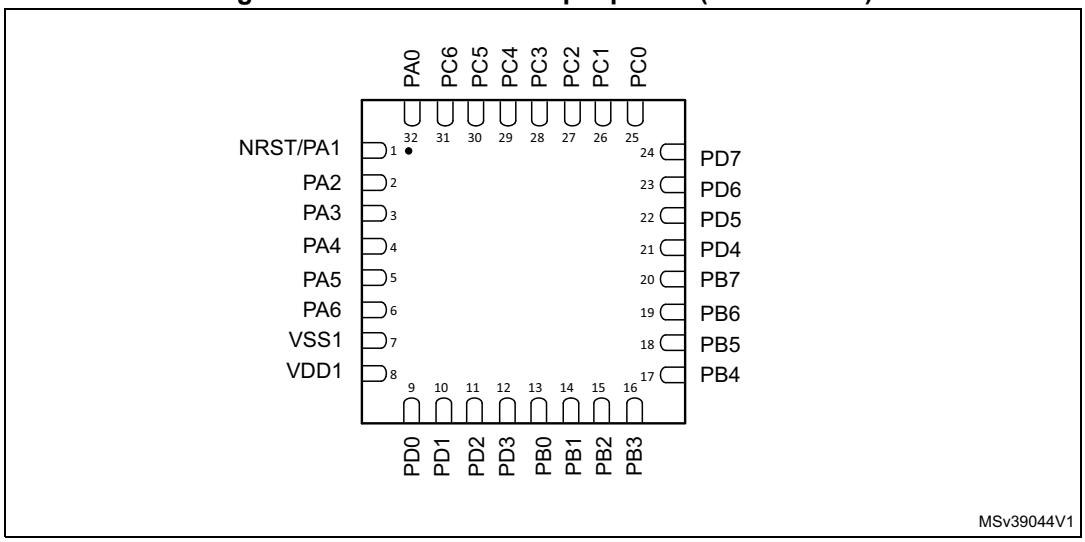


Figure 8. STM8AL3Lx6U 32-pin pinout (with LCD)

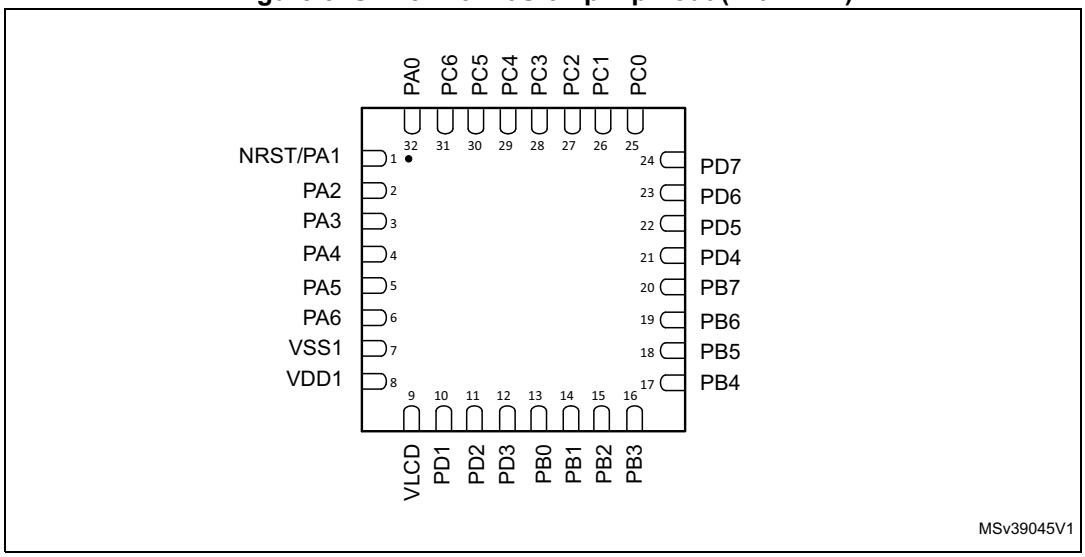


Table 5. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48	VFQFPN32	LQFP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	5	5	PA5/TIM3_BKIN/ *[TIM3_ETR]*(4)/ LCD_COM1(2)/ADC1_IN1 /COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port A5	Timer 3 - break input / *[Timer 3 - trigger]* / LCD_COM 1 / ADC1 input 1 / Comparator 1 positive input
7	6	6	PA6/*[ADC1_TRIG]*(4)/ LCD_COM2(2)/ADC1_IN0 /COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port A6	*[ADC1 - trigger]* / LCD_COM2 / ADC1 input 0 / Comparator 1 positive input
8	-	-	PA7/LCD_SEG0(2)(5)	I/O	FT	X	X	X	HS	X	X	Port A7	LCD segment 0
24	13	13	PB0(6)/TIM2_CH1/ LCD_SEG10(2)/ ADC1_IN18/COMP1_INP	I/O	TT(3)	X(6)	X(6)	X	HS	X	X	Port B0	Timer 2 - channel 1 / LCD segment 10 / ADC1_IN18 / Comparator 1 positive input
25	14	14	PB1/TIM3_CH1/ LCD_SEG11(2)/ ADC1_IN17/COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port B1	Timer 3 - channel 1 / LCD segment 11 / ADC1_IN17 / Comparator 1 positive input
26	15	15	PB2/ TIM2_CH2/ LCD_SEG12(2)/ ADC1_IN16/COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port B2	Timer 2 - channel 2 / LCD segment 12 / ADC1_IN16/ Comparator 1 positive input
27	-	-	PB3/TIM2_ETR/ LCD_SEG13(2)/ ADC1_IN15/COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port B3	Timer 2 - trigger / LCD segment 13 /ADC1_IN15 / Comparator 1 positive input
-	16	16	PB3/*[TIM2_ETR]*(4)/ TIM1_CH2N/LCD_SEG13 (2)/ADC1_IN15/ COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port B3	*[Timer 2 - trigger]* / Timer 1 inverted channel 2 / LCD segment 13 / ADC1_IN15 / Comparator 1 positive input

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50A9 to 0x00 50AF	Reserved area (7 bytes)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2	PWR	PWR_CSR1	Power control and status register 1	0x00
0x00 50B3		PWR_CSR2	Power control and status register 2	0x00
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_DIVR	Clock master divider register	0x03
0x00 50C1		CLK_CRTCR	Clock RTC register	0x00
0x00 50C2		CLK_ICKR	Internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	Peripheral clock gating register 1	0x00
0x00 50C4		CLK_PCKENR2	Peripheral clock gating register 2	0x80
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6		CLK_ECKR	External clock control register	0x00
0x00 50C7		CLK_SCSR	System clock status register	0x01
0x00 50C8		CLK_SWR	System clock switch register	0x01
0x00 50C9		CLK_SWCR	Clock switch control register	0bxxxx0000
0x00 50CA		CLK_CSSR	Clock security system register	0x00
0x00 50CB		CLK_CBEEPR	Clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	HSI calibration register	0xxx
0x00 50CD		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	Main regulator control status register	0bxx11100x
0x00 50D0 to 0x00 50D2	Reserved area (3 bytes)			
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDR window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 slave mode control register	0x00
0x00 52E3		TIM4_DER	TIM4 DMA1 request enable register	0x00
0x00 52E4		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 52E5		TIM4_SR1	TIM4 status register 1	0x00
0x00 52E6		TIM4_EGR	TIM4 event generation register	0x00
0x00 52E7		TIM4_CNTR	TIM4 counter	0x00
0x00 52E8		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E9		TIM4_ARR	TIM4 auto-reload register	0x00
0x00 52EA to 0x00 52FE	Reserved area (21 bytes)			
0x00 52FF	IRTIM	IR_CR	Infrared control register	0x00
0x00 5300 to 0x00 533F	Reserved area (64 bytes)			
0x00 5340	ADC1	ADC1_CR1	ADC1 configuration register 1	0x00
0x00 5341		ADC1_CR2	ADC1 configuration register 2	0x00
0x00 5342		ADC1_CR3	ADC1 configuration register 3	0x1F
0x00 5343		ADC1_SR	ADC1 status register	0x00
0x00 5344		ADC1_DRH	ADC1 data register high	0x00
0x00 5345		ADC1_DRL	ADC1 data register low	0x00
0x00 5346		ADC1_HTRH	ADC1 high threshold register high	0x0F
0x00 5347		ADC1_HTRL	ADC1 high threshold register low	0xFF
0x00 5348		ADC1_LTRH	ADC1 low threshold register high	0x00
0x00 5349		ADC1_LTRL	ADC1 low threshold register low	0x00
0x00 534A		ADC1_SQR1	ADC1 channel sequence 1 register	0x00
0x00 534B		ADC1_SQR2	ADC1 channel sequence 2 register	0x00
0x00 534C		ADC1_SQR3	ADC1 channel sequence 3 register	0x00
0x00 534D		ADC1_SQR4	ADC1 channel sequence 4 register	0x00
0x00 534E		ADC1_TRIGR1	ADC1 trigger disable 1	0x00
0x00 534F		ADC1_TRIGR2	ADC1 trigger disable 2	0x00
0x00 5350		ADC1_TRIGR3	ADC1 trigger disable 3	0x00
0x00 5351		ADC1_TRIGR4	ADC1 trigger disable 4	0x00

Table 16. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by IR_TIM pin (with high sink LED driver capability)	80	
	Output current sunk by any other I/O and control pin	25	
	Output current sourced by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$	Injected current on true open-drain pins (PC0 and PC1)(1)	- 5/+0	
	Injected current on five-volt tolerant (FT) pins (PA7 and PE0)(1)	- 5/+0	
	Injected current on 3.6 V tolerant (TT) pins(1)	- 5/+0	
	Injected current on any other pin(2)	- 5/+5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(3)	± 25	

1. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15* for maximum allowed input voltage values.
2. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15* for maximum allowed input voltage values.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	° C
T_J	Maximum junction temperature	150	

Table 18. Operating lifetime (OLF)(1)

Symbol	Ratings	Value	Unit
OLF	Conforming to AEC-Q100	-40 to 125 °C	Grade 1

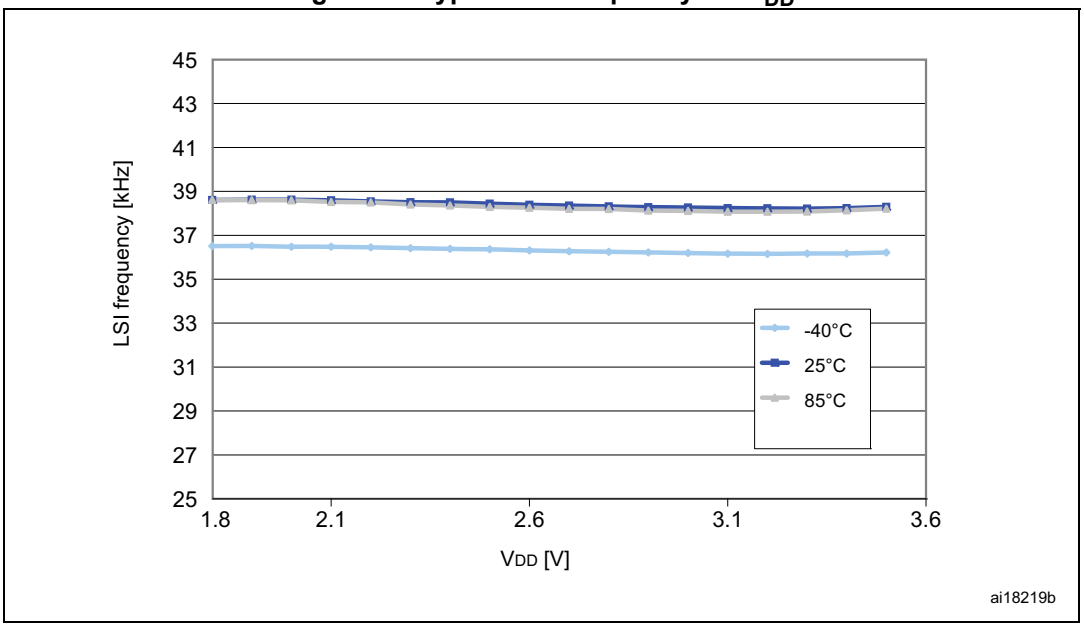
1. For detailed mission profile analysis, please contact the local ST Sales Office.

Table 21. Total current consumption in Run mode (continued)

Symbol	Parameter	Conditions			Typ	Max	Unit
$I_{DD(RUN)}$	Supply current in Run mode	All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI RC osc.(5)	f_{CPU} = 125 kHz	0.45	0.60(3)	mA
				f_{CPU} = 1 MHz	0.60	0.85(3)	
				f_{CPU} = 4 MHz	1.10	1.45(3)	
				f_{CPU} = 8 MHz	1.90	2.40(3)	
				f_{CPU} = 16 MHz	3.80	4.90	
			HSE external clock (f_{CPU}=f_{HSE}) (4)	f_{CPU} = 125 kHz	0.30	0.45(3)	
				f_{CPU} = 1 MHz	0.40	0.55(3)	
				f_{CPU} = 4 MHz	1.15	1.50(3)	
				f_{CPU} = 8 MHz	2.15	2.75(3)	
				f_{CPU} = 16 MHz	4.00	4.75(3)	
			LSI RC osc.	f_{CPU} = f_{LSI}	100	150(3)	µA
			LSE external clock (32.768 kHz)(6)	f_{CPU} = f_{LSE}	100	120(3)	

1. CPU executing typical data processing
2. The run from RAM consumption can be approximated with the linear formula: I_{DD}(run_from_RAM) = Freq * 90 µA/MHz + 400µA
3. Guaranteed by characterization results.
4. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 32*.
5. The run from Flash consumption can be approximated with the linear formula: I_{DD}(run_from_Flash) = Freq * 195 µA/MHz + 440 µA
6. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 33*.

Figure 18. Typical LSI frequency vs. V_{DD}



9.3.5 Memory characteristics

T_A = -40 to 125 °C unless otherwise specified.

Table 36. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization results.

Flash memory

Table 37. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{SYSCLK} = 16 MHz	1.65	-	3.6	V
t_{prog}	Programming time for 1 or 128 bytes (block) erase/write cycles (on programmed byte)	-	-	6	-	ms
	Programming time for 1 to 128 bytes (block) write cycles (on erased byte)	-	-	3	-	
I_{prog}	Programming/ erasing consumption	T_A = +25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A = +25 °C, V_{DD} = 1.8 V	-		-	

Table 38. Flash program memory

Symbol	Parameter	Conditions	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	125	°C
N_{WE}	Flash program memory endurance (erase/write cycles)(1)	T_A = 25 °C	1000	-	cycles
t_{RET}	Data retention time	T_A = 25 °C	40	-	years
		T_A = 55 °C	20	-	

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.

Data memory

Table 39. Data memory

Symbol	Parameter	Conditions	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	125	°C
N_{WE}	Data memory endurance (erase/write cycles)(1)	T_A = 25 °C	300 k	-	cycles
		T_A = -40 to 125 °C	100 k(2)	-	
t_{RET}	Data retention time	T_A = 25 °C	40(2)(3)	-	years
		T_A = 55 °C	20(2)(3)	-	

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.
2. More information on the relationship between data retention time and number of write/erase cycles is available in a separate technical document.
3. Retention time for 256B of data memory after up to 1000 cycles at 125 °C.

9.3.6 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error, out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation, LCD levels, etc.).

The test results are given in the following table.

Table 40. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on true open-drain pins (PC0 and PC1)	-5	+0	mA
	Injected current on all five-volt tolerant (FT) pins	-5	+0	
	Injected current on all 3.6 V tolerant (TT) pins	-5	+0	
	Injected current on any other pin	-5	+5	

9.3.7 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 41. I/O static characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	Input voltage on all pins	V_{SS}-0.3	-	0.3 x V_{DD}	V
V_{IH}	Input high level voltage	Input voltage on true open-drain pins (PC0 and PC1) with V_{DD} < 2 V	0.70 x V_{DD}	-	5.2(2)	
		Input voltage on true open-drain pins (PC0 and PC1) with V_{DD} ≥ 2 V		-	5.5(2)	
		Input voltage on five-volt tolerant (FT) pins (PA7 and PE0) with V_{DD} < 2 V	0.70 x V_{DD}	-	5.2(2)	
		Input voltage on five-volt tolerant (FT) pins (PA7 and PE0) with V_{DD} ≥ 2 V		-	5.5(2)	
		Input voltage on 3.6 V tolerant (TT) pins		-	3.6(2)	
		Input voltage on any other pin	0.70 x V_{DD}	-	V_{DD}+0.3(2)	
V_{hys}	Schmitt trigger voltage hysteresis (3)	I/Os	-	200	-	mV
		True open drain I/Os	-	200	-	
I_{lkg}	Input leakage current (4)	$V_{SS} \le V_{IN} \le V_{DD}$ High sink I/Os	-	-	50	nA
		$V_{SS} \le V_{IN} \le V_{DD}$ True open drain I/Os	-	-	200	
		$V_{SS} \le V_{IN} \le V_{DD}$ PA0 with high sink LED driver capability	-	-	200	

Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 42. Output driving current (high sink ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
High sink	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +2 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +2 mA, V_{DD} = 1.8 V	-	0.45	
			I_{IO} = +10 mA, V_{DD} = 3.0 V	-	0.7	
	V_{OH} (2)	Output high level voltage for an I/O pin	I_{IO} = -2 mA, V_{DD} = 3.0 V	V_{DD}-0.45	-	V
			I_{IO} = -1 mA, V_{DD} = 1.8 V	V_{DD}-0.45	-	
			I_{IO} = -10 mA, V_{DD} = 3.0 V	V_{DD}-0.7	-	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

Table 43. Output driving current (true open drain ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Open drain	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +3 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +1 mA, V_{DD} = 1.8 V	-	0.45	

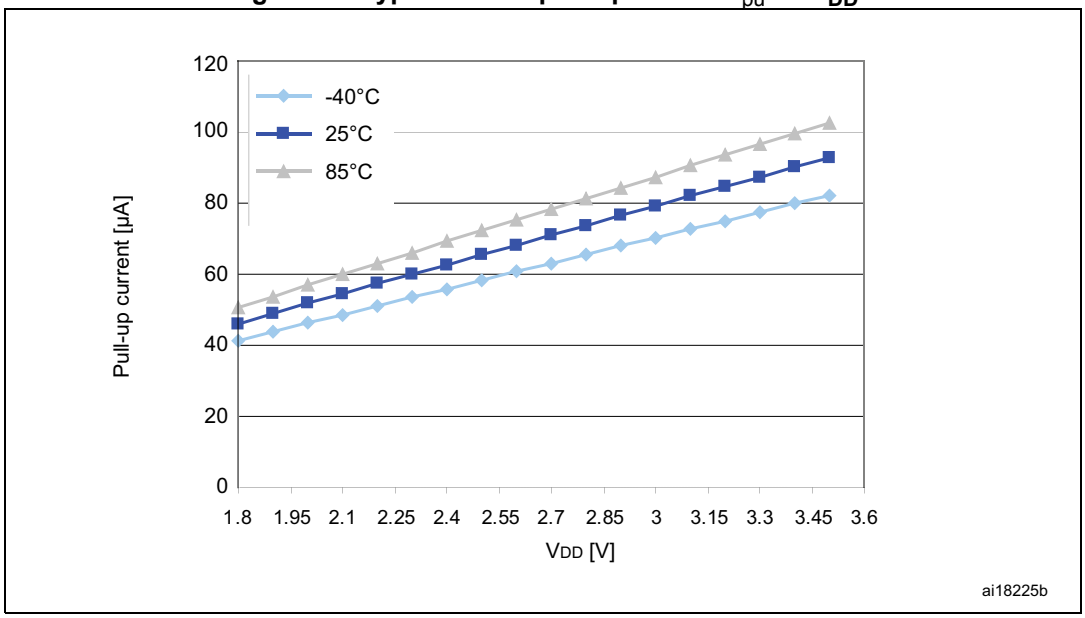
1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Table 44. Output driving current (PA0 with high sink LED driver capability)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
IR	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA, V_{DD} = 2.0 V	-	0.45	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Figure 30. Typical NRST pull-up current I_{pu} vs V_{DD}



The reset network shown in *Figure 31* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 45*. Otherwise the reset is not taken into account internally.

For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, attention must be paid to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. The minimum recommended capacity is 10 nF.

Figure 31. Recommended NRST pin configuration

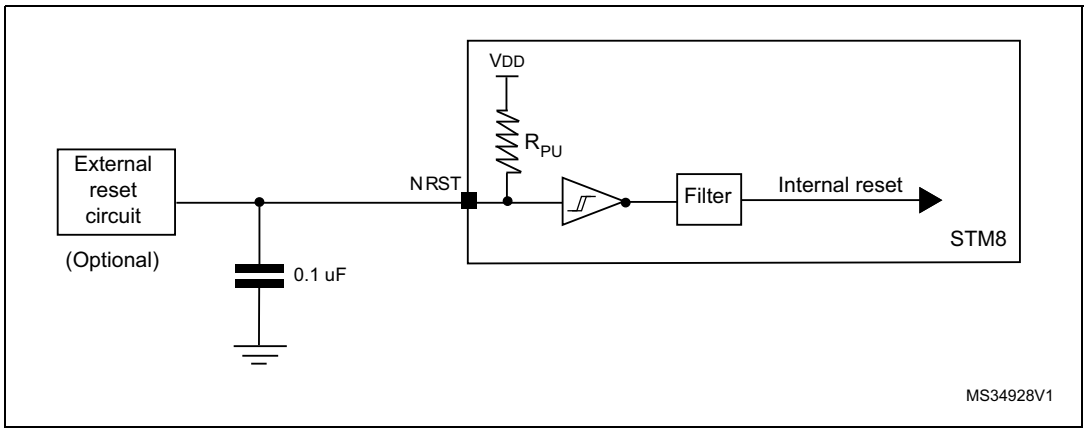


Table 49. Reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max.	Unit
I_{REFINT}	Internal reference voltage consumption	-	-	1.4	-	µA
$T_{S\_VREFINT}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	-	5	10	µs
I_{BUF}(2)	Internal reference voltage buffer consumption (used for ADC)	-	-	13.5	25	µA
$V_{REFINT\ out}$	Reference voltage output	-	1.202 (3)	1.224	1.242 (3)	V
I_{LPBUF}(2)	Internal reference voltage low power buffer consumption (used for comparators or output)	-	-	730	1200	nA
I_{REFOUT}(2)	Buffer output current(4)	-	-	-	1	µA
C_{REFOUT}	Reference voltage output load	-	-	-	50	pF
$t_{VREFINT}$	Internal reference voltage startup time	-	-	2	3	ms
t_{BUFEN}(2)	Internal reference voltage buffer startup time once enabled (1)	-	-	-	10	µs
$ACC_{VREFINT}$	Accuracy of V_{REFINT} stored in the VREFINT_Factory_CONV byte(5)	-	-	-	± 5	mV
$STAB_{VREFINT}$(2)	Stability of V_{REFINT} over temperature	-40 °C ≤ T_A ≤ 125 °C	-	20	50	ppm/°C
	Stability of V_{REFINT} over temperature	0 °C ≤ T_A ≤ 50 °C	-	-	20	
$STAB_{VREFINT}$(2)	Stability of V_{REFINT} after 1000 hours	-	-	-	1000	ppm

1. Defined when ADC output reaches its final value ±1/2LSB
2. Guaranteed by design.
3. Tested in production at V_{DD} = 3 V ±10 mV.
4. To guaranty less than 1% V_{REFOUT} deviation.
5. Measured at V_{DD} = 3 V ±10 mV. This value takes into account V_{DD} accuracy and ADC conversion accuracy.

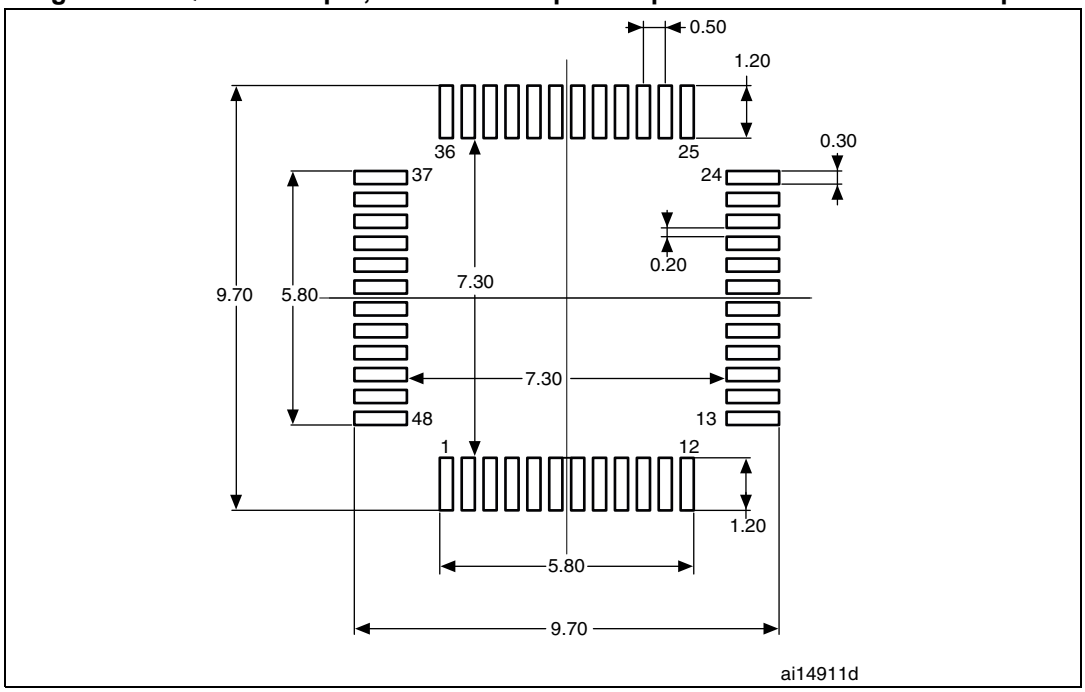
9.3.11 Temperature sensor

In the following table, data are based on characterization results, not tested in production, unless otherwise specified.

Table 50. TS characteristics

Symbol	Parameter	Min	Typ	Max.	Unit
V_{125}(1)	Sensor reference voltage at 125 °C ±5 °C	0.640	0.660	0.680	V
T_L	V_{SENSOR} linearity with temperature	-	±1	±2	°C
Avg_slope	Average slope	1.59(2)	1.62	1.65(2)	mV/°C
$I_{DD(TEMP)}$	Consumption	-	3.4	6(2)	µA

Figure 42. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint

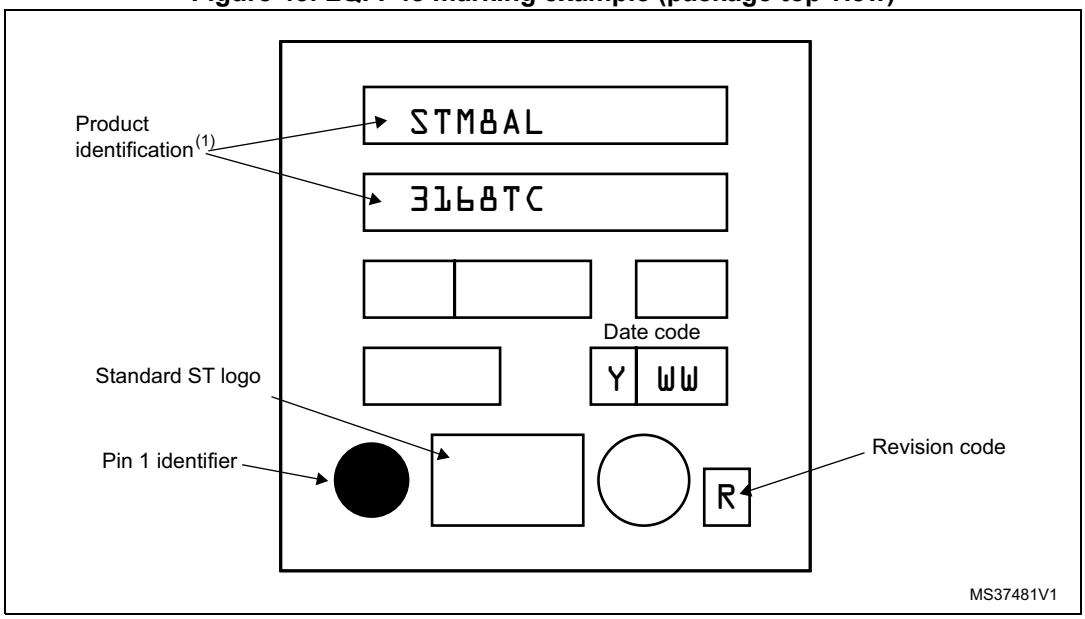


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 43. LQFP48 marking example (package top view)



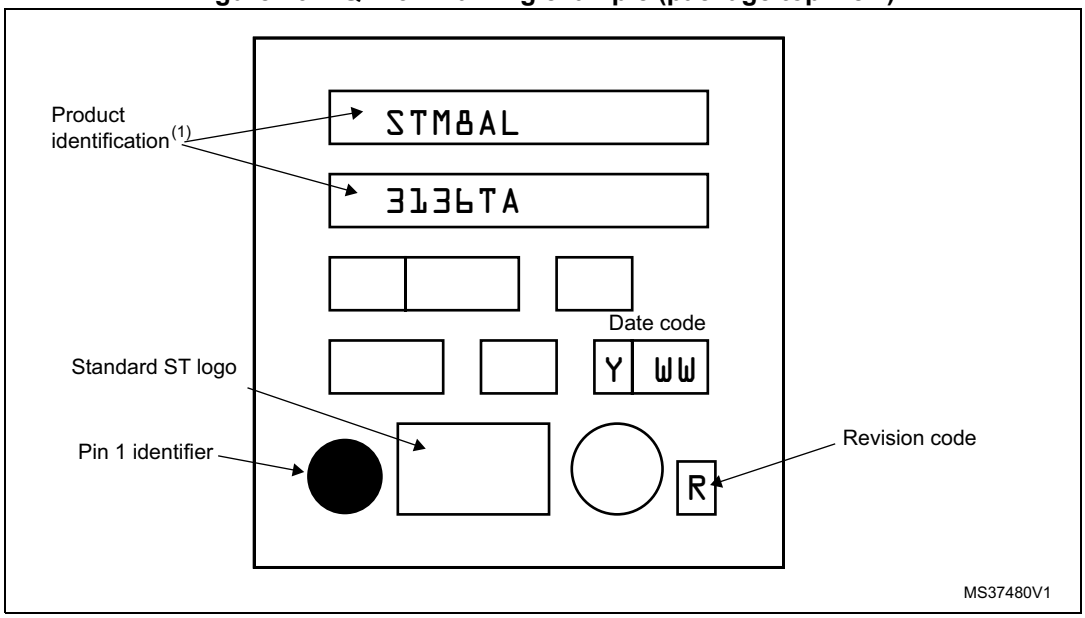
1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

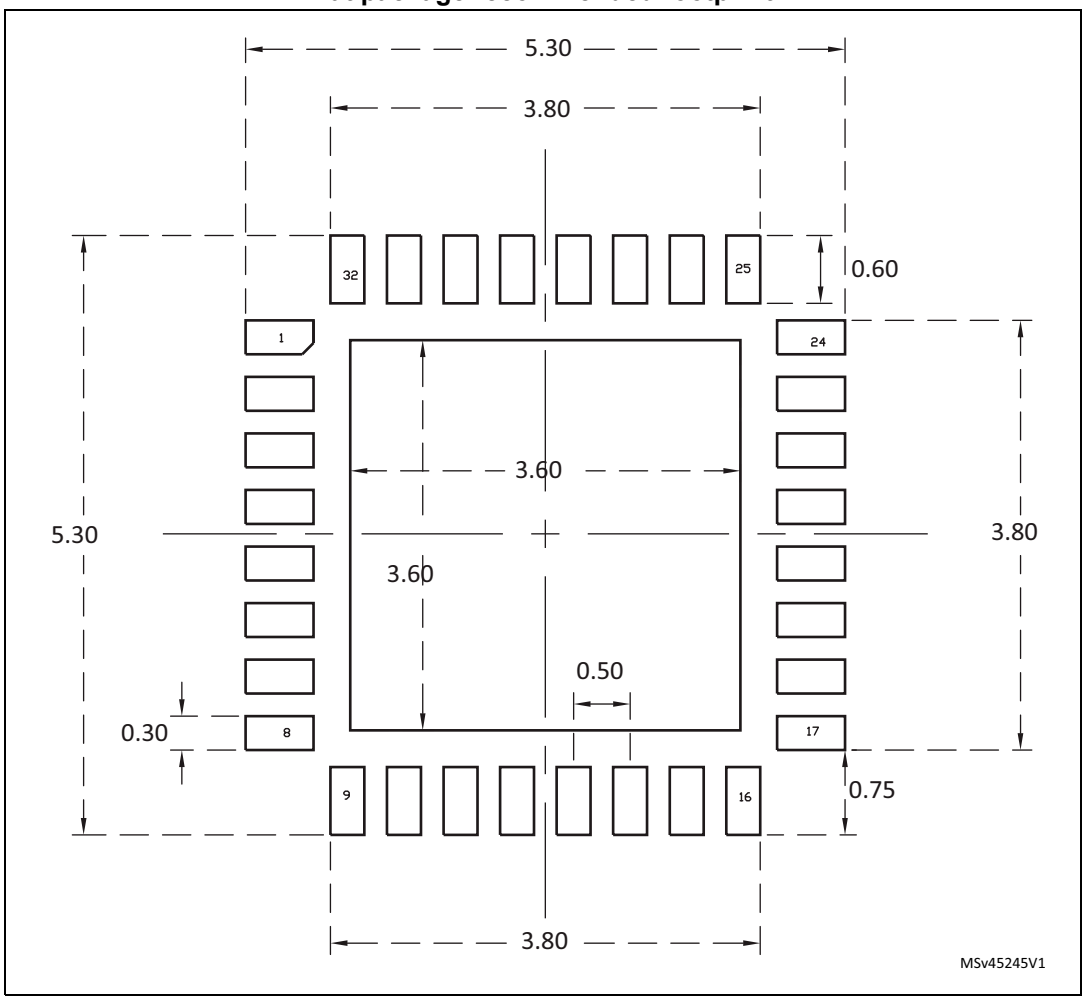
Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 46. LQFP32 marking example (package top view)



1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Figure 48. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



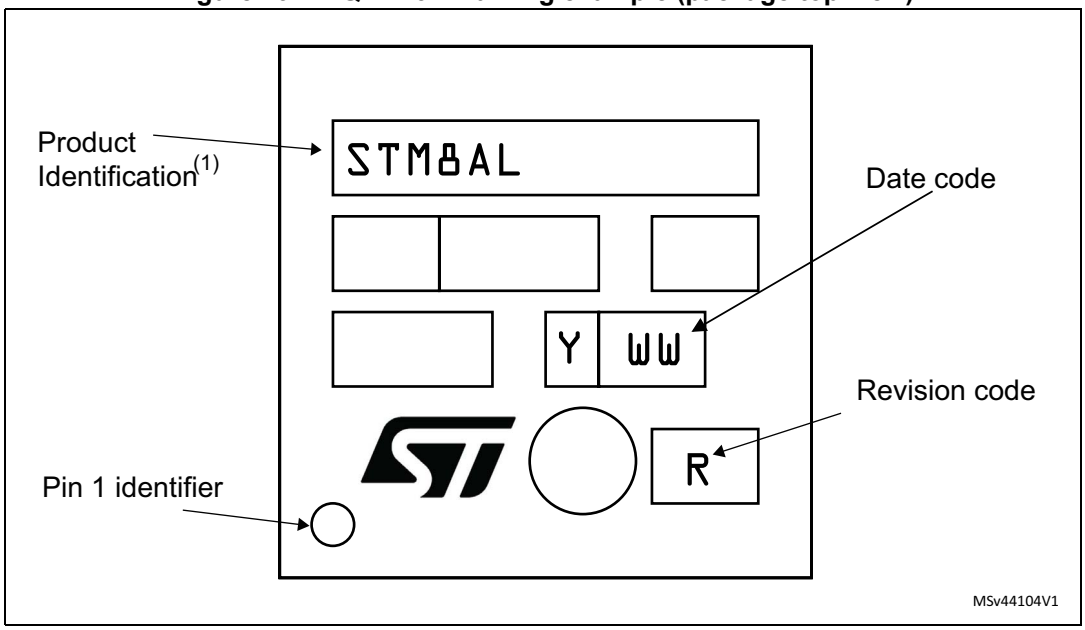
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 49. VFQFPN32 marking example (package top view)



1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.