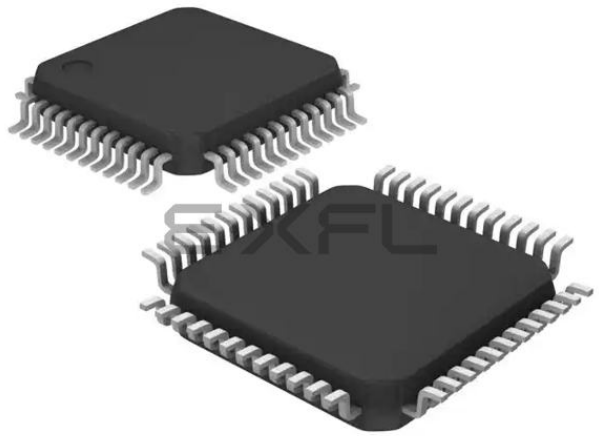

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	41
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 25x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3148tay

2.1 Device overview

Table 2. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x low-power device features and peripheral counts

Features		STM8AL3xx6			STM8AL3xx8		
Flash (Kbyte)		8	16	32	8	16	32
Data EEPROM (Kbyte)		1					
RAM-Kbyte		2			2		
LCD		4x17 (1)			4x28 (1)		
Timers	Basic	1 (8-bit)			1 (8-bit)		
	General purpose	2 (16-bit)			2 (16-bit)		
	Advanced control	1 (16-bit)			1 (16-bit)		
Communication interfaces	SPI	1			1		
	I2C	1			1		
	USART	1			1		
GPIOs		30 (2)(3) or 29 (1)(3)			41(3)		
12-bit synchronized ADC (number of channels)		1 (22 (2) or 21 (1))			1 (25)		
12-Bit DAC (number of channels)		1 (1)			1 (1)		
Comparators COMP1/COMP2		2			2		
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator					
CPU frequency		16 MHz					
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power down)					
Operating temperature		-40 to +85 °C/-40 to +125 °C					
Packages		LQFP32 (7 x7 mm) VFQFPN32 (5 x 5 mm)			LQFP48 (7x7) VFQFPN32 (5 x 5 mm)		

1. STM8AL3Lxx versions only
2. STM8AL31xx versions only
3. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

3.3 Reset and supply management

3.3.1 Power supply scheme

The STM8AL313x/4x/6x and STM8AL3L4x/6x require a 1.65 V to 3.6 V operating supply voltage (V_{DD}). The external power supply pins must be connected as follows:

- V_{SS1}; V_{DD1} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supply for I/Os and for the internal regulator. Provided externally through V_{DD1} pins, the corresponding ground pin is V_{SS1}.
- $V_{SSA;}$ V_{DDA} = 1.8 V to 3.6 V, down to 1.65 V at power down: external power supplies for analog peripherals (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC1 is used). V_{DDA} and V_{SSA} must be connected to V_{DD1} and V_{SS1}, respectively.
- V_{SS2}; V_{DD2} = 1.8 V to 3.6 V, down to 1.65 V at power down: external power supplies for I/Os. V_{DD2} and V_{SS2} must be connected to V_{DD1} and V_{SS1}, respectively.
- V_{REF+}; V_{REF-} (for ADC1): external reference voltage for ADC1. Must be provided externally through V_{REF+} and V_{REF-} pin.
- V_{REF+} (for DAC): external voltage reference for DAC must be provided externally through V_{REF+}.

3.3.2 Power supply supervisor

The STM8AL313x/4x/6x and STM8AL3L4x/6x have an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently (in which case, the V_{DD} min value at power down is 1.65 V).

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains under reset when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

The STM8AL313x/4x/6x and STM8AL3L4x/6x feature an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.13 Timers

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x devices contain one advanced control timer (TIM1), two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

Table 3 compares the features of the advanced control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA1 request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	up/down	Any integer from 1 to 65536	Yes	3 + 1	3
TIM2			Any power of 2 from 1 to 128		2	None
TIM3						
TIM4	8-bit	up	Any power of 2 from 1 to 32768		0	

3.13.1 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down auto reload counter with 16-bit prescaler
- Three independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output.
- One additional capture/compare channel which is not connected to an external I/O
- Synchronization module to control the timer with external signals
- Break input to force timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

3.13.2 16-bit general purpose timers

- 16-bit auto reload (AR) up/down-counter
- 7-bit prescaler adjustable to fixed power of 2 ratios (1…128)
- Two individually configurable capture/compare channels
- PWM mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

3.13.3 8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow or for DAC trigger generation.

3.14 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

3.14.1 Window watchdog timer

The window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

3.14.2 Independent watchdog timer

The independent watchdog peripheral (IWDG) can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

3.15 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

3.16 Communication interfaces

3.16.1 SPI

The serial peripheral interface (SPI1) provides half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s ($f_{SYSCLK}/2$) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

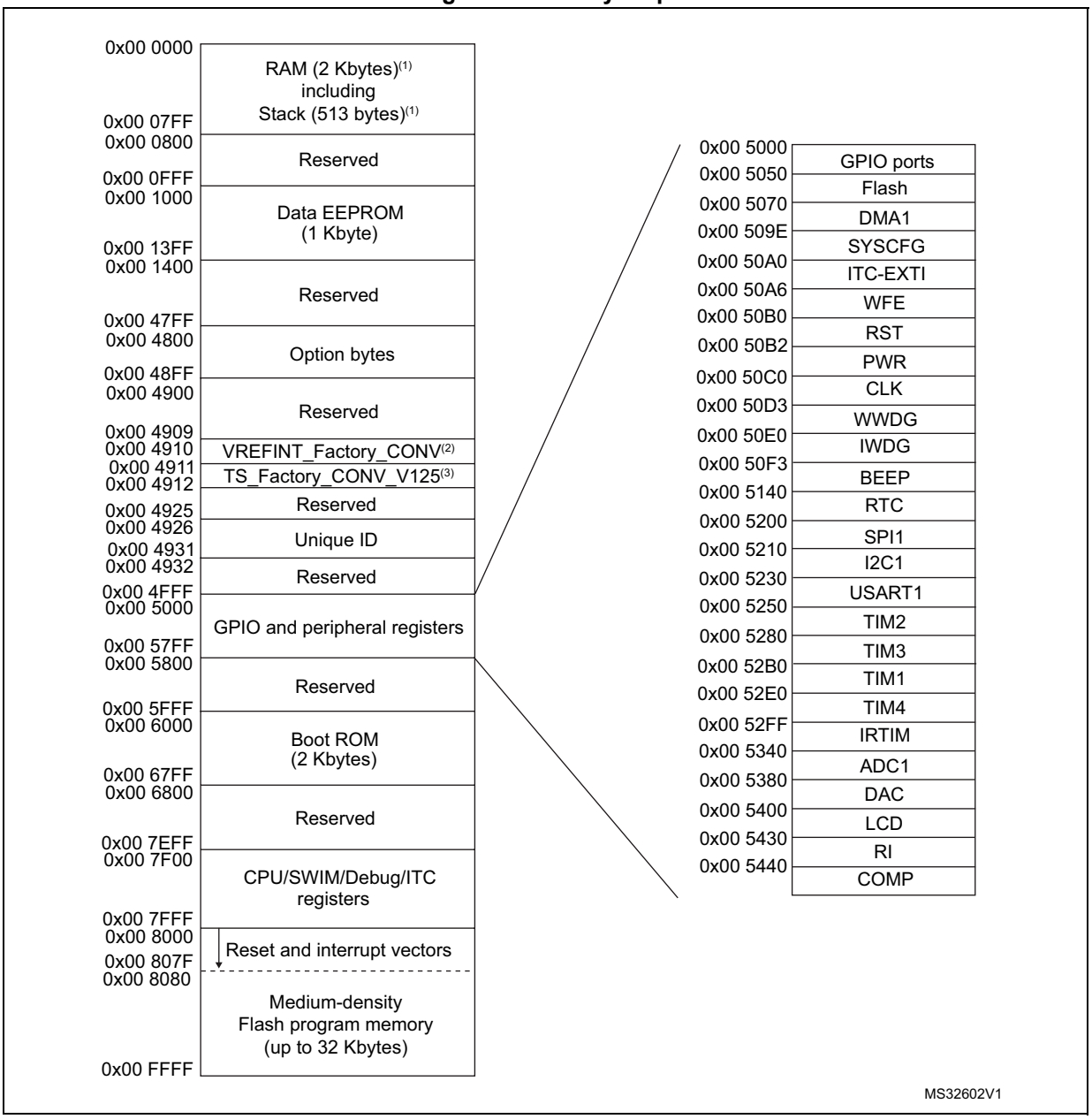
Note: SPI1 can be served by the DMA1 Controller.

5 Memory and register map

5.1 Memory mapping

The memory map is shown in *Figure 9*.

Figure 9. Memory map



1. *Table 6* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. The VREFINT_Factory_CONV byte represents the LSB of the V_{REFINT} 12-bit ADC conversion result. The MSB have a fixed value: 0x6.
3. The TS_Factory_CONV_V125 byte represents the LSB of the V_{125} 12-bit ADC conversion result. The MSB have a fixed value: 0x3. The V_{125} measurement is performed at 125°C.
4. Refer to *Table 9* for an overview of hardware register mapping, to *Table 8* for details on I/O port hardware registers, and to *Table 10* for information on CPU/SWIM/debug module controller registers.

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5230	USART1	USART1_SR	USART1 status register	0xC0
0x00 5231		USART1_DR	USART1 data register	undefined
0x00 5232		USART1_BRR1	USART1 baud rate register 1	0x00
0x00 5233		USART1_BRR2	USART1 baud rate register 2	0x00
0x00 5234		USART1_CR1	USART1 control register 1	0x00
0x00 5235		USART1_CR2	USART1 control register 2	0x00
0x00 5236		USART1_CR3	USART1 control register 3	0x00
0x00 5237		USART1_CR4	USART1 control register 4	0x00
0x00 5238		USART1_CR5	USART1 control register 5	0x00
0x00 5239		USART1_GTR	USART1 guard time register	0x00
0x00 523A		USART1_PSCR	USART1 prescaler register	0x00
0x00 523B to 0x00 524F	Reserved area (21 bytes)			
0x00 5250	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5251		TIM2_CR2	TIM2 control register 2	0x00
0x00 5252		TIM2_SMCR	TIM2 slave mode control register	0x00
0x00 5253		TIM2_ETR	TIM2 external trigger register	0x00
0x00 5254		TIM2_DER	TIM2 DMA1 request enable register	0x00
0x00 5255		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5256		TIM2_SR1	TIM2 status register 1	0x00
0x00 5257		TIM2_SR2	TIM2 status register 2	0x00
0x00 5258		TIM2_EGR	TIM2 event generation register	0x00
0x00 5259		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 525A		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 525B		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 525C		TIM2_CNTRH	TIM2 counter high	0x00
0x00 525D		TIM2_CNTRL	TIM2 counter low	0x00
0x00 525E		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 525F		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 5260		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 5261		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5262		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5263		TIM2_CCR2H	TIM2 capture/compare register 2 high	0x00
0x00 5264		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00

6 Interrupt vector mapping

Table 11. Interrupt mapping

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
-	RESET	Reset	Yes	Yes	Yes	Yes	0x00 8000
-	TRAP	Software interrupt	-	-	-	-	0x00 8004
0	Reserved						0x00 8008
1	FLASH	Flash end of programming/write attempted to protected page interrupt	-	-	Yes	Yes	0x00 800C
2	DMA1 0/1	DMA1 channels 0/1 half transaction/transaction complete interrupt	-	-	Yes	Yes	0x00 8010
3	DMA1 2/3	DMA1 channels 2/3 half transaction/transaction complete interrupt	-	-	Yes	Yes	0x00 8014
4	RTC	RTC alarm A/ wakeup/tamper 1/ tamper 2/tamper 3	Yes	Yes	Yes	Yes	0x00 8018
5	EXTI E/F/ PVD(2)	External interrupt port E/F PVD interrupt	Yes	Yes	Yes	Yes	0x00 801C
6	EXTIB/G	External interrupt port B/G	Yes	Yes	Yes	Yes	0x00 8020
7	EXTID/H	External interrupt port D/H	Yes	Yes	Yes	Yes	0x00 8024
8	EXTI0	External interrupt 0	Yes	Yes	Yes	Yes	0x00 8028
9	EXTI1	External interrupt 1	Yes	Yes	Yes	Yes	0x00 802C
10	EXTI2	External interrupt 2	Yes	Yes	Yes	Yes	0x00 8030
11	EXTI3	External interrupt 3	Yes	Yes	Yes	Yes	0x00 8034
12	EXTI4	External interrupt 4	Yes	Yes	Yes	Yes	0x00 8038
13	EXTI5	External interrupt 5	Yes	Yes	Yes	Yes	0x00 803C
14	EXTI6	External interrupt 6	Yes	Yes	Yes	Yes	0x00 8040
15	EXTI7	External interrupt 7	Yes	Yes	Yes	Yes	0x00 8044
16	LCD	LCD interrupt	-	-	Yes	Yes	0x00 8048
17	CLK/TIM1/ DAC	CLK system clock switch/ CSS interrupt/ TIM1 Break/DAC	-	-	Yes	Yes	0x00 804C

Table 11. Interrupt mapping (continued)

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
18	COMP1/ COMP2/ ADC1	COMP1 interrupt/ COMP2 interrupt ADC1 end of conversion/ analog watchdog/ overrun interrupt	Yes	Yes	Yes	Yes	0x00 8050
19	TIM2	TIM2 update/overflow/ trigger/break interrupt	-	-	Yes	Yes	0x00 8054
20	TIM2	TIM2 capture/compare interrupt	-	-	Yes	Yes	0x00 8058
21	TIM3	TIM3 update /overflow/ trigger/break interrupt	-	-	Yes	Yes	0x00 805C
22	TIM3	TIM3 capture/compare interrupt	-	-	Yes	Yes	0x00 8060
23	TIM1	TIM1 update /overflow/ trigger/COM	-	-	-	Yes	0x00 8064
24	TIM1	TIM1 capture/compare interrupt	-	-	-	Yes	0x00 8068
25	TIM4	TIM4 update /overflow/ trigger interrupt	-	-	Yes	Yes	0x00 806C
26	SPI1	SPI TX buffer empty/RX buffer not empty/error/wakeup interrupt	Yes	Yes	Yes	Yes	0x00 8070
27	USART1	USART1 transmit data register empty/ transmission complete interrupt	-	-	Yes	Yes	0x00 8074
28	USART 1	USART1 received data ready/overrun error/ idle line detected/parity error/global error interrupt	-	-	Yes	Yes	0x00 8078
29	I^2C1	I^2C1 interrupt(3)	Yes	Yes	Yes	Yes	0x00 807C

1. The Low power wait mode is entered when executing a WFE instruction in Low power run mode. In WFE mode, the interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When the interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.
2. The interrupt from PVD is logically OR-ed with Port E and F interrupts. Register EXTI_CONF allows to select between Port E and Port F interrupt (see *External interrupt port select register (EXTI_CONF)* in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).
3. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

Table 16. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by IR_TIM pin (with high sink LED driver capability)	80	
	Output current sunk by any other I/O and control pin	25	
	Output current sourced by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$	Injected current on true open-drain pins (PC0 and PC1)(1)	- 5/+0	
	Injected current on five-volt tolerant (FT) pins (PA7 and PE0)(1)	- 5/+0	
	Injected current on 3.6 V tolerant (TT) pins(1)	- 5/+0	
	Injected current on any other pin(2)	- 5/+5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(3)	± 25	

1. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15* for maximum allowed input voltage values.
2. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15* for maximum allowed input voltage values.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	° C
T_J	Maximum junction temperature	150	

Table 18. Operating lifetime (OLF)(1)

Symbol	Ratings	Value	Unit
OLF	Conforming to AEC-Q100	-40 to 125 °C	Grade 1

1. For detailed mission profile analysis, please contact the local ST Sales Office.

Table 24. Total current consumption in low-power wait mode at V_{DD} = 1.65 V to 3.6 V

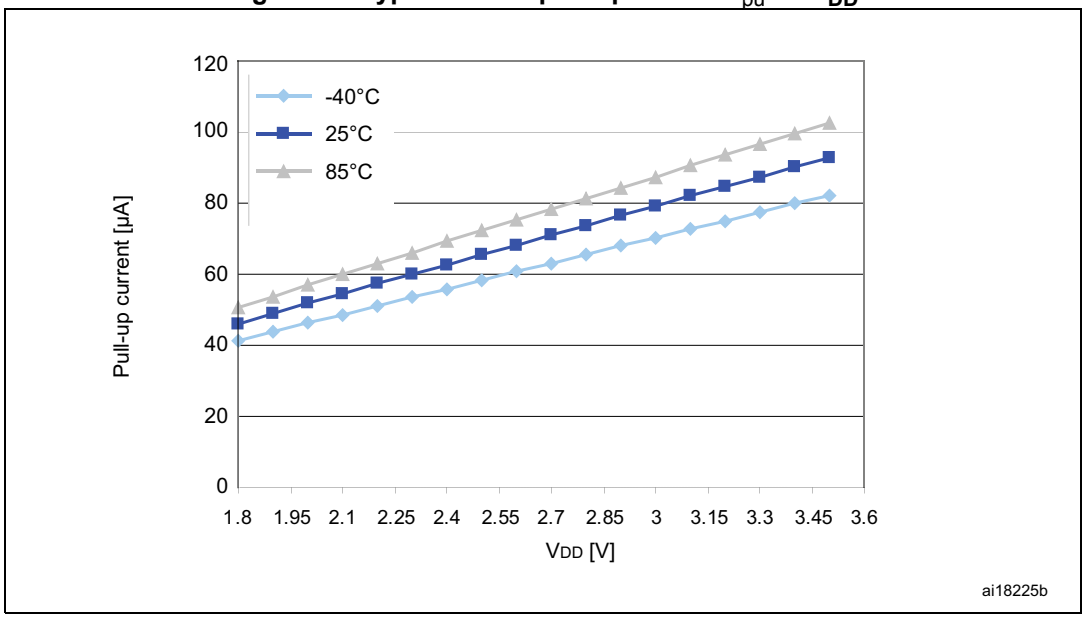
Symbol	Parameter	Conditions(1)			Typ	Max	Unit
$I_{DD(LPW)}$	Supply current in Low power wait mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	3.00	3.30(2)	µA
				T_A = 85 °C	4.40	9(3)	
				T_A = 125 °C	11.00	18(3)	
		LSE external clock(4) (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	2.35	2.70(2)	
				T_A = 85 °C	3.10	3.70(2)	
				T_A = 125 °C	7.20	11.00(2)	

1. No floating I/Os.
2. Guaranteed by characterization results.
3. Tested at 85°C for temperature range A or 125°C for temperature range C.
4. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 33*.

Table 25. Total current consumption and timing in active-halt mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions (1)			Typ	Max(2)	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSI RC (at 38 kHz)	LCD OFF(3)	T_A = -40 °C to 25 °C	0.90	2.10	µA
				T_A = 85 °C	1.50	3.40	
				T_A = 125 °C	5.10	12.00	
			LCD ON (static duty/ external V_{LCD}) (4)	T_A = -40 °C to 25 °C	1.40	3.10	
				T_A = 85 °C	1.90	4.30	
				T_A = 125 °C	5.50	13.00	
			LCD ON (1/4 duty/ external V_{LCD}) (5)	T_A = -40 °C to 25 °C	1.90	4.30	
				T_A = 85 °C	2.40	5.40	
				T_A = 125 °C	6.00	15.00	
			LCD ON (1/4 duty/ internal V_{LCD}) (6)	T_A = -40 °C to 25 °C	3.90	8.75	
				T_A = 85 °C	4.50	10.20	
				T_A = 125 °C	6.80	16.30	

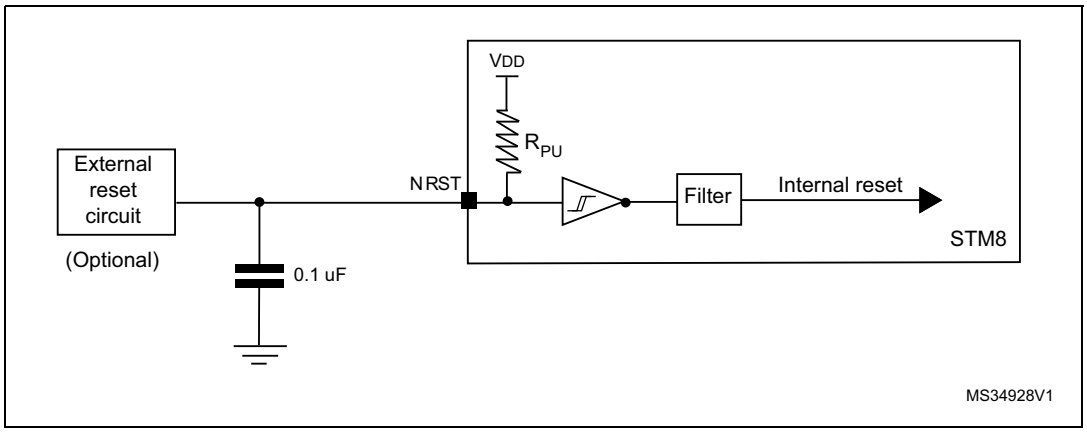
Figure 30. Typical NRST pull-up current I_{pu} vs V_{DD}



The reset network shown in *Figure 31* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 45*. Otherwise the reset is not taken into account internally.

For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, attention must be paid to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. The minimum recommended capacity is 10 nF.

Figure 31. Recommended NRST pin configuration



9.3.8 Communication interfaces

SPI1 - Serial peripheral interface

Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under ambient temperature, f_{SYSCLK} frequency and V_{DD} supply voltage conditions summarized in *Section 9.3.1*. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 46. SPI1 characteristics

Symbol	Parameter	Conditions(1)	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI1 clock frequency	Master mode	0	8	MHz
		Slave mode	0	8	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI1 clock rise and fall time	Capacitive load: C = 30 pF	-	30	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 x $1/f_{SYSCLK}$	-	
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	80	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{MASTER} = 8 MHz, f_{SCK}= 4 MHz	105	145	
$t_{su(MI)}$(2) $t_{su(SI)}$(2)	Data input setup time	Master mode	30	-	
		Slave mode	3	-	
$t_{h(MI)}$(2) $t_{h(SI)}$(2)	Data input hold time	Master mode	15	-	
		Slave mode	0	-	
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode	-	3x $1/f_{SYSCLK}$	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	30	-	
$t_{v(SO)}$(2)	Data output valid time	Slave mode (after enable edge)	-	60	
$t_{v(MO)}$(2)	Data output valid time	Master mode (after enable edge)	-	20	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$(2)		Master mode (after enable edge)	1	-	

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and max time is for the maximum time to put the data in Hi-Z.

Table 56. ADC1 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	2.4 V ≤ V_{DDA} ≤ 3.6 V	2.4	-	V_{DDA}	V
		1.8 V ≤ V_{DDA} ≤ 2.4 V	V_{DDA}			
V_{REF-}	Lower reference voltage	-	V_{SSA}			
I_{VDDA}	Current on the V_{DDA} input pin	-	-	1000	1450	µA
I_{VREF+}	Current on the V_{REF+} input pin	-	-	400	700 (peak)(1)	
		-	-		450 (average)(1)	
V_{AIN}	Conversion voltage range	-	0(2)	-	V_{REF+}	-
T_A	Temperature range	-	-40	-	125	°C
R_{AIN}	External resistance on V_{AIN}	on PF0 fast channel	-	-	50(3)	kΩ
		on all other channels	-	-		
C_{ADC}	Internal sample and hold capacitor	on PF0 fast channel	-	16	-	pF
		on all other channels	-		-	
f_{ADC}	ADC sampling clock frequency	2.4 V ≤ V_{DDA} ≤ 3.6 V without zooming	0.320	-	16	MHz
		1.8 V ≤ V_{DDA} ≤ 2.4 V with zooming	0.320	-	8	
f_{CONV}	12-bit conversion rate	V_{AIN} on PF0 fast channel	-	-	1(4)(5)	
		V_{AIN} on all other channels	-	-	760(4)(5)	kHz
f_{TRIG}	External trigger frequency	-	-	-	t_{conv}	$1/f_{ADC}$
t_{LAT}	External trigger latency	-	-	-	3.5	$1/f_{SYSCLK}$

In the following three tables, data are guaranteed by characterization result, not tested in production.

Table 57. ADC1 accuracy with V_{DDA} = 2.5 V to 3.3 V

Symbol	Parameter	Conditions	Typ.	Max(1)	Unit
DNL	Differential non linearity	f_{ADC} = 16 MHz	1	1.6	LSB
		f_{ADC} = 8 MHz	1	1.6	
		f_{ADC} = 4 MHz	1	1.5	
INL	Integral non linearity	f_{ADC} = 16 MHz	1.2	2	
		f_{ADC} = 8 MHz	1.2	1.8	
		f_{ADC} = 4 MHz	1.2	1.7	
TUE	Total unadjusted error	f_{ADC} = 16 MHz	2.2	3.0	
		f_{ADC} = 8 MHz	1.8	2.5	
		f_{ADC} = 4 MHz	1.8	2.3	
Offset	Offset error	f_{ADC} = 16 MHz	1.5	2	LSB
		f_{ADC} = 8 MHz	1	1.5	
		f_{ADC} = 4 MHz	0.7	1.2	
Gain	Gain error	f_{ADC} = 16 MHz	1	1.5	
		f_{ADC} = 8 MHz			
		f_{ADC} = 4 MHz			

1. Not tested in production.

Table 58. ADC1 accuracy with V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Typ.	Max(1)	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	1.7	3	
TUE	Total unadjusted error	2	4	
Offset	Offset error	1	2	
Gain	Gain error	1.5	3	

1. Not tested in production.

10.5 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 19: General operating conditions*.

The maximum chip-junction temperature, T_{Jmax}, in degree Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma(V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,

  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

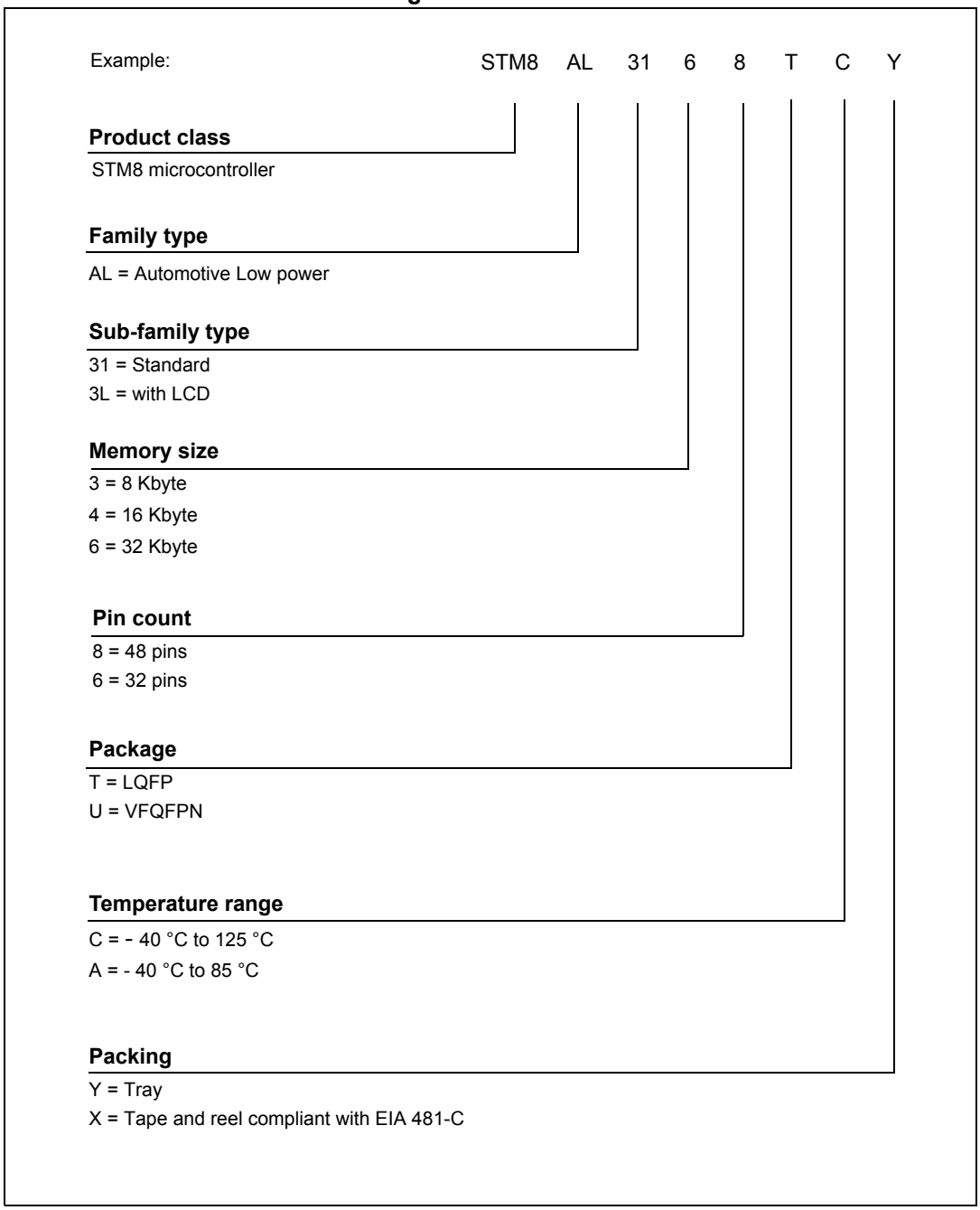
Table 68. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP48- 7 x 7 mm	65	°C/W
	Thermal resistance junction-ambient LQFP32 - 7 x 7 mm	59	
	Thermal resistance junction-ambient VFQFPN32 - 5 x 5 mm	62	

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

11 Device ordering information

Figure 50. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x ordering information scheme



1. For a list of available options (e.g. memory size, package) and order-able part numbers or for further information on any aspect of this device, please contact the nearest ST sales office.

12 Revision history

Table 69. Document revision history

Date	Revision	Changes
04-Jan-2012	1	Initial release
20-Dec-2012	2	Added consumption values when run from Flash or from RAM. Added 8k Flash devices STM8AL3138 and STM8AL3136 to *Table 1: Device summary*, *Table 2: Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x low-power device features and peripheral counts*. and *Figure 50: Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x ordering information scheme*. Added footnotes stating that power consumption has not been tested to *Table 21* and *Table 22* for HSE, and to *Table 23* and *Table 24* for LSE. Updated max LSI amperage values in *Table 23* and *Table 24*. Replaced *Table 38: Flash program memory* and *Table 39: Data memory*. Added a production test footnote to *Table 50: TS characteristics*. Updated voltage values in *Table 50: TS characteristics*, and current values in *Table 51: Comparator 1 characteristics* and *Table 52: Comparator 2 characteristics*. Removed *Figure 13: Typ. $I_{DD(LPR)}$ vs. V_{DD} (LSI clock source)* and *Figure 14: Typ. $I_{DD(LPW)}$ vs. V_{DD} (LSI clock source)*.
03-Jun-2013	3	Updated ‘Qualification conforms’ bullet on cover page. Updated ‘TS_Factory_CONV’ in *Figure 9: Memory map* Removed ‘rev G’ in *Table 18: Operating lifetime (OLF)* Ratings Replaced 0.40 by 0.38 in *Table 22: Total current consumption in Wait mode* ‘code executed from Flash’ fcpu = 125 kHz Updated footnote (3) in *Table 23: Total current consumption and timing in low-power run mode at VDD = 1.65 V to 3.6 V*, *Table 24: Total current consumption in low-power wait mode at VDD = 1.65 V to 3.6 V* and *Table 27: Total current consumption and timing in Halt mode at VDD = 1.65 to 3.6 V* Updated footnote (2) in *Table 26: Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal* Updated max ILEAK_HSE in *Table 30: HSE external clock characteristics* and *Table 31: LSE external clock characteristics* Updated ACC_{HSI} in *Table 34: HSI oscillator characteristics* Updated tprog max *Table 38: Flash program memory* Updated $STAB_{VREFINT}$ in *Table 49: Reference voltage characteristics* Updated ‘TS_Factory_CONV’ in *Table 50: TS characteristics* footnote. Updated ‘tconv’ and ‘title’ in *Table 56: ADC1 characteristics* Updated title in *Table 57: ADC1 accuracy with VDDA = 2.5 V to 3.3 V* Updated *Table 64: Electrical sensitivities*
14-Jun-2013	4	Updated max LSI measures in *Table 23: Total current consumption and timing in low-power run mode at VDD = 1.65 V to 3.6 V* and *Table 24: Total current consumption in low-power wait mode at VDD = 1.65 V to 3.6 V*

Table 69. Document revision history (continued)

Date	Revision	Changes
03-Mar-2014	5	Changed the document status to Datasheet - Production data to reflect the device maturity. Corrected the data memory size in the *Features*. Updated the package assignment in *Table 2: Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x low-power device features and peripheral counts*
13-May-2015	6	Updated: – the product names in the document headers and on the cover page, – *Section 1: Introduction*, – the captions of *Figure 3: STM8AL31x8T 48-pin pinout (without LCD)*, *Figure 4: STM8AL3Lx8T 48-pin pinout (with LCD)*, *Figure 5: STM8AL31x6T 32-pin pinout (without LCD)*, *Figure 6: STM8AL3Lx6T 32-pin pinout (with LCD)*, – *Table 6: Flash and RAM boundary addresses*, – I_{LEAK_HSE} maximum value in *Table 32: HSE oscillator characteristics*,I_{LEAK_LSE} maximum value in *Table 33: LSE oscillator characteristics*, – *Table 54*, *Table 57*, *Table 58*, *Table 59* with a footnote for Max values not tested in production, – *Section 9.3.15: EMC characteristics*, – *Section 10.2: LQFP48 package information*, – *Section 10.3: LQFP32 package information*, – *Figure 50: Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x ordering information scheme*. Added: – *Figure 43: LQFP48 marking example (package top view)*, – *Figure 46: LQFP32 marking example (package top view)*. Moved *Section 10.5: Thermal characteristics* to *Section 10: Package information*.