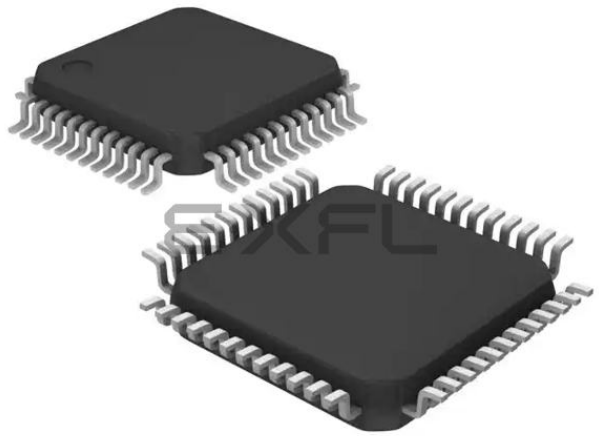

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	41
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 25x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3148tcy

- Development support
  - Fast on-chip programming and non intrusive debugging with SWIM
  - Bootloader using USART
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM8AL313x/4x/6x (without LCD)	STM8AL3136, STM8AL3138, STM8AL3146, STM8AL3148, STM8AL3166, STM8AL3168
STM8AL3L4x/6x (with LCD)	STM8AL3L46, STM8AL3L48, STM8AL3L66, STM8AL3L68

Contents

2.1 Device overview

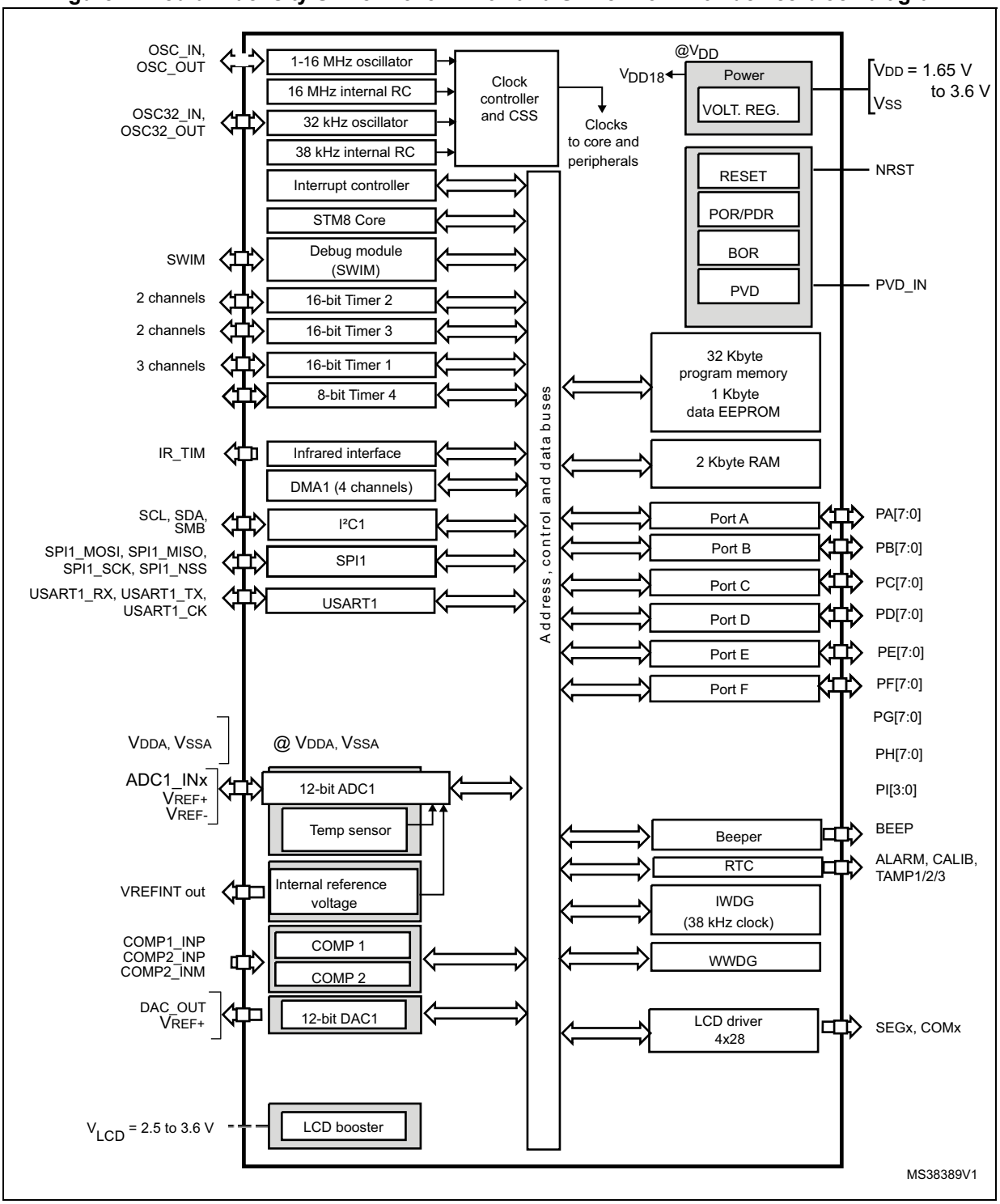
Table 2. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x low-power device features and peripheral counts

Features		STM8AL3xx6			STM8AL3xx8		
Flash (Kbyte)		8	16	32	8	16	32
Data EEPROM (Kbyte)		1					
RAM-Kbyte		2			2		
LCD		4x17 (1)			4x28 (1)		
Timers	Basic	1 (8-bit)			1 (8-bit)		
	General purpose	2 (16-bit)			2 (16-bit)		
	Advanced control	1 (16-bit)			1 (16-bit)		
Communication interfaces	SPI	1			1		
	I2C	1			1		
	USART	1			1		
GPIOs		30 (2)(3) or 29 (1)(3)			41(3)		
12-bit synchronized ADC (number of channels)		1 (22 (2) or 21 (1))			1 (25)		
12-Bit DAC (number of channels)		1 (1)			1 (1)		
Comparators COMP1/COMP2		2			2		
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator					
CPU frequency		16 MHz					
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power down)					
Operating temperature		-40 to +85 °C/-40 to +125 °C					
Packages		LQFP32 (7 x7 mm) VFQFPN32 (5 x 5 mm)			LQFP48 (7x7) VFQFPN32 (5 x 5 mm)		

1. STM8AL3Lxx versions only
2. STM8AL31xx versions only
3. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

3 Functional overview

Figure 1. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x device block diagram



1. **Legend**: ADC (Analog-to-digital converter), BOR (Brownout reset), DMA (Direct memory access), DAC (Digital-to-analog converter), I²C (Inter-integrated circuit multimaster interface), IWDG (Independent watchdog), LCD (Liquid crystal display), POR/PDR (Power on reset / power down reset), RTC (Real-time clock), SPI (Serial peripheral interface), SWIM (Single wire interface module), USART (Universal synchronous asynchronous receiver transmitter), WWDG (Window watchdog).

Table 5. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48	VFQFPN32	LQFP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
38	26	26	PC1(5)/I2C1_SCL	I/O	FT	X	-	X	-	T(7)		Port C1	I2C1 clock
41	27	27	PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ COMP1_INP/VREFINT	I/O	TT(3)	X	X	X	HS	X	X	Port C2	USART1 receive / LCD segment 22 / ADC1_IN6 / Comparator 1 positive input / Internal voltage reference output
42	28	28	PC3/USART1_TX/ LCD_SEG23(2)/ ADC1_IN5/COMP1_INP/ COMP2_INM	I/O	TT(3)	X	X	X	HS	X	X	Port C3	USART1 transmit / LCD segment 23 / ADC1_IN5 / Comparator 1 positive input / Comparator 2 negative input
43	29	29	PC4/USART1_CK/ I2C1_SMB/CCO/ LCD_SEG24(2)/ ADC1_IN4/COMP2_INM/ COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port C4	USART1 synchronous clock / I2C1_SMB / Configurable clock output / LCD segment 24 / ADC1_IN4 / Comparator 2 negative input / Comparator 1 positive input
44	30	30	PC5/OSC32_IN /*[SPI1_NSS]*(4)/ *[USART1_TX]*(4)	I/O	-	X	X	X	HS	X	X	Port C5	LSE oscillator input / *[SPI1 master/slave select] / [USART1 transmit]*
45	31	31	PC6/OSC32_OUT/ *[SPI1_SCK]*(4)/ *[USART1_RX]*(4)	I/O	-	X	X	X	HS	X	X	Port C6	LSE oscillator output / *[SPI1 clock] / [USART1 receive]*
46	-	-	PC7/LCD_SEG25(2)/ ADC1_IN3/COMP2_INM/ COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port C7	LCD segment 25 /ADC1_IN3/ Comparator negative input / Comparator 1 positive input

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 508C	DMA1	DMA1_C2PARH	DMA1 peripheral address high register (channel 2)	0x52
0x00 508D		DMA1_C2PARL	DMA1 peripheral address low register (channel 2)	0x00
0x00 508E		Reserved area (1 byte)		
0x00 508F		DMA1_C2M0ARH	DMA1 memory 0 address high register (channel 2)	0x00
0x00 5090		DMA1_C2M0ARL	DMA1 memory 0 address low register (channel 2)	0x00
0x00 5091 0x00 5092		Reserved area (2 bytes)		
0x00 5093		DMA1_C3CR	DMA1 channel 3 configuration register	0x00
0x00 5094		DMA1_C3SPR	DMA1 channel 3 status & priority register	0x00
0x00 5095		DMA1_C3NDTR	DMA1 number of data to transfer register (channel 3)	0x00
0x00 5096		DMA1_C3PARH_ C3M1ARH	DMA1 peripheral address high register (channel 3)	0x40
0x00 5097		DMA1_C3PARL_ C3M1ARL	DMA1 peripheral address low register (channel 3)	0x00
0x00 5098		Reserved area (1 byte)		
0x00 5099		DMA1_C3M0ARH	DMA1 memory 0 address high register (channel 3)	0x00
0x00 509A		DMA1_C3M0ARL	DMA1 memory 0 address low register (channel 3)	0x00
0x00 509B to 0x00 509D		Reserved area (3 bytes)		
0x00 509E	SYSCFG	SYSCFG_RMPCR1	Remapping register 1	0x00
0x00 509F		SYSCFG_RMPCR2	Remapping register 2	0x00
0x00 50A0	ITC - EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF1	External interrupt port select register 1	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8		WFE_CR3	WFE control register 3	0x00

8 Unique ID

The devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single bytes and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Table 14. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4926	X co-ordinate on the wafer	U_ID[7:0]							
0x4927		U_ID[15:8]							
0x4928	Y co-ordinate on the wafer	U_ID[23:16]							
0x4929		U_ID[31:24]							
0x492A	Wafer number	U_ID[39:32]							
0x492B	Lot number	U_ID[47:40]							
0x492C		U_ID[55:48]							
0x492D		U_ID[63:56]							
0x492E		U_ID[71:64]							
0x492F		U_ID[79:72]							
0x4930		U_ID[87:80]							
0x4931		U_ID[95:88]							

Table 24. Total current consumption in low-power wait mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions(1)			Typ	Max	Unit
$I_{DD(LPW)}$	Supply current in Low power wait mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	3.00	3.30(2)	µA
				T_A = 85 °C	4.40	9(3)	
				T_A = 125 °C	11.00	18(3)	
		LSE external clock(4) (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	2.35	2.70(2)	
				T_A = 85 °C	3.10	3.70(2)	
				T_A = 125 °C	7.20	11.00(2)	

1. No floating I/Os.
2. Guaranteed by characterization results.
3. Tested at 85°C for temperature range A or 125°C for temperature range C.
4. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 33*.

Table 25. Total current consumption and timing in active-halt mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions (1)			Typ	Max(2)	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSI RC (at 38 kHz)	LCD OFF(3)	T_A = -40 °C to 25 °C	0.90	2.10	µA
				T_A = 85 °C	1.50	3.40	
				T_A = 125 °C	5.10	12.00	
			LCD ON (static duty/ external V_{LCD}) (4)	T_A = -40 °C to 25 °C	1.40	3.10	
				T_A = 85 °C	1.90	4.30	
				T_A = 125 °C	5.50	13.00	
			LCD ON (1/4 duty/ external V_{LCD}) (5)	T_A = -40 °C to 25 °C	1.90	4.30	
				T_A = 85 °C	2.40	5.40	
				T_A = 125 °C	6.00	15.00	
			LCD ON (1/4 duty/ internal V_{LCD}) (6)	T_A = -40 °C to 25 °C	3.90	8.75	
				T_A = 85 °C	4.50	10.20	
				T_A = 125 °C	6.80	16.30	

Current consumption of on-chip peripherals

Table 28. Peripheral current consumption

Symbol	Parameter		Typ. V_{DD} = 3.0 V	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)		13	µA/MHz
$I_{DD(TIM2)}$	TIM2 supply current (1)		8	
$I_{DD(TIM3)}$	TIM3 supply current (1)		8	
$I_{DD(TIM4)}$	TIM4 timer supply current (1)		3	
$I_{DD(USART1)}$	USART1 supply current (2)		6	
$I_{DD(SPI1)}$	SPI1 supply current (2)		3	
$I_{DD(I2C1)}$	I^2C1 supply current (2)		5	
$I_{DD(DMA1)}$	DMA1 supply current(2)		3	
$I_{DD(WWDG)}$	WWDG supply current(2)		2	
$I_{DD(ALL)}$	Peripherals ON(3)		44	
$I_{DD(ADC1)}$	ADC1 supply current(4)		1500	µA
$I_{DD(DAC)}$	DAC supply current(5)		370	
$I_{DD(COMP1)}$	Comparator 1 supply current(6)		0.160	
$I_{DD(COMP2)}$	Comparator 2 supply current(6)	Slow mode	2	
		Fast mode	5	
$I_{DD(PVD/BOR)}$	Power voltage detector and brownout Reset unit supply current (7)		2.6	
$I_{DD(BOR)}$	Brownout Reset unit supply current (7)		2.4	
$I_{DD(IDWDG)}$	Independent watchdog supply current	including LSI supply current	0.45	
		excluding LSI supply current	0.05	

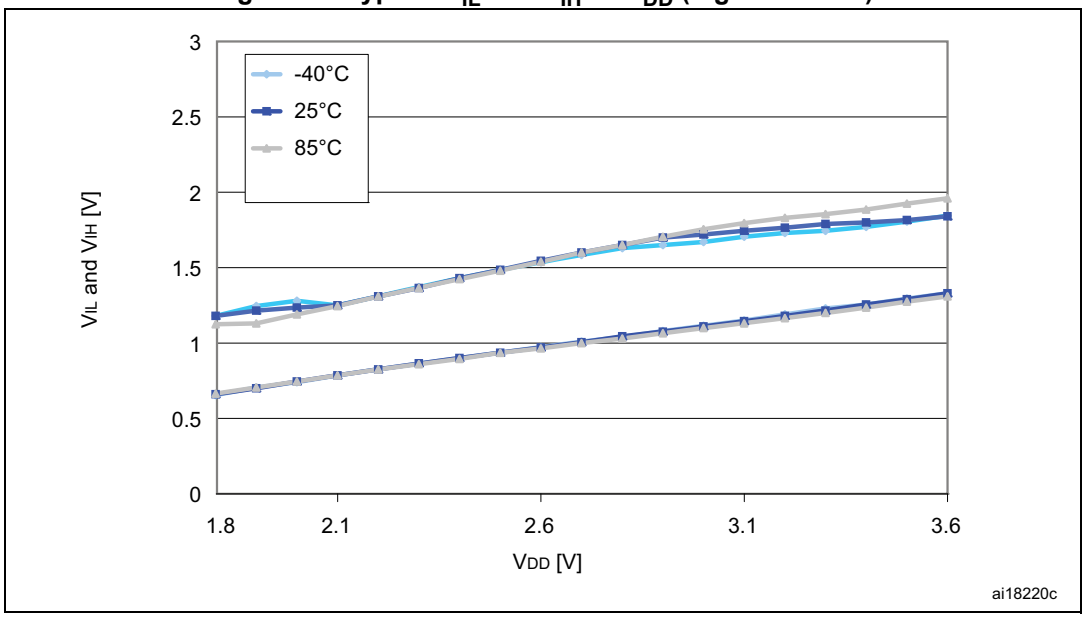
1. Data based on a differential I_{DD} measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
3. Peripherals listed above the $I_{DD(ALL)}$ parameter ON: TIM1, TIM2, TIM3, TIM4, USART1, SPI1, I2C1, DMA1, WWDG.
4. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion.
5. Data based on a differential I_{DD} measurement between DAC in reset configuration and continuous DAC conversion of V_{DD} /2. Floating DAC output.
6. Data based on a differential I_{DD} measurement between COMP1 or COMP2 in reset configuration and COMP1 or COMP2 enabled with static inputs. Supply current of internal reference voltage excluded.
7. Including supply current of internal reference voltage.

Table 41. I/O static characteristics (continued)

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	30(6)	45	60(6)	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. If V_{IH} maximum cannot be respected, the injection current must be limited externally to $I_{INJ(PIN)}$ maximum.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 22*).
6. Data not tested in production.

Figure 19. Typical V_{IL} and V_{IH} vs V_{DD} (high sink I/Os)



Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 42. Output driving current (high sink ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
High sink	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +2 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +2 mA, V_{DD} = 1.8 V	-	0.45	
			I_{IO} = +10 mA, V_{DD} = 3.0 V	-	0.7	
	V_{OH} (2)	Output high level voltage for an I/O pin	I_{IO} = -2 mA, V_{DD} = 3.0 V	V_{DD}-0.45	-	V
			I_{IO} = -1 mA, V_{DD} = 1.8 V	V_{DD}-0.45	-	
			I_{IO} = -10 mA, V_{DD} = 3.0 V	V_{DD}-0.7	-	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

Table 43. Output driving current (true open drain ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Open drain	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +3 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +1 mA, V_{DD} = 1.8 V	-	0.45	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Table 44. Output driving current (PA0 with high sink LED driver capability)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
IR	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA, V_{DD} = 2.0 V	-	0.45	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Figure 32. SPI1 timing diagram - slave mode and CPHA=0

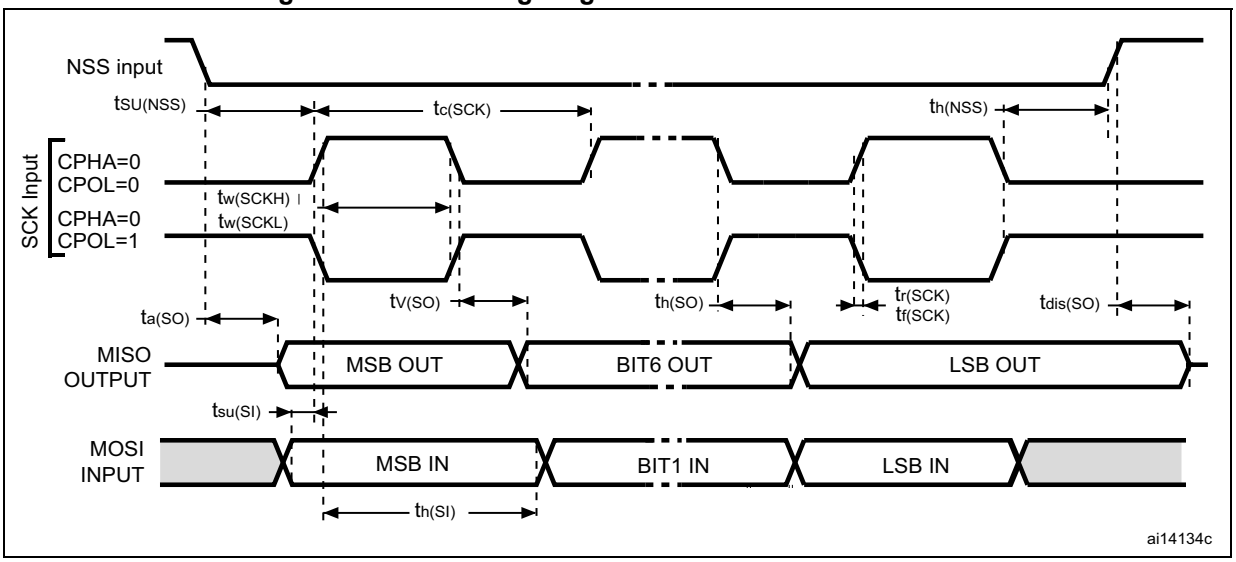
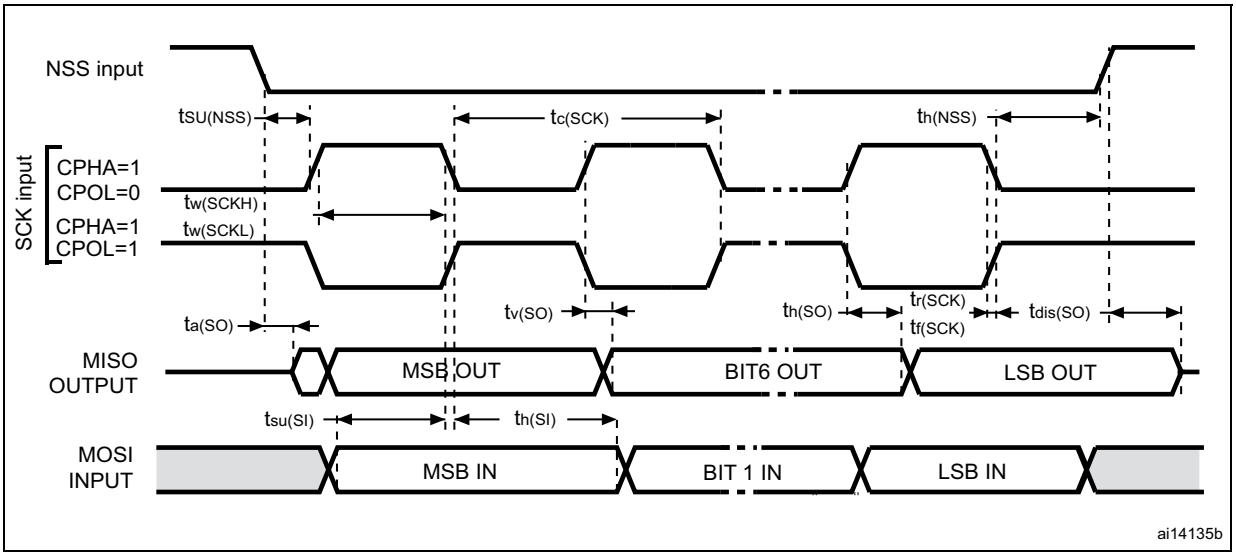


Figure 33. SPI1 timing diagram - slave mode and CPHA=1(1)



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

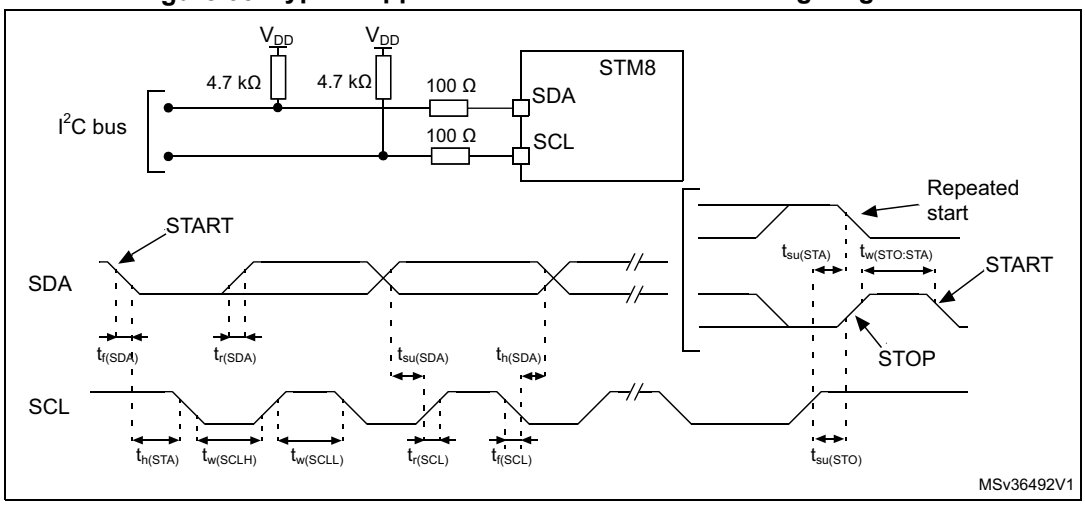
Table 47. I²C characteristics (continued)

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max (2)	Min (2)	Max (2)	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0		0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{SYSCLK} must be at least equal to 8 MHz to achieve max fast I²C speed (400 kHz).
2. Data based on standard I²C protocol requirements, not tested in production.

Note: For speeds around 200 kHz, the achieved speed can have a ± 5% tolerance
For other speed ranges, the achieved speed can have a ± 2% tolerance
The above variations depend on the accuracy of the external components used.

Figure 35. Typical application with I²C bus and timing diagram(1)



1. Measurement points are done at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}

9.3.9 LCD controller (STM8AL3Lxx only)

In the following table, data are guaranteed by design and are not tested in production.

Table 48. LCD characteristics

Symbol	Parameter	Min	Typ	Max.	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.7	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.8	-	
V_{LCD3}	LCD internal reference voltage 3	-	2.9	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.0	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.1	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.2	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.3	-	
C_{EXT}	V_{LCD} external capacitance	0.1	-	2	µF
I_{DD}	Supply current(1) at V_{DD} = 1.8 V	-	3	-	µA
	Supply current(1) at V_{DD} = 3 V	-	3	-	
R_{HN} (2)	High value resistive network (low drive)	-	6.6	-	MΩ
R_{LN} (3)	Low value resistive network (high drive)	-	360	-	kΩ
V_{33}	Segment/Common higher level voltage	-	-	V_{LCDx}	V
V_{23}	Segment/Common 2/3 level voltage	-	$2/3V_{LCDx}$	-	
V_{12}	Segment/Common 1/2 level voltage	-	$1/2V_{LCDx}$	-	
V_{13}	Segment/Common 1/3 level voltage	-	$1/3V_{LCDx}$	-	
V_0	Segment/Common lowest level voltage	0	-	-	

1. LCD enabled with 3 V internal booster (LCD_CR1 = 0x08), 1/4 duty, 1/3 bias, division ratio= 64, all pixels active, no LCD connected.
2. R_{HN} is the total high value resistive network.
3. R_{LN} is the total low value resistive network.

VLCD external capacitor (STM8AL3Lxx only)

The application can achieve a stabilized LCD reference voltage by connecting an external capacitor C_{EXT} to the V_{LCD} pin. C_{EXT} is specified in *Table 48*.

9.3.10 Embedded reference voltage

In the following table, data are based on characterization results, not tested in production, unless otherwise specified.

In the following table, data based on characterization results, not tested in production.

Table 54. DAC accuracy

Symbol	Parameter	Conditions	Typ.	Max(1)	Unit
DNL	Differential non linearity(2)	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF, DACOUT buffer ON(3)	1.5	3	12-bit LSB
		No load, DACOUT buffer OFF	1.5	3	
INL	Integral non linearity(4)	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF,DACOUT buffer ON(3)	2	4	
		No load, DACOUT buffer OFF	2	4	
Offset	Offset error(5)	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF, DACOUT buffer ON(3)	±10	±25	
		No load, DACOUT buffer OFF	±5	±8	
Offset1	Offset error at Code 1 (6)	DACOUT buffer OFF	±1.5	±5	
Gain error	Gain error(7)	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF,DACOUT buffer ON(3)	+0.1/-0.2	+0.2/-0.5	%
		No load, DACOUT buffer OFF	+0/-0.2	+0/-0.4	
TUE	Total unadjusted error	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF, DACOUT buffer ON(3)	12	30	12-bit LSB
		No load, DACOUT buffer OFF	8	12	

1. Not tested in production.
2. Difference between two consecutive codes - 1 LSB.
3. For 48-pin packages only. For 28-pin and 32-pin packages, DAC output buffer must be kept off and no load must be applied.
4. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023.
5. Difference between the value measured at Code (0x800) and the ideal value = $V_{REF+}/2$.
6. Difference between the value measured at Code (0x001) and the ideal value.
7. Difference between the ideal slope of the transfer function and the measured slope computed from Code 0x000 and 0xFFF when buffer is ON, and from Code giving 0.2 V and (V_{DDA} -0.2) V when buffer is OFF.

In the following table, data are guaranteed by design, not tested in production.

Table 55. DAC output on PB4-PB5-PB6(1)

Symbol	Parameter	Conditions	Max	Unit
R_{int}	Internal resistance between DAC output and PB4-PB5-PB6 output	2.7 V < V_{DD} < 3.6 V	1.4	kΩ
		2.4 V < V_{DD} < 3.6 V	1.6	
		2.0 V < V_{DD} < 3.6 V	3.2	
		1.8 V < V_{DD} < 3.6 V	8.2	

1. 32 or 28-pin packages only. The DAC channel can be routed either on PB4, PB5 or PB6 using the routing interface I/O switch registers.

9.3.14 12-bit ADC1 characteristics

In the following table, data are guaranteed by design, not tested in production.

Table 56. ADC1 characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Sampling time	V_{AIN} on PF0 fast channel V_{DDA} < 2.4 V	0.43(4)(5)	-	-	µs
		V_{AIN} on PF0 fast channel 2.4 V ≤ V_{DDA} ≤ 3.6 V	0.22(4)(5)	-	-	
		V_{AIN} on slow channels V_{DDA} < 2.4 V	0.86(4)(5)	-	-	
		V_{AIN} on slow channels 2.4 V ≤ V_{DDA} ≤ 3.6 V	0.41(4)(5)	-	-	
t_{conv}	12-bit conversion time	-	12000000 / f_{ADC} + t_S			
		16 MHz	1(4)	-	-	
t_{WKUP}	Wakeup time from OFF state	-	-	-	3	
t_{IDLE}(6)	Time before a new conversion	-	-	-	∞	s
$t_{VREFINT}$	Internal reference voltage startup time	-	-	-	refer to *Table 49*	ms

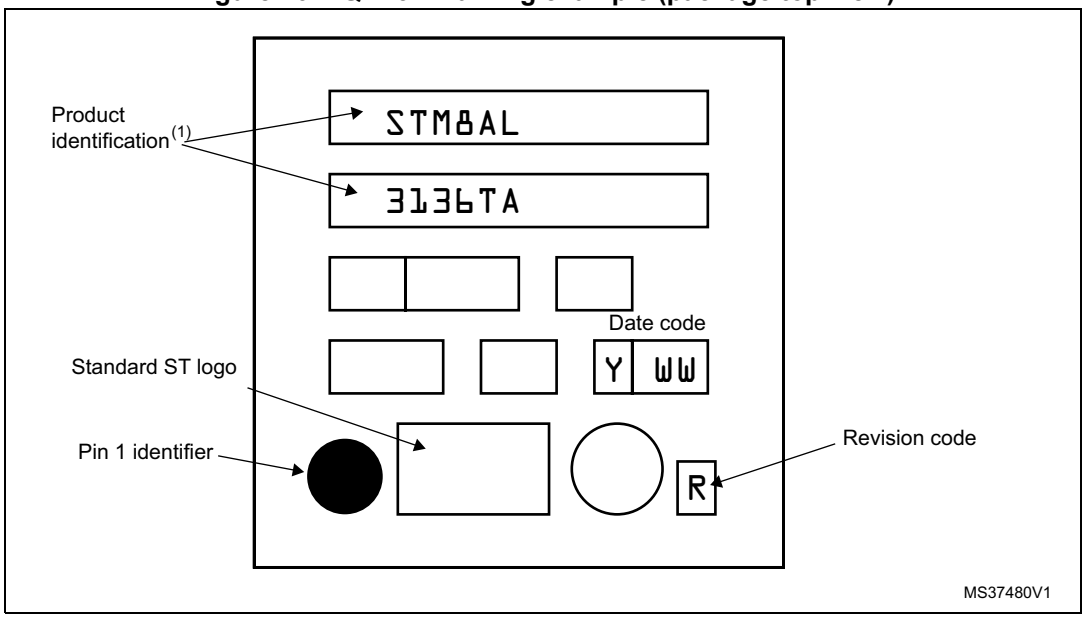
1. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. V_{REF-} or V_{DDA} must be tied to ground.
3. Guaranteed by design.
4. Minimum sampling and conversion time is reached for maximum Rext = 0.5 kΩ.
5. Value obtained for continuous conversion on fast channel.
6. In STM8L05xx, STM8L15xx, STM8L162x, STM8AL31xx, STM8AL3Lxx, STM8AL31Exx and STM8AL3LExx MCU families reference manual (RM0031), t_{IDLE} defines the time between 2 conversions, or between ADC ON and the first conversion. t_{IDLE} is not relevant for this device.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 46. LQFP32 marking example (package top view)



1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

12 Revision history

Table 69. Document revision history

Date	Revision	Changes
04-Jan-2012	1	Initial release
20-Dec-2012	2	Added consumption values when run from Flash or from RAM. Added 8k Flash devices STM8AL3138 and STM8AL3136 to *Table 1: Device summary*, *Table 2: Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x low-power device features and peripheral counts*. and *Figure 50: Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x ordering information scheme*. Added footnotes stating that power consumption has not been tested to *Table 21* and *Table 22* for HSE, and to *Table 23* and *Table 24* for LSE. Updated max LSI amperage values in *Table 23* and *Table 24*. Replaced *Table 38: Flash program memory* and *Table 39: Data memory*. Added a production test footnote to *Table 50: TS characteristics*. Updated voltage values in *Table 50: TS characteristics*, and current values in *Table 51: Comparator 1 characteristics* and *Table 52: Comparator 2 characteristics*. Removed *Figure 13: Typ. $I_{DD(LPR)}$ vs. V_{DD} (LSI clock source)* and *Figure 14: Typ. $I_{DD(LPW)}$ vs. V_{DD} (LSI clock source)*.
03-Jun-2013	3	Updated ‘Qualification conforms’ bullet on cover page. Updated ‘TS_Factory_CONV’ in *Figure 9: Memory map* Removed ‘rev G’ in *Table 18: Operating lifetime (OLF)* Ratings Replaced 0.40 by 0.38 in *Table 22: Total current consumption in Wait mode* ‘code executed from Flash’ fcpu = 125 kHz Updated footnote (3) in *Table 23: Total current consumption and timing in low-power run mode at VDD = 1.65 V to 3.6 V*, *Table 24: Total current consumption in low-power wait mode at VDD = 1.65 V to 3.6 V* and *Table 27: Total current consumption and timing in Halt mode at VDD = 1.65 to 3.6 V* Updated footnote (2) in *Table 26: Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal* Updated max ILEAK_HSE in *Table 30: HSE external clock characteristics* and *Table 31: LSE external clock characteristics* Updated ACC_{HSI} in *Table 34: HSI oscillator characteristics* Updated tprog max *Table 38: Flash program memory* Updated $STAB_{VREFINT}$ in *Table 49: Reference voltage characteristics* Updated ‘TS_Factory_CONV’ in *Table 50: TS characteristics* footnote. Updated ‘tconv’ and ‘title’ in *Table 56: ADC1 characteristics* Updated title in *Table 57: ADC1 accuracy with VDDA = 2.5 V to 3.3 V* Updated *Table 64: Electrical sensitivities*
14-Jun-2013	4	Updated max LSI measures in *Table 23: Total current consumption and timing in low-power run mode at VDD = 1.65 V to 3.6 V* and *Table 24: Total current consumption in low-power wait mode at VDD = 1.65 V to 3.6 V*