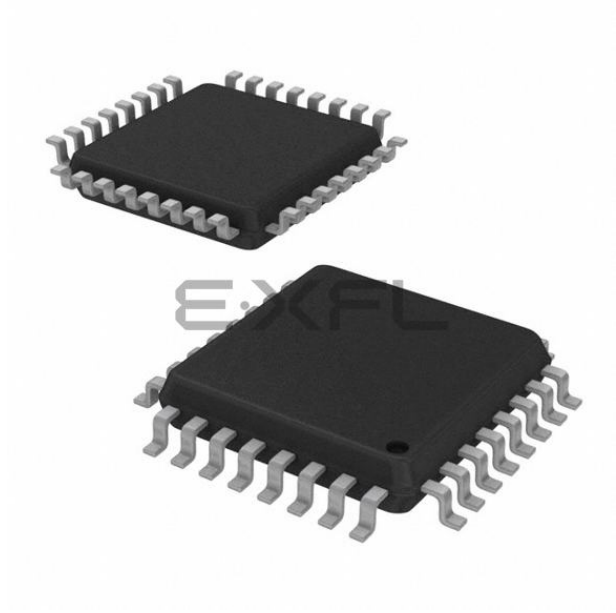

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	30
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3166tay

3.2 Central processing unit STM8

3.2.1 Advanced STM8 core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains six internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16 Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

3.2.2 Interrupt controller

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x feature a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts

3.10 Digital-to-analog converter (DAC)

- 12-bit DAC with output buffer
- Synchronized update capability using TIM4
- DMA capability
- External triggers for conversion
- Input reference voltage V_{REF+} for better resolution

Note: DAC can be served by DMA1.

3.11 Ultra-low-power comparators

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x embed two comparators (COMP1 and COMP2) that share the same current bias and voltage reference. The voltage reference can be internal or external (coming from an I/O).

- One comparator with fixed threshold (COMP1).
- One comparator rail to rail with fast or slow mode (COMP2). The threshold can be one of the following:
  - DAC output,
  - External I/O,
  - Internal reference voltage or internal reference voltage sub multiple (1/4, 1/2, 3/4).

The two comparators can be used together to offer a window function. They can wake up from Halt mode.

3.12 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1, COMP2, DAC and the internal reference voltage V_{REFINT}. It also provides a set of registers for efficiently managing the charge transfer acquisition sequence (see *Section 3.13: Timers*).

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 507F	DMA1	DMA1_C1CR	DMA1 channel 1 configuration register	0x00
0x00 5080		DMA1_C1SPR	DMA1 channel 1 status & priority register	0x00
0x00 5081		DMA1_C1NDTR	DMA1 number of data to transfer register (channel 1)	0x00
0x00 5082		DMA1_C1PARH	DMA1 peripheral address high register (channel 1)	0x52
0x00 5083		DMA1_C1PARL	DMA1 peripheral address low register (channel 1)	0x00
0x00 5084		Reserved area (1 byte)		
0x00 5085		DMA1_C1M0ARH	DMA1 memory 0 address high register (channel 1)	0x00
0x00 5086		DMA1_C1M0ARL	DMA1 memory 0 address low register (channel 1)	0x00
0x00 5087 0x00 5088		Reserved area (2 bytes)		
0x00 5089		DMA1_C2CR	DMA1 channel 2 configuration register	0x00
0x00 508A		DMA1_C2SPR	DMA1 channel 2 status & priority register	0x00
0x00 508B		DMA1_C2NDTR	DMA1 number of data to transfer register (channel 2)	0x00

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 12* for details on option byte addresses.

The option bytes can also be modified ‘on the fly’ by the application in IAP mode, except for the ROP, and UBC values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L15x/STM8L16x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0320) for information on SWIM programming procedures.

Table 12. Option byte addresses

Address	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0xAA
0x00 4802	UBC (User Boot code size)	OPT1	UBC[7:0]								0x00
0x00 4807	Reserved										0x00
0x00 4808	Independent watchdog option	OPT3 [3:0]	Reserved				WWDG_HALT	WWDG_HW	IWDG_HALT	IWDG_HW	0x00
0x00 4809	Number of stabilization clock cycles for HSE and LSE oscillators	OPT4	Reserved				LSECNT[1:0]		HSECNT[1:0]		0x00
0x00 480A	Brownout reset (BOR)	OPT5 [3:0]	Reserved				BOR_TH			BOR_ON	0x01
0x00 480B	Bootloader option bytes (OPTBL)	OPTBL [15:0]	OPTBL[15:0]								0x00
0x00 480C											0x00

Table 13. Option byte description

Option byte no.	Option description
OPT0	**ROP[7:0]** Memory readout protection (ROP) 0xAA: Disable readout protection (write access via SWIM protocol) Refer to Readout protection section in STM8L05xx, STM8L15xx, STM8L162x, STM8AL31xx, STM8AL3Lxx, STM8AL31Exx and STM8AL3LExx MCU families reference manual (RM0031).
OPT1	**UBC[7:0]** Size of the user boot code area 0x00: No UBC 0x01: the UBC contains only the interrupt vectors. 0x02: Page 0 and 1 reserved for the UBC and read/write protected. Page 0 contains only the interrupt vectors. 0x03: Page 0 to 2 reserved for UBC, memory write-protected. 0xFF: Page 0 to 254 reserved for the UBC, memory write-protected. Refer to User boot code section in STM8L05xx, STM8L15xx, STM8L162x, STM8AL31xx, STM8AL3Lxx, STM8AL31Exx and STM8AL3LExx MCU families reference manual (RM0031).
OPT2	Reserved
OPT3	**IWDG_HW:** Independent watchdog 0: Independent watchdog activated by software 1: Independent watchdog activated by hardware
	IWDG_HALT: Independent watchdog off in Halt/Active-halt 0: Independent watchdog continues running in Halt/Active-halt mode 1: Independent watchdog stopped in Halt/Active-halt mode
	WWDG_HW: Window watchdog 0: Window watchdog activated by software 1: Window watchdog activated by hardware
	WWDG_HALT: Window window watchdog reset on Halt/Active-halt 0: Window watchdog stopped in Halt mode 1: Window watchdog generates a reset when MCU enters Halt mode
OPT4	**HSECNT**: Number of HSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles
	LSECNT: Number of LSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles Refer to *Table 33: LSE oscillator characteristics*

Table 13. Option byte description (continued)

Option byte no.	Option description
OPT5	**BOR_ON**: 0: Brownout reset off 1: Brownout reset on
	BOR_TH[3:1]: Brownout reset thresholds. Refer to *Table 20* for details on the thresholds according to the value of BOR_TH bits.
OPTBL	**OPTBL[15:0]**: This option is checked by the boot ROM code after reset. Depending on the content of addresses Ox00 480B, Ox00 480C and 0x8000 (reset vector) the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 bootloader user manual for more details.

Table 16. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by IR_TIM pin (with high sink LED driver capability)	80	
	Output current sunk by any other I/O and control pin	25	
	Output current sourced by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$	Injected current on true open-drain pins (PC0 and PC1)(1)	- 5/+0	
	Injected current on five-volt tolerant (FT) pins (PA7 and PE0)(1)	- 5/+0	
	Injected current on 3.6 V tolerant (TT) pins(1)	- 5/+0	
	Injected current on any other pin(2)	- 5/+5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(3)	± 25	

1. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15* for maximum allowed input voltage values.
2. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15* for maximum allowed input voltage values.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	° C
T_J	Maximum junction temperature	150	

Table 18. Operating lifetime (OLF)(1)

Symbol	Ratings	Value	Unit
OLF	Conforming to AEC-Q100	-40 to 125 °C	Grade 1

1. For detailed mission profile analysis, please contact the local ST Sales Office.

Table 20. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PDR}	Power-down reset threshold	Falling edge	1.30	1.50	1.65(2)	V
V_{BOR0}	Brown-out reset threshold 0 (BOR_TH[2:0]=000)	Falling edge	1.45	1.70	1.74(2)	
		Rising edge	1.69(2)	1.75	1.80	
V_{BOR1}	Brown-out reset threshold 1 (BOR_TH[2:0]=001)	Falling edge	1.75	1.93	1.97(2)	
		Rising edge	1.96(2)	2.04	2.23	
V_{BOR2}	Brown-out reset threshold 2 (BOR_TH[2:0]=010)	Falling edge	2.10	2.30	2.35(2)	
		Rising edge	2.31(2)	2.41	2.61	
V_{BOR3}	Brown-out reset threshold 3 (BOR_TH[2:0]=011)	Falling edge	2.35	2.55	2.60(2)	
		Rising edge	2.54(2)	2.66	2.86	
V_{BOR4}	Brown-out reset threshold 4 (BOR_TH[2:0]=100)	Falling edge	2.59	2.80	2.85(2)	
		Rising edge	2.78(2)	2.90	3.09	
V_{PVD0}	PVD threshold 0	Falling edge	1.75	1.84	1.88(2)	
		Rising edge	1.88(2)	1.94	2.15	
V_{PVD1}	PVD threshold 1	Falling edge	1.95	2.04	2.09(2)	
		Rising edge	2.08(2)	2.14	2.35	
V_{PVD2}	PVD threshold 2	Falling edge	2.14	2.24	2.28(2)	
		Rising edge	2.28(2)	2.34	2.56	
V_{PVD3}	PVD threshold 3	Falling edge	2.33	2.44	2.48(2)	
		Rising edge	2.47(2)	2.54	2.75	
V_{PVD4}	PVD threshold 4	Falling edge	2.52	2.64	2.69(2)	
		Rising edge	2.68(2)	2.74	2.88	
V_{PVD5}	PVD threshold 5	Falling edge	2.71	2.83	2.88(2)	
		Rising edge	2.87(2)	2.94	3.15	
V_{PVD6}	PVD threshold 6	Falling edge	2.91	3.05	3.09(2)	
		Rising edge	3.08(2)	3.15	3.35	

1. Guaranteed by design.
2. Guaranteed by characterization results.

Table 22. Total current consumption in Wait mode (continued)

Symbol	Parameter	Conditions[1]			Typ	Max	Unit
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.38	0.55(3)	mA
				f_{CPU} = 1 MHz	0.40	0.60(3)	
				f_{CPU} = 4 MHz	0.50	0.65(3)	
				f_{CPU} = 8 MHz	0.60	0.75(3)	
				f_{CPU} = 16 MHz	0.80	0.90	
			HSE(4) external clock (f_{CPU}=HSE)	f_{CPU} = 125 kHz	0.05	0.10(3)	
				f_{CPU} = 1 MHz	0.10	0.20(3)	
				f_{CPU} = 4 MHz	0.25	0.45(3)	
				f_{CPU} = 8 MHz	0.50	0.65(3)	
				f_{CPU} = 16 MHz	1.00	1.20(3)	
			LSI	$f_{CPU} = f_{LSI}$	0.05	0.10(3)	
			LSE(5) external clock (32.768 kHz)	$f_{CPU} = f_{LSE}$	0.05	0.08(3)	

1. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU} = f_{SYSCLK}$
2. Flash is configured in I_{DDQ} mode in Wait mode by setting the EPM or WAITM bit in the Flash_CR1 register.
3. Guaranteed by characterization results.
4. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 32*.
5. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 33*.

Table 29. Current consumption under external reset

Symbol	Parameter	Conditions		Typ	Unit
$I_{DD(RST)}$	Supply current under external reset (1)	All pins are externally tied to V_{DD}	V_{DD} = 1.8 V	48	µA
			V_{DD} = 3 V	76	
			V_{DD} = 3.6 V	91	

1. All pins except PA0, PB0 and PB4 are floating under reset. PA0, PB0 and PB4 are configured with pull-up under reset.

9.3.4 Clock and timing characteristics

HSE external clock (HSEBYP = 1 in CLK_ECKCR)

Subject to general operating conditions for V_{DD} and T_A.

Table 30. HSE external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	-	1(1)	-	16(1)	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7 x V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	0.3 x V_{DD}	
$C_{in(HSE)}$	OSC_IN input capacitance	-	-	2.6	-	pF
I_{LEAK_HSE}	OSC_IN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-	-	±500	nA

1. Guaranteed by design.

LSE external clock (LSEBYP=1 in CLK_ECKCR)

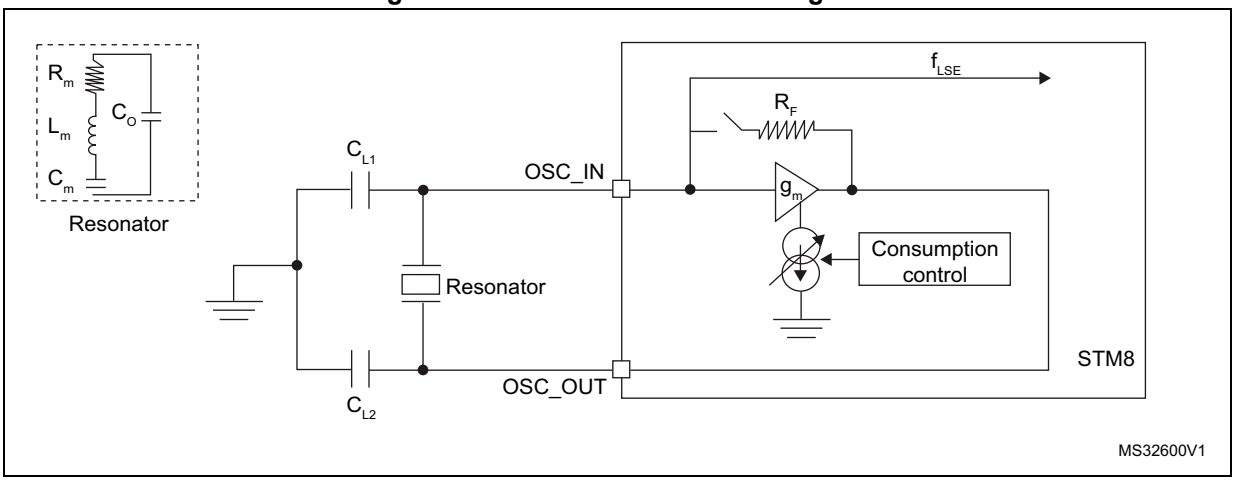
Subject to general operating conditions for V_{DD} and T_A.

Table 31. LSE external clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency	-	32.768	-	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	0.7 x V_{DD}(1)	-	V_{DD}(1)	V
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}(1)	-	0.3 x V_{DD}(1)	
$C_{in(LSE)}$	OSC32_IN input capacitance	-	0.6	-	pF
I_{LEAK_LSE}	OSC32_IN input leakage current	-		±500	nA

1. Guaranteed by characterization results.

Figure 16. LSE oscillator circuit diagram



Internal clock sources

Subject to general operating conditions for V_{DD}, and T_A.

High speed internal RC oscillator (HSI)

In the following table, data are based on characterization results and are not tested in production, unless otherwise specified.

Table 34. HSI oscillator characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
ACC_{HSI}	HSI oscillator user trimming accuracy	Trimmed by the application for any V_{DD} and T_A conditions	-1	-	1	%
	HSI oscillator accuracy (factory calibrated)	$V_{DD} \le 1.8\ V \le V_{DD} \le 3.6\ V$, $-40\ °C \le T_A \le 125\ °C$	-5	-	5	
TRIM	HSI user trimming step(2)	Trimming code ≠ multiple of 16	-	0.4	0.7(2)	
		Trimming code = multiple of 16	-		± 1.5(2)	
$t_{su(HSI)}$	HSI oscillator setup time (wakeup time)	-	-	3.7	6(3)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	100	140(3)	µA

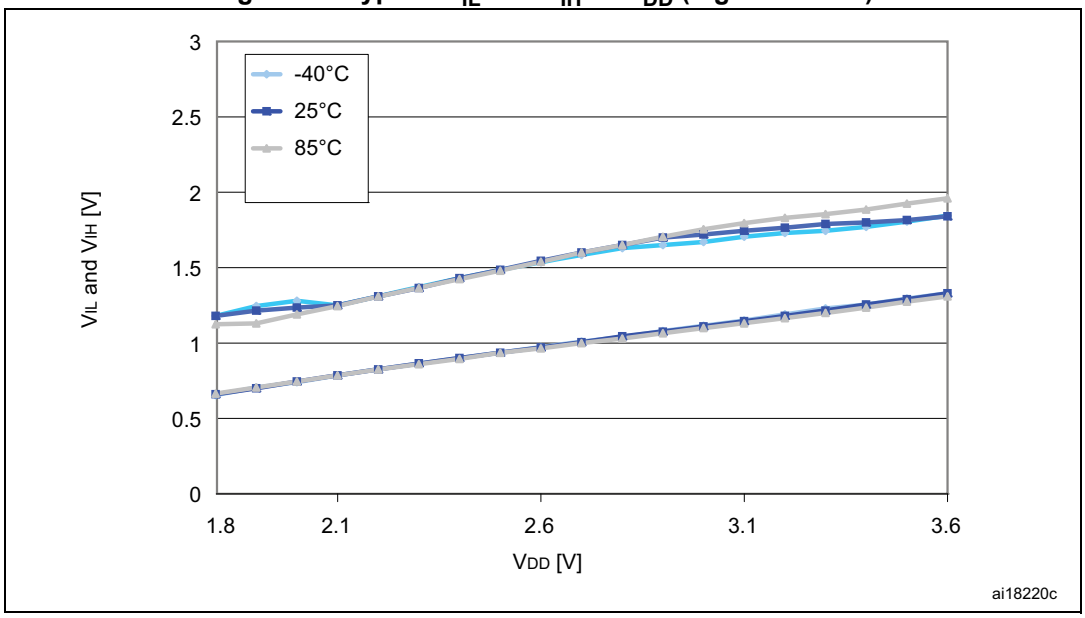
1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0). Refer to the AN3101 “STM8L05xxx/15xxx, STM8L162xx and STM8AL31xx/3Lxx internal RC oscillator calibration” application note for more details.
3. Guaranteed by design.

Table 41. I/O static characteristics (continued)

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	30(6)	45	60(6)	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. If V_{IH} maximum cannot be respected, the injection current must be limited externally to $I_{INJ(PIN)}$ maximum.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 22*).
6. Data not tested in production.

Figure 19. Typical V_{IL} and V_{IH} vs V_{DD} (high sink I/Os)



NRST pin

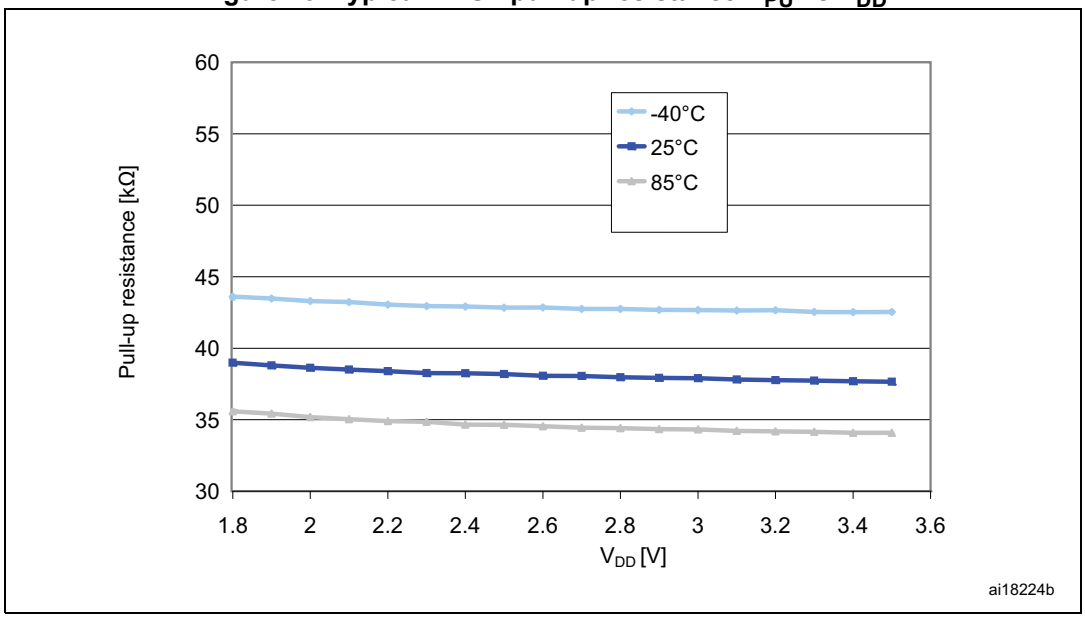
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 45. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	V_{SS}(1)	-	0.8(1)	V
$V_{IH(NRST)}$	NRST input high level voltage	-	1.4(1)	-	V_{DD}(1)	
$V_{OL(NRST)}$	NRST output low level voltage	I_{OL} = 2 mA for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	0.4(1)	
		I_{OL} = 1.5 mA for V_{DD} < 2.7 V	-	-		
V_{HYST}	NRST input hysteresis	-	10%V_{DD}(2)(3)	-	-	mV
$R_{PU(NRST)}$	NRST pull-up equivalent resistor	-	30(1)	45	60(1)	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	50(3)	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	-	300(3)	-	-	

1. Guaranteed by characterization results.
2. 200 mV min.
3. Guaranteed by design.

Figure 29. Typical NRST pull-up resistance R_{PU} vs V_{DD}



9.3.9 LCD controller (STM8AL3Lxx only)

In the following table, data are guaranteed by design and are not tested in production.

Table 48. LCD characteristics

Symbol	Parameter	Min	Typ	Max.	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.7	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.8	-	
V_{LCD3}	LCD internal reference voltage 3	-	2.9	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.0	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.1	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.2	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.3	-	
C_{EXT}	V_{LCD} external capacitance	0.1	-	2	µF
I_{DD}	Supply current(1) at V_{DD} = 1.8 V	-	3	-	µA
	Supply current(1) at V_{DD} = 3 V	-	3	-	
R_{HN} (2)	High value resistive network (low drive)	-	6.6	-	MΩ
R_{LN} (3)	Low value resistive network (high drive)	-	360	-	kΩ
V_{33}	Segment/Common higher level voltage	-	-	V_{LCDx}	V
V_{23}	Segment/Common 2/3 level voltage	-	$2/3V_{LCDx}$	-	
V_{12}	Segment/Common 1/2 level voltage	-	$1/2V_{LCDx}$	-	
V_{13}	Segment/Common 1/3 level voltage	-	$1/3V_{LCDx}$	-	
V_0	Segment/Common lowest level voltage	0	-	-	

1. LCD enabled with 3 V internal booster (LCD_CR1 = 0x08), 1/4 duty, 1/3 bias, division ratio= 64, all pixels active, no LCD connected.
2. R_{HN} is the total high value resistive network.
3. R_{LN} is the total low value resistive network.

VLCD external capacitor (STM8AL3Lxx only)

The application can achieve a stabilized LCD reference voltage by connecting an external capacitor C_{EXT} to the V_{LCD} pin. C_{EXT} is specified in *Table 48*.

9.3.10 Embedded reference voltage

In the following table, data are based on characterization results, not tested in production, unless otherwise specified.

Table 56. ADC1 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	2.4 V ≤ V_{DDA} ≤ 3.6 V	2.4	-	V_{DDA}	V
		1.8 V ≤ V_{DDA} ≤ 2.4 V	V_{DDA}			
V_{REF-}	Lower reference voltage	-	V_{SSA}			
I_{VDDA}	Current on the V_{DDA} input pin	-	-	1000	1450	µA
I_{VREF+}	Current on the V_{REF+} input pin	-	-	400	700 (peak)(1)	
		-	-		450 (average)(1)	
V_{AIN}	Conversion voltage range	-	0(2)	-	V_{REF+}	-
T_A	Temperature range	-	-40	-	125	°C
R_{AIN}	External resistance on V_{AIN}	on PF0 fast channel	-	-	50(3)	kΩ
		on all other channels	-	-		
C_{ADC}	Internal sample and hold capacitor	on PF0 fast channel	-	16	-	pF
		on all other channels	-		-	
f_{ADC}	ADC sampling clock frequency	2.4 V ≤ V_{DDA} ≤ 3.6 V without zooming	0.320	-	16	MHz
		1.8 V ≤ V_{DDA} ≤ 2.4 V with zooming	0.320	-	8	
f_{CONV}	12-bit conversion rate	V_{AIN} on PF0 fast channel	-	-	1(4)(5)	
		V_{AIN} on all other channels	-	-	760(4)(5)	kHz
f_{TRIG}	External trigger frequency	-	-	-	t_{conv}	$1/f_{ADC}$
t_{LAT}	External trigger latency	-	-	-	3.5	$1/f_{SYSCLK}$

Table 59. ADC1 accuracy with $V_{DDA} = V_{REF}^+ = 1.8$ V to 2.4 V

Symbol	Parameter	Typ.	Max(1)	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	2	3	
TUE	Total unadjusted error	3	5	
Offset	Offset error	2	3	
Gain	Gain error	2	3	

1. Not tested in production.

Figure 36. ADC1 accuracy characteristics

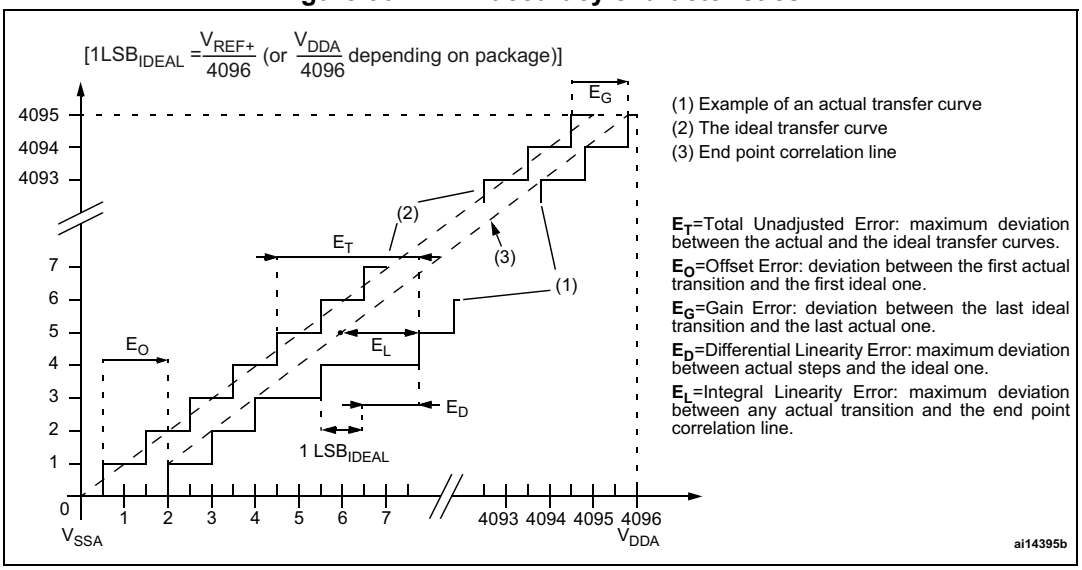
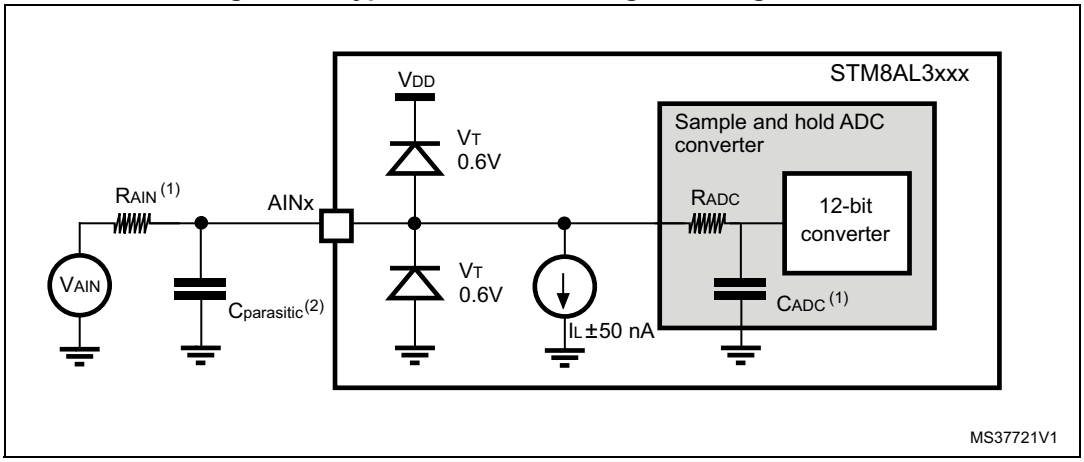


Figure 37. Typical connection diagram using the ADC



1. Refer to *Table 56* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

Figure 39. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

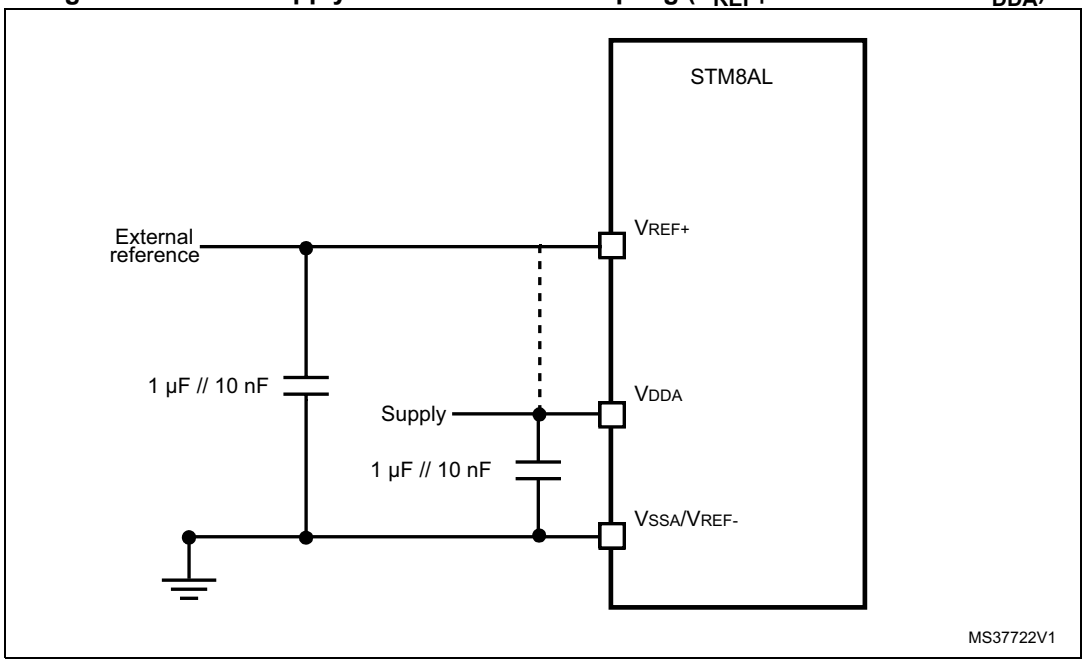


Figure 40. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

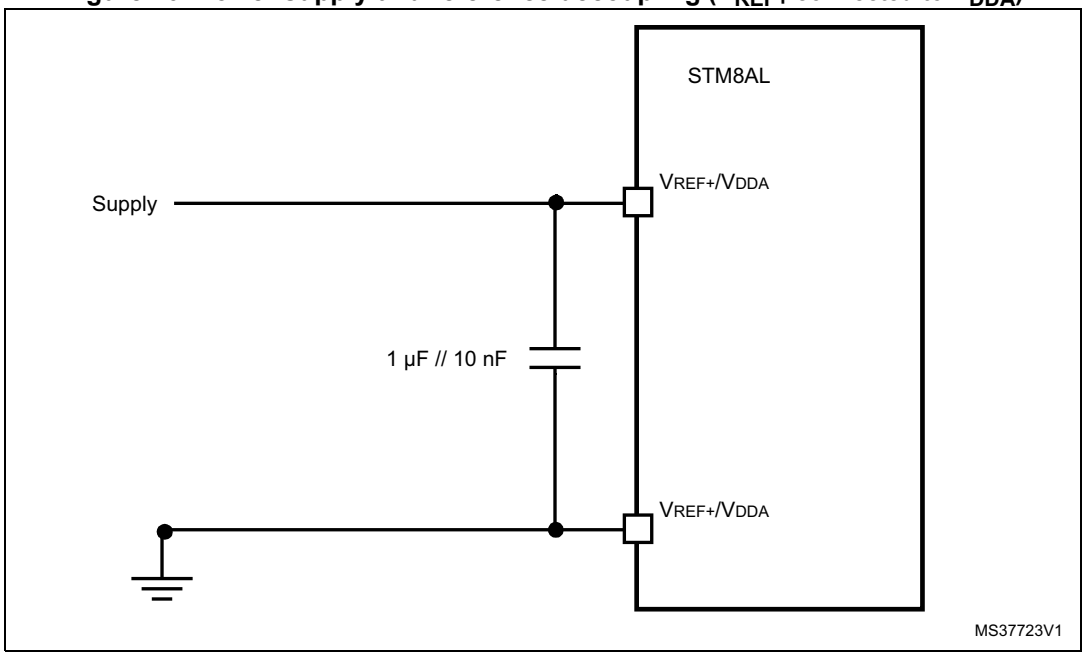
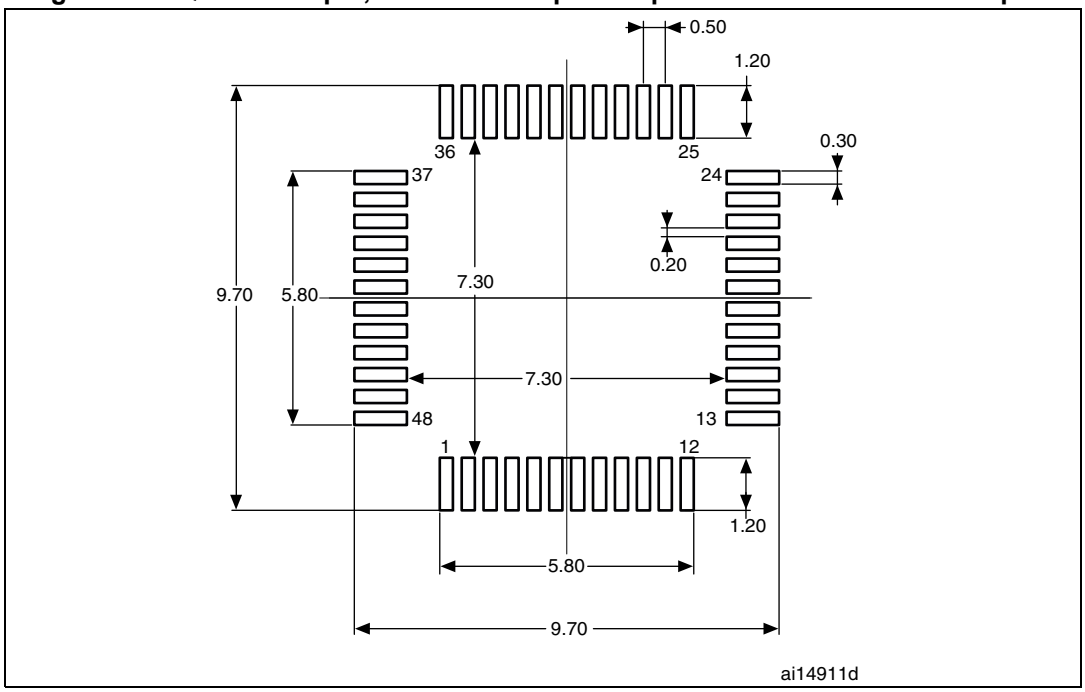


Table 65. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 42. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint

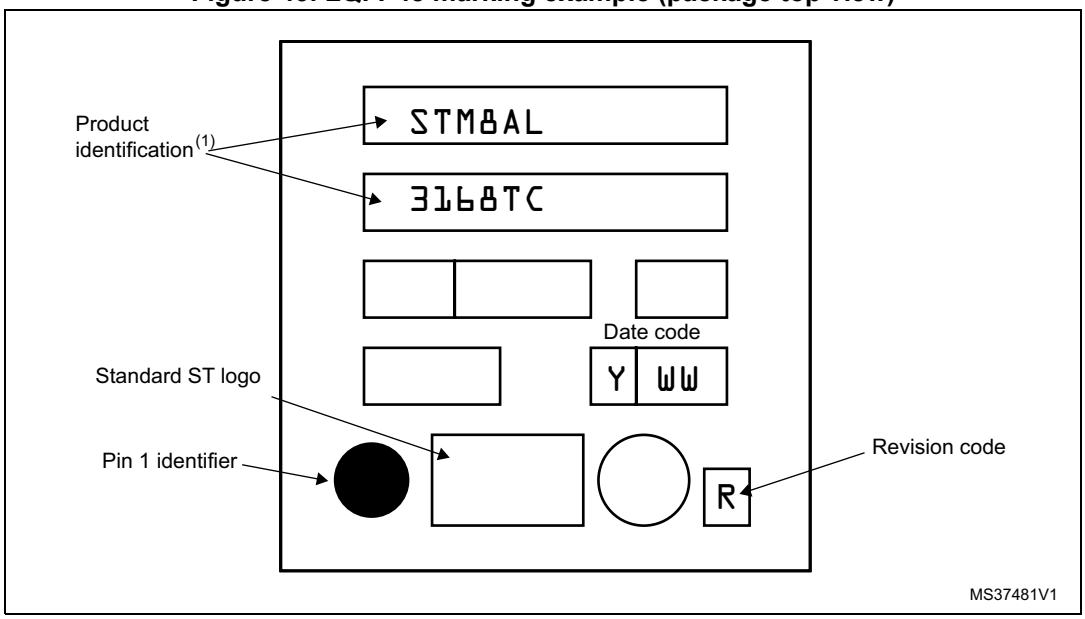


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 43. LQFP48 marking example (package top view)



1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.