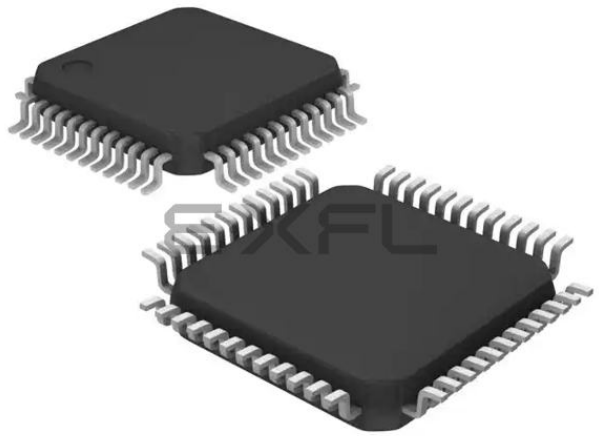


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

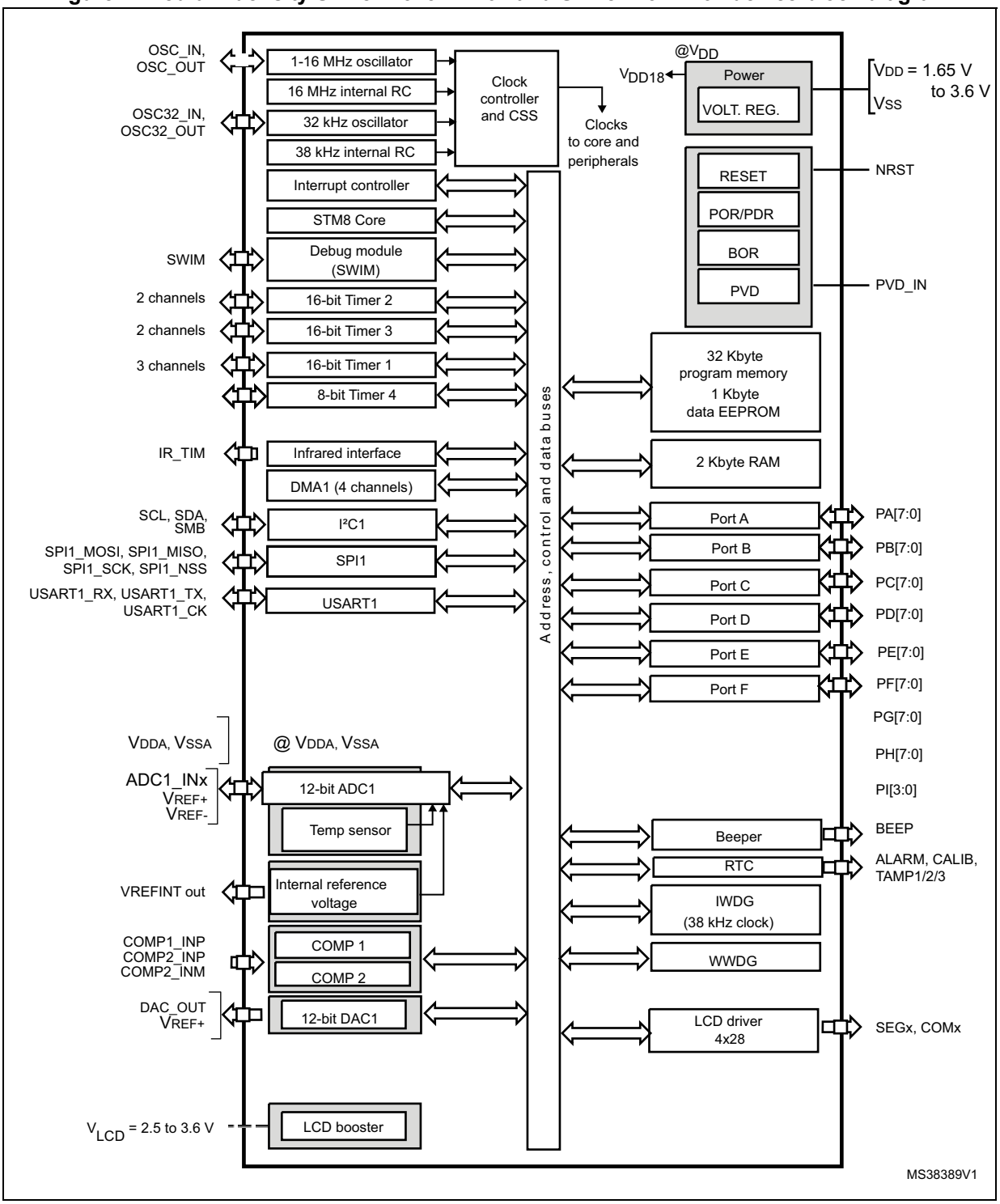
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	41
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 25x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3168tay

3 Functional overview

Figure 1. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x device block diagram



1. **Legend**: ADC (Analog-to-digital converter), BOR (Brownout reset), DMA (Direct memory access), DAC (Digital-to-analog converter), I²C (Inter-integrated circuit multimaster interface), IWDG (Independent watchdog), LCD (Liquid crystal display), POR/PDR (Power on reset / power down reset), RTC (Real-time clock), SPI (Serial peripheral interface), SWIM (Single wire interface module), USART (Universal synchronous asynchronous receiver transmitter), WWDG (Window watchdog).

3.2 Central processing unit STM8

3.2.1 Advanced STM8 core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains six internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16 Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

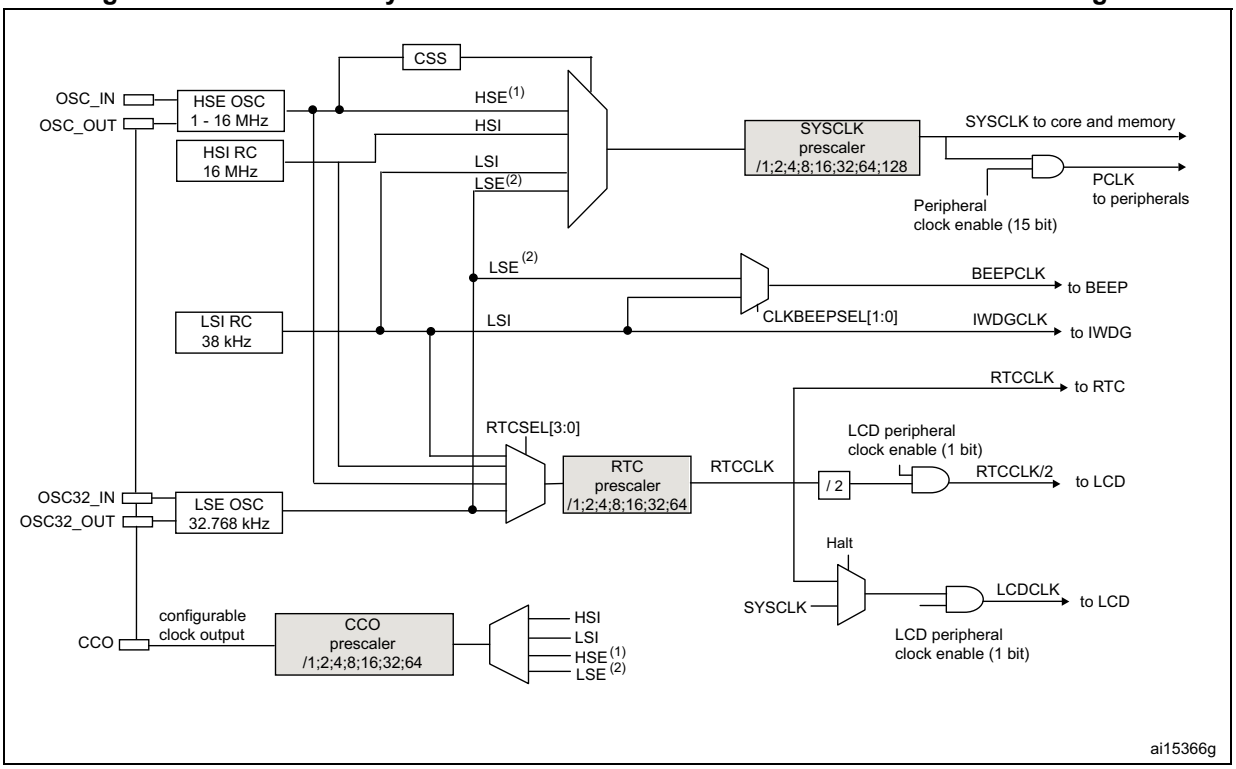
- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

3.2.2 Interrupt controller

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x feature a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts

Figure 2. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x clock tree diagram



1. The HSE clock source can be either an external crystal/ceramic resonator or an external source (HSE bypass). Refer to *Section HSE clock* in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).
2. The LSE clock source can be either an external crystal/ceramic resonator or a external source (LSE bypass). Refer to *Section LSE clock* in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).

3.5 Low power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours.
- Periodic alarms based on the calendar can also be generated from every second to every year.

Table 5. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x pin description (continued)

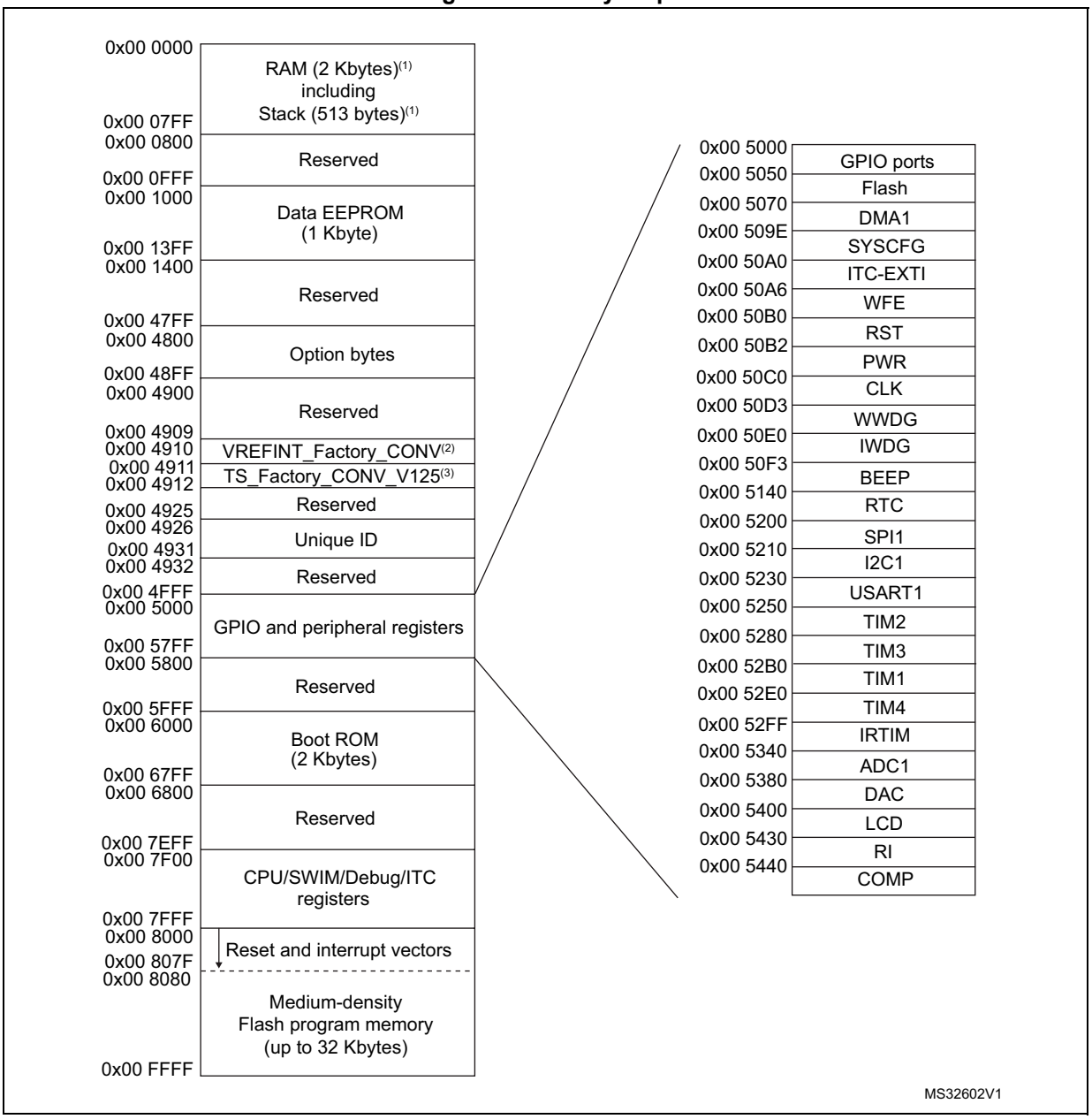
Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48	VFQFPN32	LQFP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
34	22	22	PD5/TIM1_CH3 /LCD_SEG19(2)/ ADC1_IN9/COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port D5	Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9/ Comparator 1 positive input
35	23	23	PD6/TIM1_BKIN /LCD_SEG20(2)/ ADC1_IN8/RTC_CALIB/ /VREFINT/ COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port D6	Timer 1 - break input / LCD segment 20 / ADC1_IN8 / RTC calibration / Internal voltage reference output / Comparator 1 positive input
36	24	24	PD7/TIM1_CH1N /LCD_SEG21(2)/ ADC1_IN7/RTC_ALARM/ VREFINT/ COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port D7	Timer 1 - inverted channel 1/ LCD segment 21 / ADC1_IN7 / RTC alarm / Internal voltage reference output /Comparator 1 positive input
14	-	-	PE0(5)/LCD_SEG1(2)	I/O	FT	X	X	X	HS	X	X	Port E0	LCD segment 1
15	-	-	PE1/TIM1_CH2N /LCD_SEG2(2)	I/O	TT(3)	X	X	X	HS	X	X	Port E1	Timer 1 - inverted channel 2 / LCD segment 2
16	-	-	PE2/TIM1_CH3N /LCD_SEG3(2)	I/O	TT(3)	X	X	X	HS	X	X	Port E2	Timer 1 - inverted channel 3 / LCD segment 3
17	-	-	PE3/LCD_SEG4(2)	I/O	TT(3)	X	X	X	HS	X	X	Port E3	LCD segment 4
18	-	-	PE4/LCD_SEG5(2)	I/O	TT(3)	X	X	X	HS	X	X	Port E4	LCD segment 5
19	-	-	PE5/LCD_SEG6(2)/ ADC1_IN23/COMP2_INP / COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port E5	LCD segment 6 / ADC1_IN23 / Comparator 2 positive input / Comparator 1 positive input
47	-	-	PE6/LCD_SEG26(2)/ PVD_IN	I/O	TT(3)	X	X	X	HS	X	X	Port E6	LCD segment 26/PVD_IN
48	-	-	PE7/LCD_SEG27(2)	I/O	TT(3)	X	X	X	HS	X	X	Port E7	LCD segment 27
32	-	-	PF0/ADC1_IN24/ DAC_OUT	I/O	TT(3)	X	X	X	HS	X	X	Port F0	ADC1_IN24 / DAC_OUT

5 Memory and register map

5.1 Memory mapping

The memory map is shown in *Figure 9*.

Figure 9. Memory map



1. *Table 6* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. The VREFINT_Factory_CONV byte represents the LSB of the V_{REFINT} 12-bit ADC conversion result. The MSB have a fixed value: 0x6.
3. The TS_Factory_CONV_V125 byte represents the LSB of the V_{125} 12-bit ADC conversion result. The MSB have a fixed value: 0x3. The V_{125} measurement is performed at 125°C.
4. Refer to *Table 9* for an overview of hardware register mapping, to *Table 8* for details on I/O port hardware registers, and to *Table 10* for information on CPU/SWIM/debug module controller registers.

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 508C	DMA1	DMA1_C2PARH	DMA1 peripheral address high register (channel 2)	0x52
0x00 508D		DMA1_C2PARL	DMA1 peripheral address low register (channel 2)	0x00
0x00 508E		Reserved area (1 byte)		
0x00 508F		DMA1_C2M0ARH	DMA1 memory 0 address high register (channel 2)	0x00
0x00 5090		DMA1_C2M0ARL	DMA1 memory 0 address low register (channel 2)	0x00
0x00 5091 0x00 5092		Reserved area (2 bytes)		
0x00 5093		DMA1_C3CR	DMA1 channel 3 configuration register	0x00
0x00 5094		DMA1_C3SPR	DMA1 channel 3 status & priority register	0x00
0x00 5095		DMA1_C3NDTR	DMA1 number of data to transfer register (channel 3)	0x00
0x00 5096		DMA1_C3PARH_ C3M1ARH	DMA1 peripheral address high register (channel 3)	0x40
0x00 5097		DMA1_C3PARL_ C3M1ARL	DMA1 peripheral address low register (channel 3)	0x00
0x00 5098		Reserved area (1 byte)		
0x00 5099		DMA1_C3M0ARH	DMA1 memory 0 address high register (channel 3)	0x00
0x00 509A		DMA1_C3M0ARL	DMA1 memory 0 address low register (channel 3)	0x00
0x00 509B to 0x00 509D		Reserved area (3 bytes)		
0x00 509E	SYSCFG	SYSCFG_RMPCR1	Remapping register 1	0x00
0x00 509F		SYSCFG_RMPCR2	Remapping register 2	0x00
0x00 50A0	ITC - EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF1	External interrupt port select register 1	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8		WFE_CR3	WFE control register 3	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50A9 to 0x00 50AF	Reserved area (7 bytes)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2	PWR	PWR_CSR1	Power control and status register 1	0x00
0x00 50B3		PWR_CSR2	Power control and status register 2	0x00
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_DIVR	Clock master divider register	0x03
0x00 50C1		CLK_CRTCR	Clock RTC register	0x00
0x00 50C2		CLK_ICKR	Internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	Peripheral clock gating register 1	0x00
0x00 50C4		CLK_PCKENR2	Peripheral clock gating register 2	0x80
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6		CLK_ECKR	External clock control register	0x00
0x00 50C7		CLK_SCSR	System clock status register	0x01
0x00 50C8		CLK_SWR	System clock switch register	0x01
0x00 50C9		CLK_SWCR	Clock switch control register	0bxxxx0000
0x00 50CA		CLK_CSSR	Clock security system register	0x00
0x00 50CB		CLK_CBEEPR	Clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	HSI calibration register	0xxx
0x00 50CD		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	Main regulator control status register	0bxx11100x
0x00 50D0 to 0x00 50D2	Reserved area (3 bytes)			
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDR window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF

6 Interrupt vector mapping

Table 11. Interrupt mapping

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
-	RESET	Reset	Yes	Yes	Yes	Yes	0x00 8000
-	TRAP	Software interrupt	-	-	-	-	0x00 8004
0	Reserved						0x00 8008
1	FLASH	Flash end of programming/write attempted to protected page interrupt	-	-	Yes	Yes	0x00 800C
2	DMA1 0/1	DMA1 channels 0/1 half transaction/transaction complete interrupt	-	-	Yes	Yes	0x00 8010
3	DMA1 2/3	DMA1 channels 2/3 half transaction/transaction complete interrupt	-	-	Yes	Yes	0x00 8014
4	RTC	RTC alarm A/ wakeup/tamper 1/ tamper 2/tamper 3	Yes	Yes	Yes	Yes	0x00 8018
5	EXTI E/F/ PVD(2)	External interrupt port E/F PVD interrupt	Yes	Yes	Yes	Yes	0x00 801C
6	EXTIB/G	External interrupt port B/G	Yes	Yes	Yes	Yes	0x00 8020
7	EXTID/H	External interrupt port D/H	Yes	Yes	Yes	Yes	0x00 8024
8	EXTI0	External interrupt 0	Yes	Yes	Yes	Yes	0x00 8028
9	EXTI1	External interrupt 1	Yes	Yes	Yes	Yes	0x00 802C
10	EXTI2	External interrupt 2	Yes	Yes	Yes	Yes	0x00 8030
11	EXTI3	External interrupt 3	Yes	Yes	Yes	Yes	0x00 8034
12	EXTI4	External interrupt 4	Yes	Yes	Yes	Yes	0x00 8038
13	EXTI5	External interrupt 5	Yes	Yes	Yes	Yes	0x00 803C
14	EXTI6	External interrupt 6	Yes	Yes	Yes	Yes	0x00 8040
15	EXTI7	External interrupt 7	Yes	Yes	Yes	Yes	0x00 8044
16	LCD	LCD interrupt	-	-	Yes	Yes	0x00 8048
17	CLK/TIM1/ DAC	CLK system clock switch/ CSS interrupt/ TIM1 Break/DAC	-	-	Yes	Yes	0x00 804C

Figure 12. POR/BOR thresholds

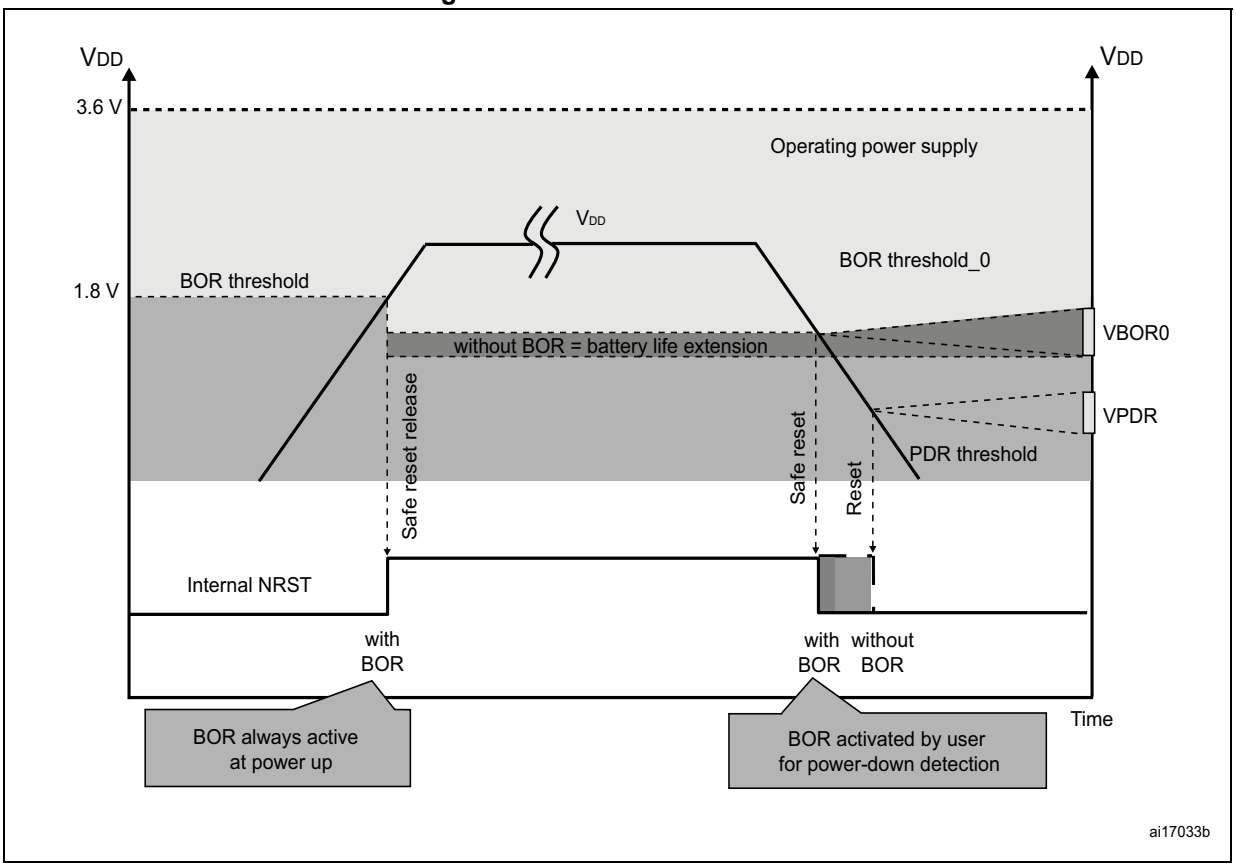


Table 25. Total current consumption and timing in active-halt mode at V_{DD} = 1.65 V to 3.6 V (continued)

Symbol	Parameter	Conditions (1)			Typ	Max(2)	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSE external clock (32.768 kHz) (7)	LCD OFF(8)	T_A = -40 °C to 25 °C	0.50	1.20	µA
				T_A = 85 °C	0.90	2.10	
				T_A = 125 °C	4.80	11.00	
			LCD ON (static duty/ external V_{LCD}) (4)	T_A = -40 °C to 25 °C	0.85	1.90	
				T_A = 85 °C	1.30	3.20	
				T_A = 125 °C	5.00	12.00	
			LCD ON (1/4 duty/ external V_{LCD}) (5)	T_A = -40 °C to 25 °C	1.50	2.50	
				T_A = 85 °C	1.80	4.20	
				T_A = 125 °C	5.70	14.00	
			LCD ON (1/4 duty/ internal V_{LCD}) (6)	T_A = -40 °C to 25 °C	3.40	7.60	
				T_A = 85 °C	3.90	9.20	
				T_A = 125 °C	6.30	15.20	
$I_{DD(WUFAH)}$	Supply current during wakeup time from Active-halt mode (using HSI)	-	-	-	2.40	-	mA
$t_{WU\_HSI(AH)}$ (9) (10)	Wakeup time from Active-halt mode to Run mode (using HSI)	-			4.70	7.00	µs
$t_{WU\_LSI(AH)}$ (9) (10)	Wakeup time from Active-halt mode to Run mode (using LSI)	-			150.0	-	

1. No floating I/O, unless otherwise specified.
2. Guaranteed by characterization results.
3. RTC enabled. Clock source = LSI.
4. RTC enabled, LCD enabled with external V_{LCD} = 3 V, static duty, division ratio = 256, all pixels active, no LCD connected.
5. RTC enabled, LCD enabled with external V_{LCD}, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
6. LCD enabled with internal LCD booster V_{LCD} = 3 V, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
7. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 33*.
8. RTC enabled. Clock source = LSE.
9. Wakeup time until start of interrupt vector fetch.
   The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.
10. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.

HSE crystal/ceramic resonator oscillator

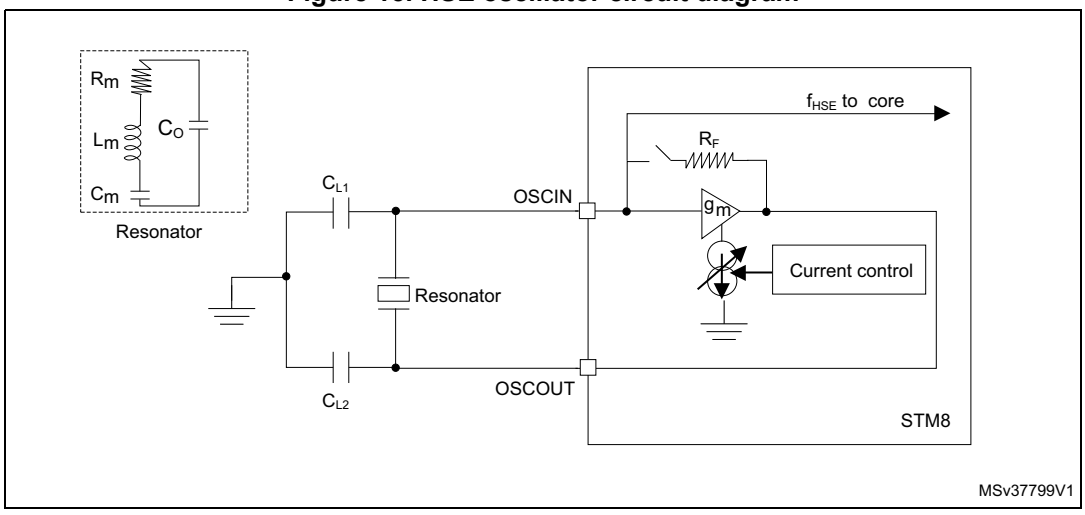
The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 32. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	High speed external oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$C^{(1)}$	Recommended load capacitance $^{(2)}$	-	-	20	-	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)$^{(3)}$	mA
		C = 10 pF, f_{OSC} =16 MHz	-	-	2.5 (startup) 0.46 (stabilized)$^{(3)}$	
g_m	Oscillator transconductance	-	3.5$^{(3)}$	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

1. $C=C_{L1}=C_{L2}$ is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Guaranteed by design.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

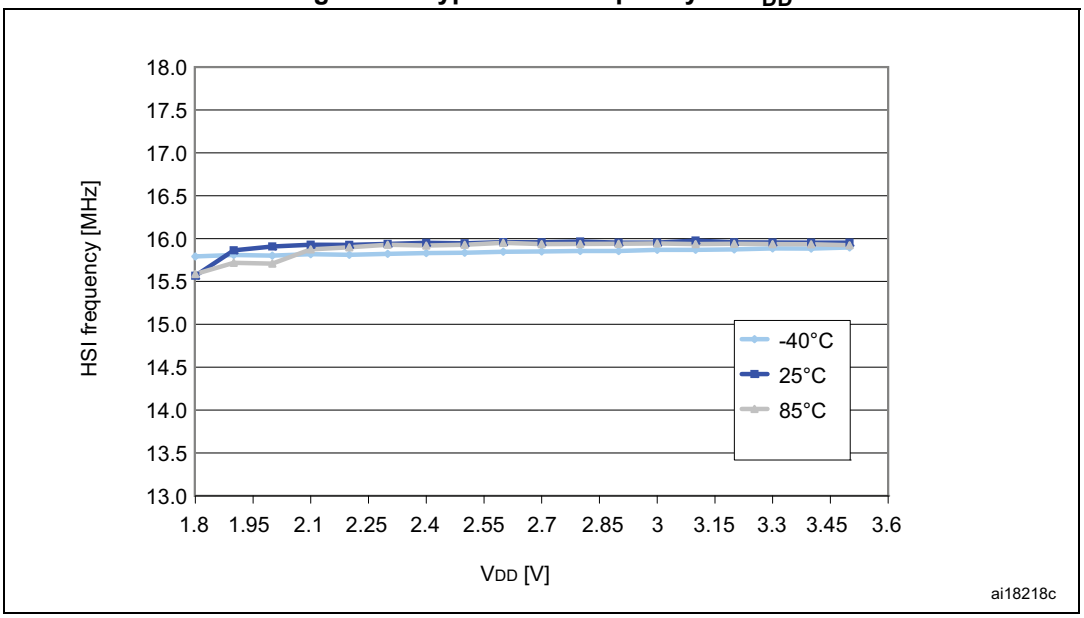
Figure 15. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

Figure 17. Typical HSI frequency vs V_{DD}



Low speed internal RC oscillator (LSI)

In the following table, data are based on characterization results, not tested in production.

Table 35. LSI oscillator characteristics

Symbol	Parameter (1)	Conditions(1)	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	26	38	56	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	200(2)	µs
$I_{DD(LSI)}$	LSI oscillator frequency drift(3)	0 °C ≤ T_A ≤ 85 °C	-12	-	11	%

1. V_{DD} = 1.65 V to 3.6 V, T_A = -40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. This is a deviation for an individual part, once the initial frequency has been measured.

Table 41. I/O static characteristics (continued)

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	30(6)	45	60(6)	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. If V_{IH} maximum cannot be respected, the injection current must be limited externally to $I_{INJ(PIN)}$ maximum.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 22*).
6. Data not tested in production.

Figure 19. Typical V_{IL} and V_{IH} vs V_{DD} (high sink I/Os)

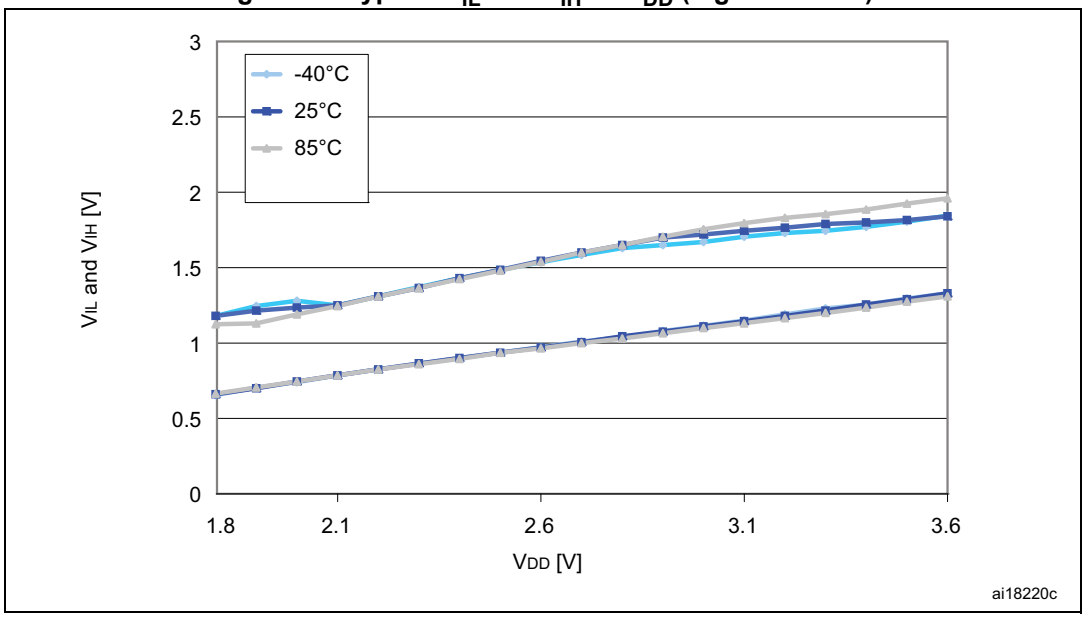
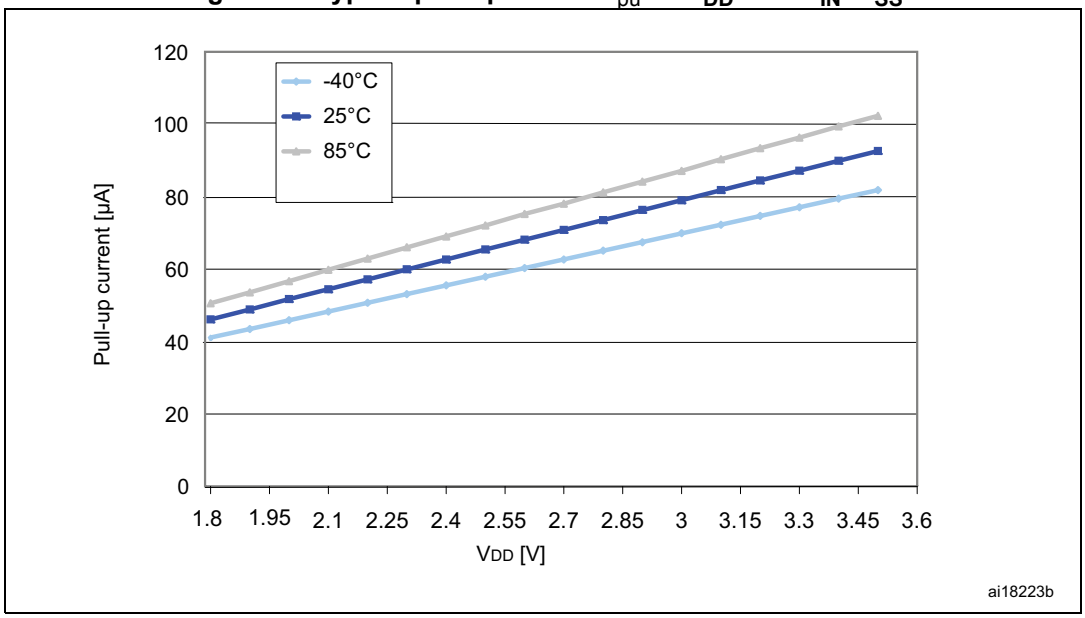


Figure 22. Typical pull-up current I_{pu} vs V_{DD} with $V_{IN}=V_{SS}$



9.3.9 LCD controller (STM8AL3Lxx only)

In the following table, data are guaranteed by design and are not tested in production.

Table 48. LCD characteristics

Symbol	Parameter	Min	Typ	Max.	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.7	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.8	-	
V_{LCD3}	LCD internal reference voltage 3	-	2.9	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.0	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.1	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.2	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.3	-	
C_{EXT}	V_{LCD} external capacitance	0.1	-	2	µF
I_{DD}	Supply current(1) at V_{DD} = 1.8 V	-	3	-	µA
	Supply current(1) at V_{DD} = 3 V	-	3	-	
R_{HN} (2)	High value resistive network (low drive)	-	6.6	-	MΩ
R_{LN} (3)	Low value resistive network (high drive)	-	360	-	kΩ
V_{33}	Segment/Common higher level voltage	-	-	V_{LCDx}	V
V_{23}	Segment/Common 2/3 level voltage	-	$2/3V_{LCDx}$	-	
V_{12}	Segment/Common 1/2 level voltage	-	$1/2V_{LCDx}$	-	
V_{13}	Segment/Common 1/3 level voltage	-	$1/3V_{LCDx}$	-	
V_0	Segment/Common lowest level voltage	0	-	-	

1. LCD enabled with 3 V internal booster (LCD_CR1 = 0x08), 1/4 duty, 1/3 bias, division ratio= 64, all pixels active, no LCD connected.
2. R_{HN} is the total high value resistive network.
3. R_{LN} is the total low value resistive network.

VLCD external capacitor (STM8AL3Lxx only)

The application can achieve a stabilized LCD reference voltage by connecting an external capacitor C_{EXT} to the V_{LCD} pin. C_{EXT} is specified in *Table 48*.

9.3.10 Embedded reference voltage

In the following table, data are based on characterization results, not tested in production, unless otherwise specified.

Table 56. ADC1 characteristics

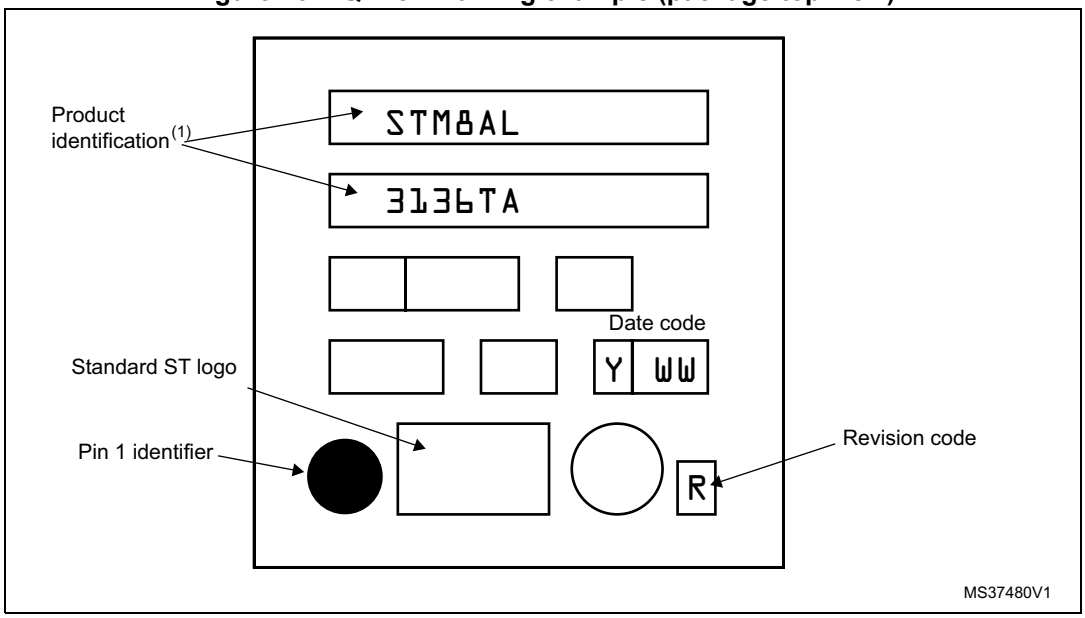
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	2.4 V ≤ V_{DDA} ≤ 3.6 V	2.4	-	V_{DDA}	V
		1.8 V ≤ V_{DDA} ≤ 2.4 V	V_{DDA}			
V_{REF-}	Lower reference voltage	-	V_{SSA}			
I_{VDDA}	Current on the V_{DDA} input pin	-	-	1000	1450	µA
I_{VREF+}	Current on the V_{REF+} input pin	-	-	400	700 (peak)(1)	
		-	-		450 (average)(1)	
V_{AIN}	Conversion voltage range	-	0(2)	-	V_{REF+}	-
T_A	Temperature range	-	-40	-	125	°C
R_{AIN}	External resistance on V_{AIN}	on PF0 fast channel	-	-	50(3)	kΩ
		on all other channels	-	-		
C_{ADC}	Internal sample and hold capacitor	on PF0 fast channel	-	16	-	pF
		on all other channels	-		-	
f_{ADC}	ADC sampling clock frequency	2.4 V ≤ V_{DDA} ≤ 3.6 V without zooming	0.320	-	16	MHz
		1.8 V ≤ V_{DDA} ≤ 2.4 V with zooming	0.320	-	8	
f_{CONV}	12-bit conversion rate	V_{AIN} on PF0 fast channel	-	-	1(4)(5)	
		V_{AIN} on all other channels	-	-	760(4)(5)	kHz
f_{TRIG}	External trigger frequency	-	-	-	t_{conv}	$1/f_{ADC}$
t_{LAT}	External trigger latency	-	-	-	3.5	$1/f_{SYSCLK}$

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

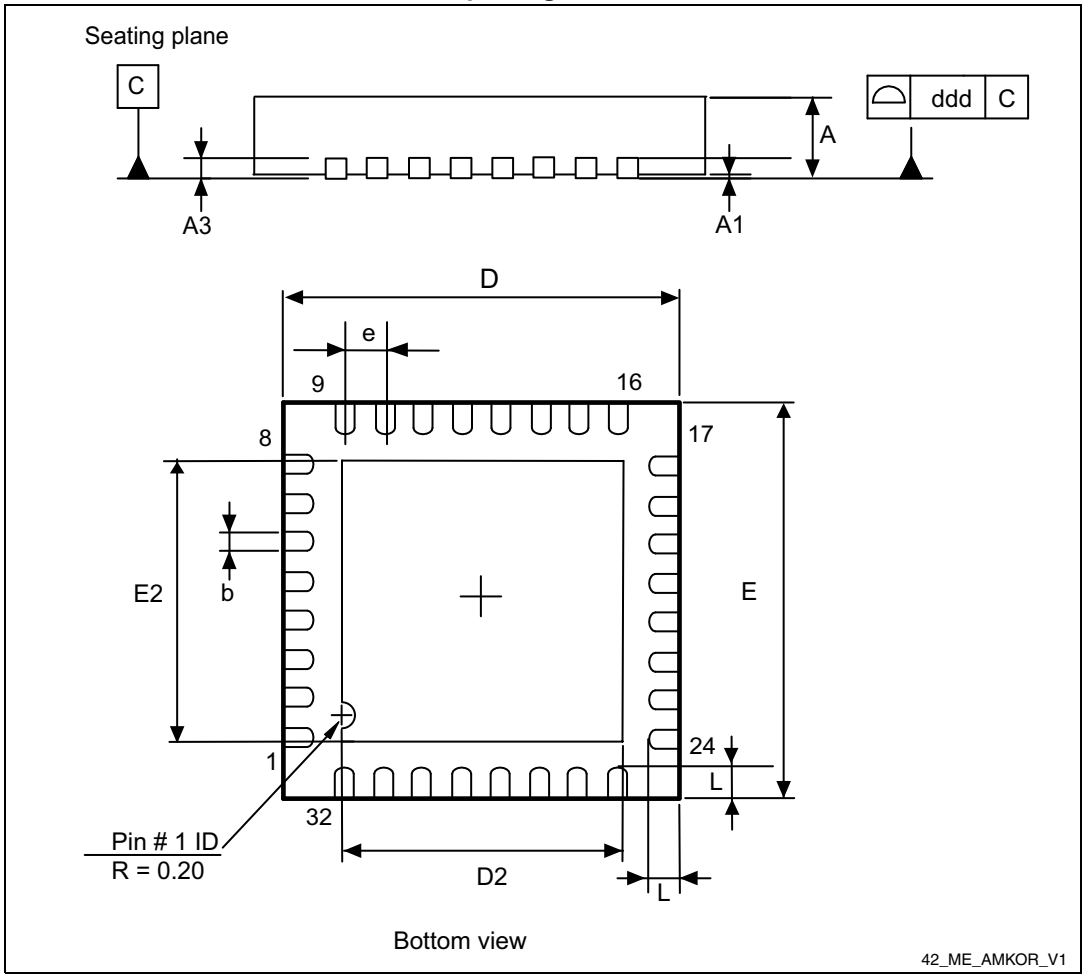
Figure 46. LQFP32 marking example (package top view)



1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

10.4 VFQFPN32 package information

Figure 47. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline



1. Drawing is not to scale.
2. There is an exposed die pad on the underside of the VQFPN package. It is recommended to connect and solder this backside pad to the PCB ground.

Table 69. Document revision history (continued)

Date	Revision	Changes
03-Mar-2014	5	Changed the document status to Datasheet - Production data to reflect the device maturity. Corrected the data memory size in the *Features*. Updated the package assignment in *Table 2: Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x low-power device features and peripheral counts*
13-May-2015	6	Updated: – the product names in the document headers and on the cover page, – *Section 1: Introduction*, – the captions of *Figure 3: STM8AL31x8T 48-pin pinout (without LCD)*, *Figure 4: STM8AL3Lx8T 48-pin pinout (with LCD)*, *Figure 5: STM8AL31x6T 32-pin pinout (without LCD)*, *Figure 6: STM8AL3Lx6T 32-pin pinout (with LCD)*, – *Table 6: Flash and RAM boundary addresses*, – I_{LEAK_HSE} maximum value in *Table 32: HSE oscillator characteristics*,I_{LEAK_LSE} maximum value in *Table 33: LSE oscillator characteristics*, – *Table 54*, *Table 57*, *Table 58*, *Table 59* with a footnote for Max values not tested in production, – *Section 9.3.15: EMC characteristics*, – *Section 10.2: LQFP48 package information*, – *Section 10.3: LQFP32 package information*, – *Figure 50: Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x ordering information scheme*. Added: – *Figure 43: LQFP48 marking example (package top view)*, – *Figure 46: LQFP32 marking example (package top view)*. Moved *Section 10.5: Thermal characteristics* to *Section 10: Package information*.