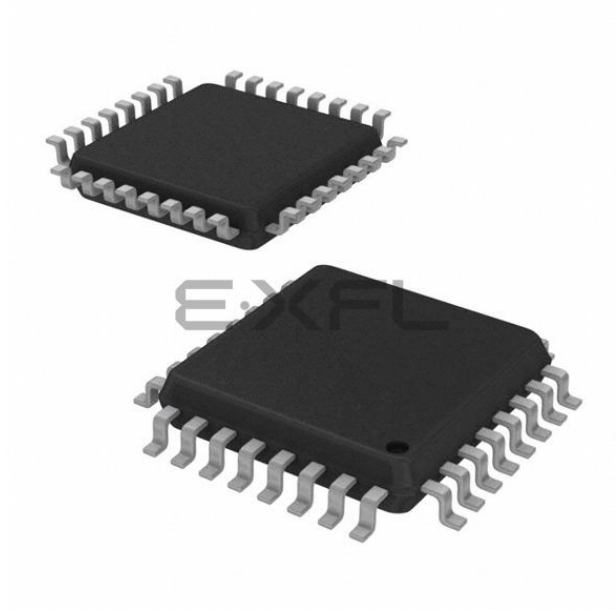


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | STM8 |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 29 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 21x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3l46tcy |

- Development support
  - Fast on-chip programming and non intrusive debugging with SWIM
  - Bootloader using USART
- 96-bit unique ID

**Table 1. Device summary**

| Reference | Part number |
|---|---|
| STM8AL313x/4x/6x (without LCD) | STM8AL3136, STM8AL3138, STM8AL3146, STM8AL3148, STM8AL3166, STM8AL3168 |
| STM8AL3L4x/6x (with LCD) | STM8AL3L46, STM8AL3L48, STM8AL3L66, STM8AL3L68 |

# List of tables

# 1 Introduction

This document describes the features, pinout, mechanical data and ordering information of the medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x devices (microcontrollers with up to 32-Kbyte Flash memory density). These devices are referred to as medium-density devices in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031) and in STM8L and STM8AL Flash programming manual (PM0054).

For more details on the whole STMicroelectronics ultra-low-power family please refer to *Section 3: Functional overview on page 13*.

For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).

For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

*Note: The medium-density devices provide the following benefits:*

- Integrated system
  - Up to 32 Kbytes of medium-density embedded Flash program memory
  - 1 Kbytes of data EEPROM
  - Internal high speed and low-power low speed RC.
  - Embedded reset
- Ultra-low power consumption
  - 195 µA/MHZ + 440 µA (consumption)
  - 0.9 µA with LSI in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for Low power wait mode and Low power run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access.
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Wide choice of development tools

All devices offer 12-bit ADC, DAC, two comparators, Real-time clock three 16-bit timers, one 8-bit timer as well as standard communication interface such as SPI, I2C and USART. A 4x28-segment LCD is available on the medium-density STM8AL3Lxx line. *Table 2: Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x low-power device features and peripheral counts* and *Section 3: Functional overview* give an overview of the complete range of peripherals proposed in this family.

*Figure 1* shows the general block diagram of the device family.

## 3.2 Central processing unit STM8

### 3.2.1 Advanced STM8 core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains six internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

#### Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16 Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

#### Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

#### Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

### 3.2.2 Interrupt controller

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x feature a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts

## 3.13 Timers

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x devices contain one advanced control timer (TIM1), two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

*Table 3* compares the features of the advanced control, general-purpose and basic timers.

**Table 3. Timer feature comparison**

| Timer | Counter resolution | Counter type | Prescaler factor | DMA1 request generation | Capture/compare channels | Complementary outputs |
|---|---|---|---|---|---|---|
| TIM1 | 16-bit | up/down | Any integer from 1 to 65536 | Yes | 3 + 1 | 3 |
| TIM2 | | | Any power of 2 from 1 to 128 | | 2 | None |
| TIM3 | | | | | | |
| TIM4 | 8-bit | up | Any power of 2 from 1 to 32768 | | 0 | |

### 3.13.1 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down auto reload counter with 16-bit prescaler
- Three independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output.
- One additional capture/compare channel which is not connected to an external I/O
- Synchronization module to control the timer with external signals
- Break input to force timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

### 3.13.2 16-bit general purpose timers

- 16-bit auto reload (AR) up/down-counter
- 7-bit prescaler adjustable to fixed power of 2 ratios (1…128)
- Two individually configurable capture/compare channels
- PWM mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

**Table 5. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x pin description (continued)**

| Pin number | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48 | VFQFPN32 | LQFP32 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 38 | 26 | 26 | PC1(5)/I2C1_SCL | I/O | FT | X | - | X | - | T(7) | | Port C1 | I2C1 clock |
| 41 | 27 | 27 | PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ COMP1_INP/VREFINT | I/O | TT(3) | X | X | X | HS | X | X | Port C2 | USART1 receive / LCD segment 22 / ADC1_IN6 / Comparator 1 positive input / Internal voltage reference output |
| 42 | 28 | 28 | PC3/USART1_TX/ LCD_SEG23(2)/ ADC1_IN5/COMP1_INP/ COMP2_INM | I/O | TT(3) | X | X | X | HS | X | X | Port C3 | USART1 transmit / LCD segment 23 / ADC1_IN5 / Comparator 1 positive input / Comparator 2 negative input |
| 43 | 29 | 29 | PC4/USART1_CK/ I2C1_SMB/CCO/ LCD_SEG24(2)/ ADC1_IN4/COMP2_INM/ COMP1_INP | I/O | TT(3) | X | X | X | HS | X | X | Port C4 | USART1 synchronous clock / I2C1_SMB / Configurable clock output / LCD segment 24 / ADC1_IN4 / Comparator 2 negative input / Comparator 1 positive input |
| 44 | 30 | 30 | PC5/OSC32_IN /*[SPI1_NSS]*(4)/ *[USART1_TX]*(4) | I/O | - | X | X | X | HS | X | X | Port C5 | LSE oscillator input / *[SPI1 master/slave select] / [USART1 transmit]* |
| 45 | 31 | 31 | PC6/OSC32_OUT/ *[SPI1_SCK]*(4)/ *[USART1_RX]*(4) | I/O | - | X | X | X | HS | X | X | Port C6 | LSE oscillator output / *[SPI1 clock] / [USART1 receive]* |
| 46 | - | - | PC7/LCD_SEG25(2)/ ADC1_IN3/COMP2_INM/ COMP1_INP | I/O | TT(3) | X | X | X | HS | X | X | Port C7 | LCD segment 25 /ADC1_IN3/ Comparator negative input / Comparator 1 positive input |

**Table 6. Flash and RAM boundary addresses**

| Memory area | Size | Start address | End address |
|---|---|---|---|
| RAM | 2 Kbyte | 0x00 0000 | 0x00 07FF |
| Flash program memory | 8 Kbyte | 0x00 8000 | 0x00 9FFF |
| | 16 Kbyte | | 0x00 BFFF |
| | 32 Kbyte | | |

## 5.2 Register map

**Table 7. Factory conversion registers**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 4910 | - | VREFINT_Factory_CONV(1) | Internal reference voltage factory conversion | 0xXX |
| 0x00 4911 | - | TS_Factory_CONV_V125(2) | Temperature sensor output voltage | 0xXX |

1. The VREFINT_Factory_CONV byte represents the 8 LSB of the result of the VREFINT 12-bit ADC conversion performed in factory. The MSB have a fixed value: 0x6.
2. The TS_Factory_CONV_V125 byte represents the 8 LSB of the result of the V125 12-bit ADC conversion performed in factory. The 2 MSB have a fixed value: 0x3.

**Table 8. I/O port hardware register map**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5000 | Port A | PA_ODR | Port A data output latch register | 0x00 |
| 0x00 5001 | | PA_IDR | Port A input pin value register | 0xXX |
| 0x00 5002 | | PA_DDR | Port A data direction register | 0x00 |
| 0x00 5003 | | PA_CR1 | Port A control register 1 | 0x01 |
| 0x00 5004 | | PA_CR2 | Port A control register 2 | 0x00 |
| 0x00 5005 | Port B | PB_ODR | Port B data output latch register | 0x00 |
| 0x00 5006 | | PB_IDR | Port B input pin value register | 0xXX |
| 0x00 5007 | | PB_DDR | Port B data direction register | 0x00 |
| 0x00 5008 | | PB_CR1 | Port B control register 1 | 0x00 |
| 0x00 5009 | | PB_CR2 | Port B control register 2 | 0x00 |
| 0x00 500A | Port C | PC_ODR | Port C data output latch register | 0x00 |
| 0x00 500B | | PB_IDR | Port C input pin value register | 0xXX |
| 0x00 500C | | PC_DDR | Port C data direction register | 0x00 |
| 0x00 500D | | PC_CR1 | Port C control register 1 | 0x00 |
| 0x00 500E | | PC_CR2 | Port C control register 2 | 0x00 |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 507F | DMA1 | DMA1_C1CR | DMA1 channel 1 configuration register | 0x00 |
| 0x00 5080 | | DMA1_C1SPR | DMA1 channel 1 status & priority register | 0x00 |
| 0x00 5081 | | DMA1_C1NDTR | DMA1 number of data to transfer register (channel 1) | 0x00 |
| 0x00 5082 | | DMA1_C1PARH | DMA1 peripheral address high register (channel 1) | 0x52 |
| 0x00 5083 | | DMA1_C1PARL | DMA1 peripheral address low register (channel 1) | 0x00 |
| 0x00 5084 | | Reserved area (1 byte) | | |
| 0x00 5085 | | DMA1_C1M0ARH | DMA1 memory 0 address high register (channel 1) | 0x00 |
| 0x00 5086 | | DMA1_C1M0ARL | DMA1 memory 0 address low register (channel 1) | 0x00 |
| 0x00 5087<br>0x00 5088 | | Reserved area (2 bytes) | | |
| 0x00 5089 | | DMA1_C2CR | DMA1 channel 2 configuration register | 0x00 |
| 0x00 508A | | DMA1_C2SPR | DMA1 channel 2 status & priority register | 0x00 |
| 0x00 508B | | DMA1_C2NDTR | DMA1 number of data to transfer register (channel 2) | 0x00 |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 540C | LCD | LCD_RAM0 | LCD display memory 0 | 0x00 |
| 0x00 540D | | LCD_RAM1 | LCD display memory 1 | 0x00 |
| 0x00 540E | | LCD_RAM2 | LCD display memory 2 | 0x00 |
| 0x00 540F | | LCD_RAM3 | LCD display memory 3 | 0x00 |
| 0x00 5410 | | LCD_RAM4 | LCD display memory 4 | 0x00 |
| 0x00 5411 | | LCD_RAM5 | LCD display memory 5 | 0x00 |
| 0x00 5412 | | LCD_RAM6 | LCD display memory 6 | 0x00 |
| 0x00 5413 | | LCD_RAM7 | LCD display memory 7 | 0x00 |
| 0x00 5414 | | LCD_RAM8 | LCD display memory 8 | 0x00 |
| 0x00 5415 | | LCD_RAM9 | LCD display memory 9 | 0x00 |
| 0x00 5416 | | LCD_RAM10 | LCD display memory 10 | 0x00 |
| 0x00 5417 | | LCD_RAM11 | LCD display memory 11 | 0x00 |
| 0x00 5418 | | LCD_RAM12 | LCD display memory 12 | 0x00 |
| 0x00 5419 | | LCD_RAM13 | LCD display memory 13 | 0x00 |
| 0x00 541A to 0x00 542F | Reserved area (22 bytes) | | | |
| 0x00 5430 | RI | Reserved area (1 byte) | | 0x00 |
| 0x00 5431 | | RI_ICR1 | Timer input capture routing register 1 | 0x00 |
| 0x00 5432 | | RI_ICR2 | Timer input capture routing register 2 | 0x00 |
| 0x00 5433 | | RI_IOIR1 | I/O input register 1 | undefined |
| 0x00 5434 | | RI_IOIR2 | I/O input register 2 | undefined |
| 0x00 5435 | | RI_IOIR3 | I/O input register 3 | undefined |
| 0x00 5436 | | RI_IOCMR1 | I/O control mode register 1 | 0x00 |
| 0x00 5437 | | RI_IOCMR2 | I/O control mode register 2 | 0x00 |
| 0x00 5438 | | RI_IOCMR3 | I/O control mode register 3 | 0x00 |
| 0x00 5439 | | RI_IOSR1 | I/O switch register 1 | 0x00 |
| 0x00 543A | | RI_IOSR2 | I/O switch register 2 | 0x00 |
| 0x00 543B | | RI_IOSR3 | I/O switch register 3 | 0x00 |
| 0x00 543C | | RI_IOGCR | I/O group control register | 0x3F |
| 0x00 543D | | RI_ASCR1 | Analog switch register 1 | 0x00 |
| 0x00 543E | | RI_ASCR2 | Analog switch register 2 | 0x00 |
| 0x00 543F | | RI_RCR | Resistor control register 1 | 0x00 |

# 8 Unique ID

The devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single bytes and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

**Table 14. Unique ID registers (96 bits)**

| Address | Content description | Unique ID bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x4926 | X co-ordinate on the wafer | U_ID[7:0] | | | | | | | |
| 0x4927 | | U_ID[15:8] | | | | | | | |
| 0x4928 | Y co-ordinate on the wafer | U_ID[23:16] | | | | | | | |
| 0x4929 | | U_ID[31:24] | | | | | | | |
| 0x492A | Wafer number | U_ID[39:32] | | | | | | | |
| 0x492B | Lot number | U_ID[47:40] | | | | | | | |
| 0x492C | | U_ID[55:48] | | | | | | | |
| 0x492D | | U_ID[63:56] | | | | | | | |
| 0x492E | | U_ID[71:64] | | | | | | | |
| 0x492F | | U_ID[79:72] | | | | | | | |
| 0x4930 | | U_ID[87:80] | | | | | | | |
| 0x4931 | | U_ID[95:88] | | | | | | | |

**Table 29. Current consumption under external reset**

| Symbol | Parameter | Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $I_{DD(RST)}$ | Supply current under external reset (1) | All pins are externally tied to $V_{DD}$ | $V_{DD}$ = 1.8 V | 48 | µA |
| | | | $V_{DD}$ = 3 V | 76 | |
| | | | $V_{DD}$ = 3.6 V | 91 | |

1. All pins except PA0, PB0 and PB4 are floating under reset. PA0, PB0 and PB4 are configured with pull-up under reset.

## 9.3.4 Clock and timing characteristics

### HSE external clock (HSEBYP = 1 in CLK_ECKCR)

Subject to general operating conditions for $V_{DD}$ and $T_A$.

**Table 30. HSE external clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE\_ext}$ | External clock source frequency | - | 1(1) | - | 16(1) | MHz |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | | 0.7 x $V_{DD}$ | - | $V_{DD}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | | $V_{SS}$ | - | 0.3 x $V_{DD}$ | |
| $C_{in(HSE)}$ | OSC_IN input capacitance | - | - | 2.6 | - | pF |
| $I_{LEAK\_HSE}$ | OSC_IN input leakage current | $V_{SS} < V_{IN} < V_{DD}$ | - | - | ±500 | nA |

1. Guaranteed by design.

### LSE external clock (LSEBYP=1 in CLK_ECKCR)

Subject to general operating conditions for $V_{DD}$ and $T_A$.

**Table 31. LSE external clock characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{LSE\_ext}$ | External clock source frequency | - | 32.768 | - | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | 0.7 x $V_{DD}$(1) | - | $V_{DD}$(1) | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | $V_{SS}$(1) | - | 0.3 x $V_{DD}$(1) | |
| $C_{in(LSE)}$ | OSC32_IN input capacitance | - | 0.6 | - | pF |
| $I_{LEAK\_LSE}$ | OSC32_IN input leakage current | - | | ±500 | nA |

1. Guaranteed by characterization results.

**Table 40. I/O current injection susceptibility**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on true open-drain pins (PC0 and PC1) | -5 | +0 | mA |
| | Injected current on all five-volt tolerant (FT) pins | -5 | +0 | |
| | Injected current on all 3.6 V tolerant (TT) pins | -5 | +0 | |
| | Injected current on any other pin | -5 | +5 | |

## 9.3.7 I/O port pin characteristics

### General characteristics

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

**Table 41. I/O static characteristics**

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage | Input voltage on all pins | $V_{SS}$-0.3 | - | 0.3 x $V_{DD}$ | V |
| $V_{IH}$ | Input high level voltage | Input voltage on true open-drain pins (PC0 and PC1) with $V_{DD}$ < 2 V | 0.70 x $V_{DD}$ | - | 5.2(2) | |
| | | Input voltage on true open-drain pins (PC0 and PC1) with $V_{DD}$ ≥ 2 V | | - | 5.5(2) | |
| | | Input voltage on five-volt tolerant (FT) pins (PA7 and PE0) with $V_{DD}$ < 2 V | 0.70 x $V_{DD}$ | - | 5.2(2) | |
| | | Input voltage on five-volt tolerant (FT) pins (PA7 and PE0) with $V_{DD}$ ≥ 2 V | | - | 5.5(2) | |
| | | Input voltage on 3.6 V tolerant (TT) pins | | - | 3.6(2) | |
| | | Input voltage on any other pin | 0.70 x $V_{DD}$ | - | $V_{DD}$+0.3(2) | |
| $V_{hys}$ | Schmitt trigger voltage hysteresis (3) | I/Os | - | 200 | - | mV |
| | | True open drain I/Os | - | 200 | - | |
| $I_{lkg}$ | Input leakage current (4) | $V_{SS} \le V_{IN} \le V_{DD}$ High sink I/Os | - | - | 50 | nA |
| | | $V_{SS} \le V_{IN} \le V_{DD}$ True open drain I/Os | - | - | 200 | |
| | | $V_{SS} \le V_{IN} \le V_{DD}$ PA0 with high sink LED driver capability | - | - | 200 | |

**Figure 23. Typ. $V_{OL}$ @ $V_{DD}$ = 3.0 V (high sink ports)**

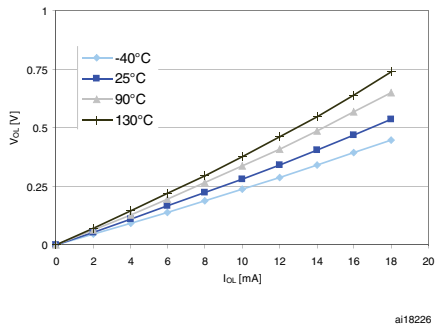



**Figure 24. Typ. $V_{OL}$ @ $V_{DD}$ = 1.8 V (high sink ports)**

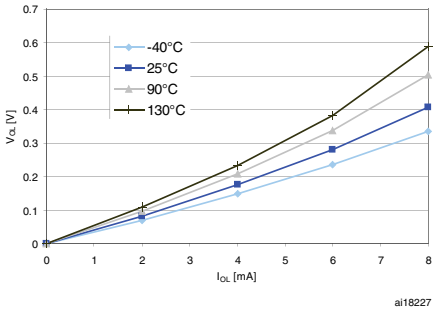



**Figure 25. Typ. $V_{OL}$ @ $V_{DD}$ = 3.0 V (true open drain ports)**

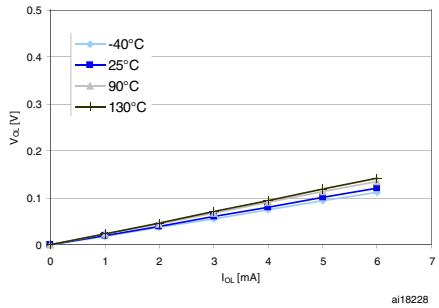



**Figure 26. Typ. $V_{OL}$ @ $V_{DD}$ = 1.8 V (true open drain ports)**

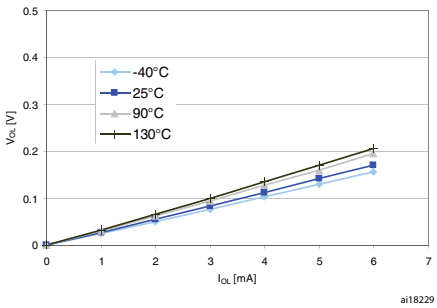



**Figure 27. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 3.0 V (high sink ports)**

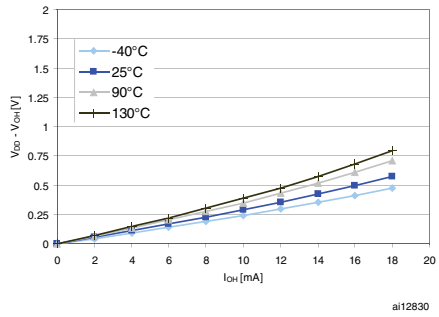



**Figure 28. Typ. $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 1.8 V (high sink ports)**

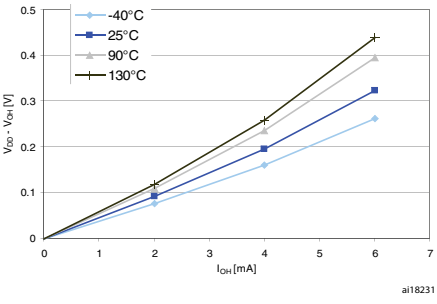


**Table 50. TS characteristics (continued)**

| Symbol | Parameter | Min | Typ | Max. | Unit |
|---|---|---|---|---|---|
| $T_{START}$(3) | Temperature sensor startup time | - | - | 10(2) | µs |
| $T_{S\_TEMP}$ | ADC sampling time when reading the temperature sensor | - | 5 | 10(2) | |

1. Tested in production at $V_{DD}$ = 3 V ±10 mV. The 8 LSB of the $V_{125}$ ADC conversion result are stored in the TS_Factory_CONV_V125 byte.
2. Guaranteed by design.
3. Defined for ADC output reaching its final value ±1/2LSB.

### 9.3.12 Comparator characteristics

In the following table, data are guaranteed by design, not tested in production, unless otherwise specified.

**Table 51. Comparator 1 characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | 1.65 | - | 3.6(1) | V |
| $T_A$ | Temperature range | -40 | - | 125(1) | °C |
| $R_{400K}$ | $R_{400K}$ value | 300 | 400 | 500(1) | kΩ |
| $R_{10K}$ | $R_{10K}$ value | 7.5 | 10 | 12.5(1) | |
| $V_{IN}$ | Comparator input voltage range | 0.6 | - | $V_{DDA}$(1) | V |
| $V_{REFINT}$ | Internal reference voltage | 1.202 | 1.224 | 1.242 | |
| $t_{START}$ | Startup time after enable | - | 7 | 10(1) | µs |
| $t_d$ | Propagation delay(2) | - | 3 | 10(1) | |
| $V_{offset}$ | Comparator offset error | - | ±3 | ±10(1) | mV |
| $I_{CMP1}$ | Consumption(3) | - | 160 | 260(1) | nA |

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

In the following table, data are guaranteed by design, not tested in production unless otherwise specified.

**Table 52. Comparator 2 characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 1.65 | - | 3.6 | V |
| $T_A$ | Temperature range | - | -40 | - | 125 | °C |
| $V_{IN}$ | Comparator 2 input voltage range | - | 0 | - | $V_{DDA}$ | V |
| $t_{START}$ | Comparator startup time | Fast mode | - | 15 | 20 | µs |
| | | Slow mode | - | 20 | 25 | |
| $t_{d\ slow}$ | Propagation delay in slow mode(2) | 1.65 V ≤ $V_{DDA}$ ≤ 2.7 V | - | 1.8 | 3.5 | |
| | | 2.7 V ≤ $V_{DDA}$ ≤ 3.6 V | | 2.5 | 6 | |
| $t_{d\ fast}$ | Propagation delay in fast mode(2) | 1.65 V ≤ $V_{DDA}$ ≤ 2.7 V | - | 0.8 | 2 | |
| | | 2.7 V ≤ $V_{DDA}$ ≤ 3.6 V | | 1.2 | 4 | |
| $V_{offset}$ | Comparator offset error | - | - | ±4 | ±20 | mV |
| $I_{COMP2}$ | Current consumption(3) | Fast mode | - | 3.5 | 5 | µA |
| | | Slow mode | | 0.5 | 2 | |

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

### 9.3.13 12-bit DAC characteristics

In the following table, data are guaranteed by design, not tested in production.

**Table 53. DAC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 1.8 | - | 3.6 | V |
| $V_{REF+}$ | Reference supply voltage | - | 1.8 | - | $V_{DDA}$ | |

In the following three tables, data are guaranteed by characterization result, not tested in production.

**Table 57. ADC1 accuracy with $V_{DDA}$ = 2.5 V to 3.3 V**

| Symbol | Parameter | Conditions | Typ. | Max(1) | Unit |
|---|---|---|---|---|---|
| DNL | Differential non linearity | $f_{ADC}$ = 16 MHz | 1 | 1.6 | LSB |
| | | $f_{ADC}$ = 8 MHz | 1 | 1.6 | |
| | | $f_{ADC}$ = 4 MHz | 1 | 1.5 | |
| INL | Integral non linearity | $f_{ADC}$ = 16 MHz | 1.2 | 2 | |
| | | $f_{ADC}$ = 8 MHz | 1.2 | 1.8 | |
| | | $f_{ADC}$ = 4 MHz | 1.2 | 1.7 | |
| TUE | Total unadjusted error | $f_{ADC}$ = 16 MHz | 2.2 | 3.0 | |
| | | $f_{ADC}$ = 8 MHz | 1.8 | 2.5 | |
| | | $f_{ADC}$ = 4 MHz | 1.8 | 2.3 | |
| Offset | Offset error | $f_{ADC}$ = 16 MHz | 1.5 | 2 | LSB |
| | | $f_{ADC}$ = 8 MHz | 1 | 1.5 | |
| | | $f_{ADC}$ = 4 MHz | 0.7 | 1.2 | |
| Gain | Gain error | $f_{ADC}$ = 16 MHz | 1 | 1.5 | |
| | | $f_{ADC}$ = 8 MHz | | | |
| | | $f_{ADC}$ = 4 MHz | | | |

1. Not tested in production.

**Table 58. ADC1 accuracy with $V_{DDA}$ = 2.4 V to 3.6 V**

| Symbol | Parameter | Typ. | Max(1) | Unit |
|---|---|---|---|---|
| DNL | Differential non linearity | 1 | 2 | LSB |
| INL | Integral non linearity | 1.7 | 3 | |
| TUE | Total unadjusted error | 2 | 4 | |
| Offset | Offset error | 1 | 2 | |
| Gain | Gain error | 1.5 | 3 | |

1. Not tested in production.

**Figure 38. Maximum dynamic current consumption on $V_{REF+}$ supply pin during ADC conversion**

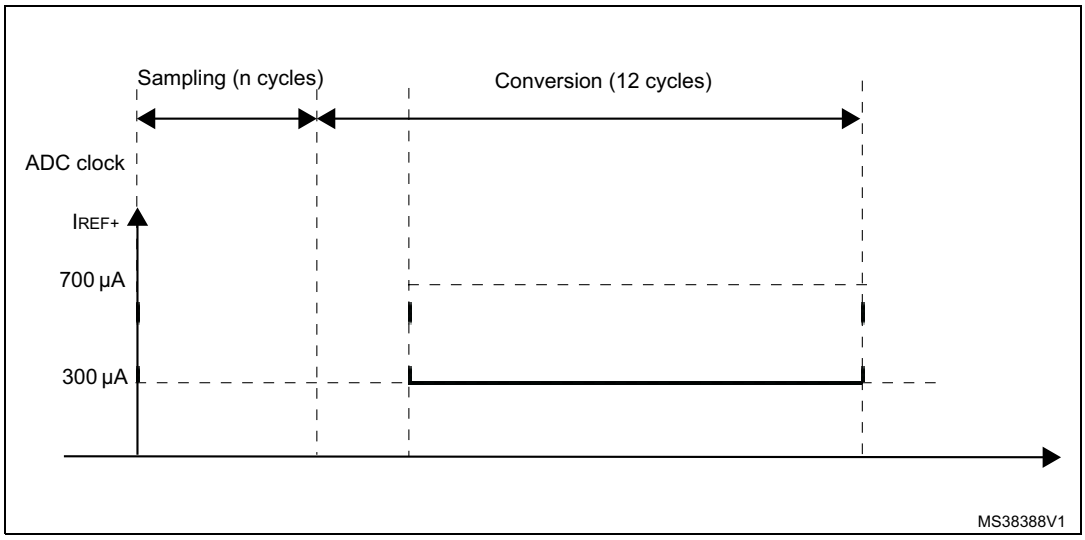



**Table 60. $R_{AIN}$ max for $f_{ADC}$ = 16 MHz(1)**

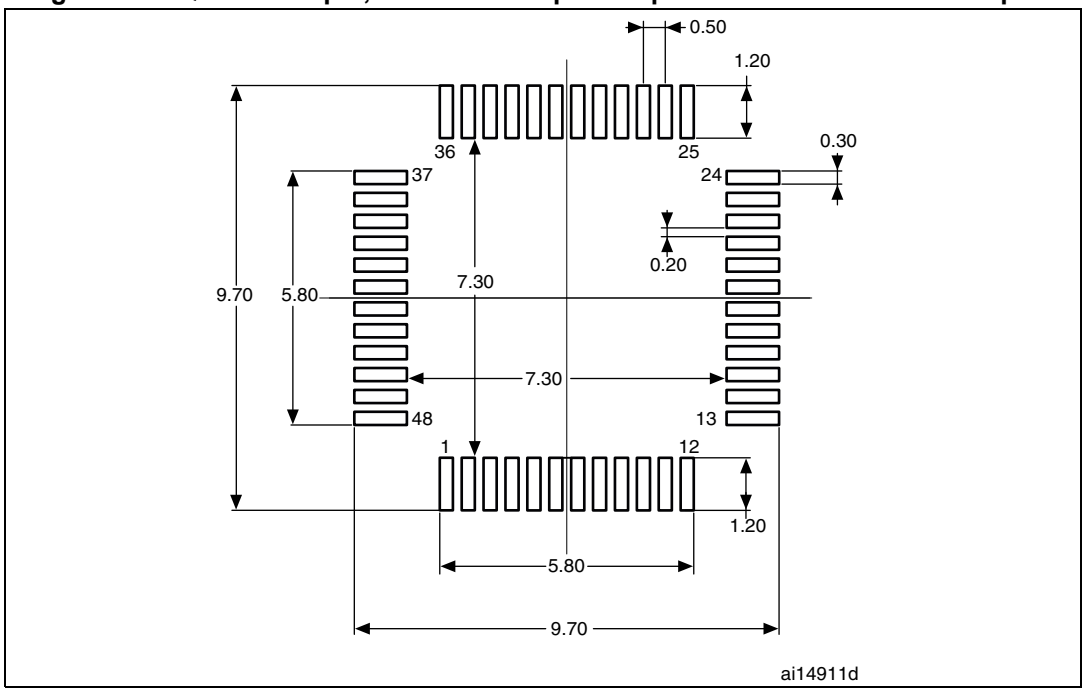
| Ts (cycles) | Ts (µs) | $R_{AIN}$ max (kohm) | | | |
|---|---|---|---|---|---|
| | | Slow channels | | Fast channels | |
| | | 2.4 V < $V_{DDA}$ < 3.6 V | 1.8 V < $V_{DDA}$ < 2.4 V | 2.4 V < $V_{DDA}$ < 3.3 V | 1.8 V < $V_{DDA}$ < 2.4 V |
| 4 | 0.25 | Not allowed | Not allowed | 0.7 | Not allowed |
| 9 | 0.5625 | 0.8 | Not allowed | 2.0 | 1.0 |
| 16 | 1 | 2.0 | 0.8 | 4.0 | 3.0 |
| 24 | 1.5 | 3.0 | 1.8 | 6.0 | 4.5 |
| 48 | 3 | 6.8 | 4.0 | 15.0 | 10.0 |
| 96 | 6 | 15.0 | 10.0 | 30.0 | 20.0 |
| 192 | 12 | 32.0 | 25.0 | 50.0 | 40.0 |
| 384 | 24 | 50.0 | 50.0 | 50.0 | 50.0 |

1. Guaranteed by design.

### General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 39* or *Figure 40*, depending on whether $V_{REF+}$ is connected to $V_{DDA}$ or not. Good quality ceramic 10 nF capacitors should be used. They should be placed as close as possible to the chip.

**Figure 42. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint**

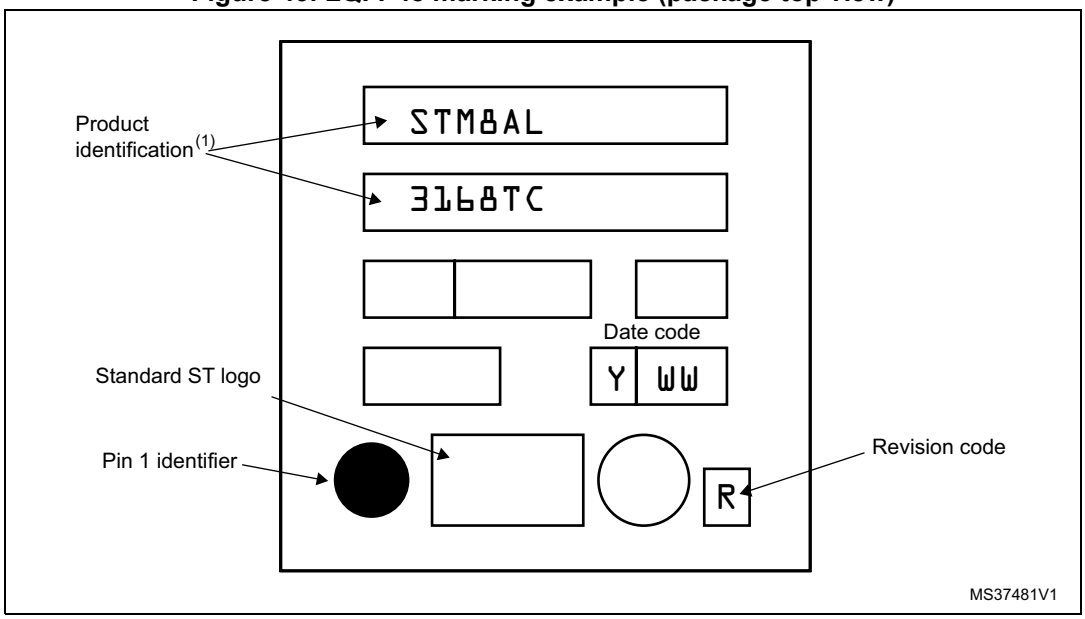



1. Dimensions are expressed in millimeters.

## Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 43. LQFP48 marking example (package top view)**




1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.