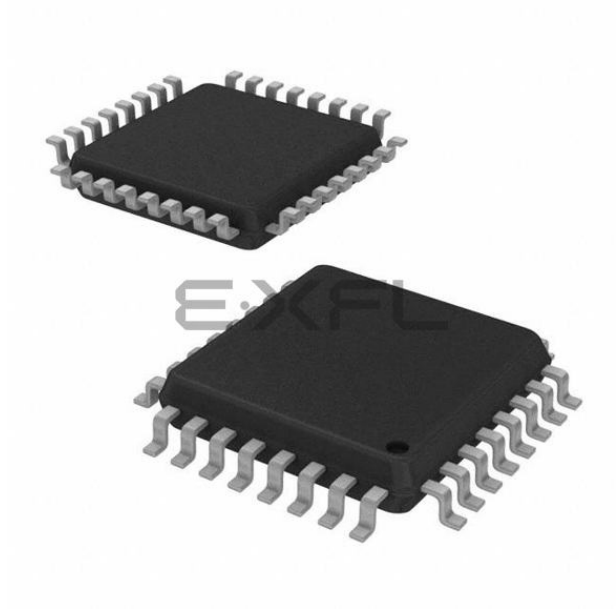

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 21x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3l66tcy

3.1 Low-power modes

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x devices support five low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Wait mode**: CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt, event or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode). Wait consumption: refer to *Table 22*.
- **Low power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash and data EEPROM are stopped and the voltage regulator is configured in ultra-low-power mode. The microcontroller enters Low power run mode by software and can exit from this mode by software or by a reset.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power run mode consumption: refer to *Table 23*.
- **Low power wait mode:** This mode is entered when executing a Wait for event in Low power run mode. It is similar to Low power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low power run mode.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power wait mode consumption: refer to *Table 24*.
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset. Active-halt consumption: refer to *Table 25* and *Table 26*.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 µs. Halt consumption: refer to *Table 27*.

3.16.2 I²C

The I^2C bus interface (I^2C1) provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz
- 7-bit and 10-bit addressing modes
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: I^2C1 can be served by the DMA1 Controller.

3.16.3 USART

The USART interface (USART1) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- SmartCard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Note: USART1 can be served by the DMA1 Controller.

USART1 can be used to implement LIN slave communication, with LIN Break detection on the framing error flag (FE in USART_SR register) with a value of 0 in the USART data register (USART_DR).

3.17 Infrared (IR) interface

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.18 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment.
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Table 5. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48	VFQFPN32	LQFP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
28	-	-	PB4[6]/*[SPI1_NSS]*[4]/ LCD_SEG14[2]/ ADC1_IN14/COMP1_INP	I/O	TT[3]	X[6]	X[6]	X	HS	X	X	Port B4	*[SPI1 master/slave select]* / LCD segment 14 / ADC1_IN14 / Comparator 1 positive input
-	17	17	PB4[6]/*[SPI1_NSS]*[4]/ LCD_SEG14[2]/ ADC1_IN14/ COMP1_INP/DAC_OUT	I/O	TT[3]	X[6]	X[6]	X	HS	X	X	Port B4	*[SPI1 master/slave select]* / LCD segment 14 / ADC1_IN14 / DAC output / Comparator 1 positive input
29	-	-	PB5/*[SPI1_SCK]*[4]/ LCD_SEG15[2]/ ADC1_IN13/COMP1_INP	I/O	TT[3]	X	X	X	HS	X	X	Port B5	*[SPI1 clock]* / LCD segment 15 / ADC1_IN13 / Comparator 1 positive input
-	18	18	PB5/*[SPI1_SCK]*[4]/ LCD_SEG15[2]/ ADC1_IN13/DAC_OUT/ COMP1_INP	I/O	TT[3]	X	X	X	HS	X	X	Port B5	*[SPI1 clock]* / LCD segment 15 / ADC1_IN13 / DAC output/ Comparator 1 positive input
30	-	-	PB6/[*SPI1_MOSI]*[4]/ LCD_SEG16[2]/ ADC1_IN12/COMP1_INP	I/O	TT[3]	X	X	X	HS	X	X	Port B6	*[SPI1 master out/slave in]*/ LCD segment 16 / ADC1_IN12 / Comparator 1 positive input
-	19	19	PB6/*[SPI1_MOSI]*[4]/ LCD_SEG16[2]/ ADC1_IN12/COMP1_INP /DAC_OUT	I/O	TT[3]	X	X	X	HS	X	X	Port B6	*[SPI1 master out]*/ slave in / LCD segment 16 / ADC1_IN12 / DAC output / Comparator 1 positive input
31	20	20	PB7/*[SPI1_MISO]*[4]/ LCD_SEG17[2]/ ADC1_IN11/COMP1_INP	I/O	TT[3]	X	X	X	HS	X	X	Port B7	*[SPI1 master in- slave out]* / LCD segment 17 / ADC1_IN11 / Comparator 1 positive input
37	25	25	PC0[5]/I2C1_SDA	I/O	FT	X	-	X		T[7]		Port C0	I2C1 data

Table 5. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48	VFQFPN32	LQFP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
38	26	26	PC1(5)/I2C1_SCL	I/O	FT	X	-	X	-	T(7)		Port C1	I2C1 clock
41	27	27	PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ COMP1_INP/VREFINT	I/O	TT(3)	X	X	X	HS	X	X	Port C2	USART1 receive / LCD segment 22 / ADC1_IN6 / Comparator 1 positive input / Internal voltage reference output
42	28	28	PC3/USART1_TX/ LCD_SEG23(2)/ ADC1_IN5/COMP1_INP/ COMP2_INM	I/O	TT(3)	X	X	X	HS	X	X	Port C3	USART1 transmit / LCD segment 23 / ADC1_IN5 / Comparator 1 positive input / Comparator 2 negative input
43	29	29	PC4/USART1_CK/ I2C1_SMB/CCO/ LCD_SEG24(2)/ ADC1_IN4/COMP2_INM/ COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port C4	USART1 synchronous clock / I2C1_SMB / Configurable clock output / LCD segment 24 / ADC1_IN4 / Comparator 2 negative input / Comparator 1 positive input
44	30	30	PC5/OSC32_IN /*[SPI1_NSS]*(4)/ *[USART1_TX]*(4)	I/O	-	X	X	X	HS	X	X	Port C5	LSE oscillator input / *[SPI1 master/slave select] / [USART1 transmit]*
45	31	31	PC6/OSC32_OUT/ *[SPI1_SCK]*(4)/ *[USART1_RX]*(4)	I/O	-	X	X	X	HS	X	X	Port C6	LSE oscillator output / *[SPI1 clock] / [USART1 receive]*
46	-	-	PC7/LCD_SEG25(2)/ ADC1_IN3/COMP2_INM/ COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port C7	LCD segment 25 /ADC1_IN3/ Comparator negative input / Comparator 1 positive input

Table 5. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x pin description (continued)

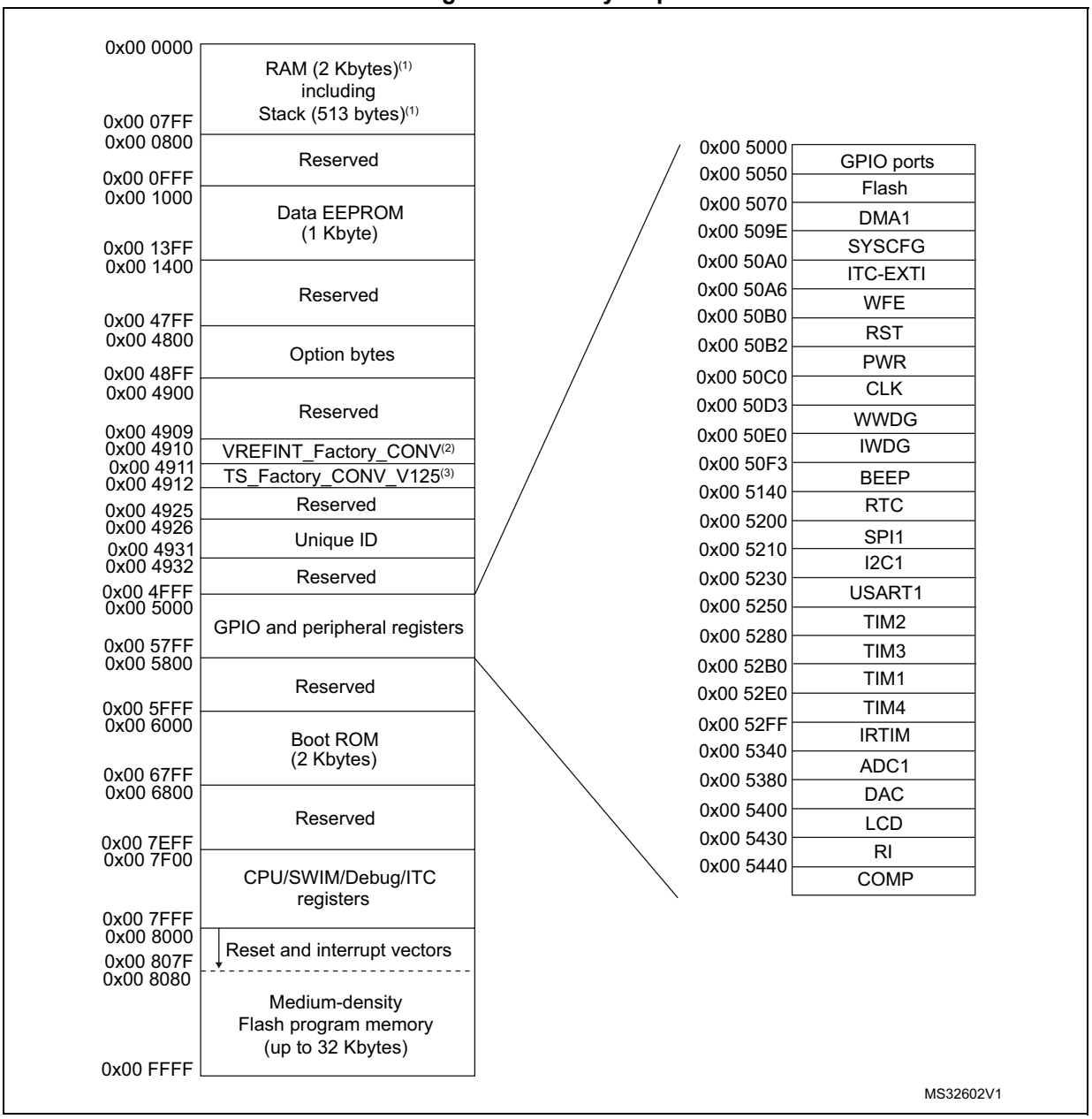
Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48	VFQFPN32	LQFP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
34	22	22	PD5/TIM1_CH3 /LCD_SEG19(2)/ ADC1_IN9/COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port D5	Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9/ Comparator 1 positive input
35	23	23	PD6/TIM1_BKIN /LCD_SEG20(2)/ ADC1_IN8/RTC_CALIB/ /VREFINT/ COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port D6	Timer 1 - break input / LCD segment 20 / ADC1_IN8 / RTC calibration / Internal voltage reference output / Comparator 1 positive input
36	24	24	PD7/TIM1_CH1N /LCD_SEG21(2)/ ADC1_IN7/RTC_ALARM/ VREFINT/ COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port D7	Timer 1 - inverted channel 1/ LCD segment 21 / ADC1_IN7 / RTC alarm / Internal voltage reference output /Comparator 1 positive input
14	-	-	PE0(5)/LCD_SEG1(2)	I/O	FT	X	X	X	HS	X	X	Port E0	LCD segment 1
15	-	-	PE1/TIM1_CH2N /LCD_SEG2(2)	I/O	TT(3)	X	X	X	HS	X	X	Port E1	Timer 1 - inverted channel 2 / LCD segment 2
16	-	-	PE2/TIM1_CH3N /LCD_SEG3(2)	I/O	TT(3)	X	X	X	HS	X	X	Port E2	Timer 1 - inverted channel 3 / LCD segment 3
17	-	-	PE3/LCD_SEG4(2)	I/O	TT(3)	X	X	X	HS	X	X	Port E3	LCD segment 4
18	-	-	PE4/LCD_SEG5(2)	I/O	TT(3)	X	X	X	HS	X	X	Port E4	LCD segment 5
19	-	-	PE5/LCD_SEG6(2)/ ADC1_IN23/COMP2_INP / COMP1_INP	I/O	TT(3)	X	X	X	HS	X	X	Port E5	LCD segment 6 / ADC1_IN23 / Comparator 2 positive input / Comparator 1 positive input
47	-	-	PE6/LCD_SEG26(2)/ PVD_IN	I/O	TT(3)	X	X	X	HS	X	X	Port E6	LCD segment 26/PVD_IN
48	-	-	PE7/LCD_SEG27(2)	I/O	TT(3)	X	X	X	HS	X	X	Port E7	LCD segment 27
32	-	-	PF0/ADC1_IN24/ DAC_OUT	I/O	TT(3)	X	X	X	HS	X	X	Port F0	ADC1_IN24 / DAC_OUT

5 Memory and register map

5.1 Memory mapping

The memory map is shown in *Figure 9*.

Figure 9. Memory map



1. *Table 6* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. The VREFINT_Factory_CONV byte represents the LSB of the V_{REFINT} 12-bit ADC conversion result. The MSB have a fixed value: 0x6.
3. The TS_Factory_CONV_V125 byte represents the LSB of the V_{125} 12-bit ADC conversion result. The MSB have a fixed value: 0x3. The V_{125} measurement is performed at 125°C.
4. Refer to *Table 9* for an overview of hardware register mapping, to *Table 8* for details on I/O port hardware registers, and to *Table 10* for information on CPU/SWIM/debug module controller registers.

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52B6	TIM1	TIM1_SR1	TIM1 status register 1	0x00
0x00 52B7		TIM1_SR2	TIM1 status register 2	0x00
0x00 52B8		TIM1_EGR	TIM1 event generation register	0x00
0x00 52B9		TIM1_CCMR1	TIM1 Capture/Compare mode register 1	0x00
0x00 52BA		TIM1_CCMR2	TIM1 Capture/Compare mode register 2	0x00
0x00 52BB		TIM1_CCMR3	TIM1 Capture/Compare mode register 3	0x00
0x00 52BC		TIM1_CCMR4	TIM1 Capture/Compare mode register 4	0x00
0x00 52BD		TIM1_CCER1	TIM1 Capture/Compare enable register 1	0x00
0x00 52BE		TIM1_CCER2	TIM1 Capture/Compare enable register 2	0x00
0x00 52BF		TIM1_CNTRH	TIM1 counter high	0x00
0x00 52C0		TIM1_CNTRL	TIM1 counter low	0x00
0x00 52C1		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 52C2		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 52C3		TIM1_ARRH	TIM1 Auto-reload register high	0xFF
0x00 52C4		TIM1_ARRL	TIM1 Auto-reload register low	0xFF
0x00 52C5		TIM1_RCR	TIM1 Repetition counter register	0x00
0x00 52C6		TIM1_CCR1H	TIM1 Capture/Compare register 1 high	0x00
0x00 52C7		TIM1_CCR1L	TIM1 Capture/Compare register 1 low	0x00
0x00 52C8		TIM1_CCR2H	TIM1 Capture/Compare register 2 high	0x00
0x00 52C9		TIM1_CCR2L	TIM1 Capture/Compare register 2 low	0x00
0x00 52CA		TIM1_CCR3H	TIM1 Capture/Compare register 3 high	0x00
0x00 52CB		TIM1_CCR3L	TIM1 Capture/Compare register 3 low	0x00
0x00 52CC		TIM1_CCR4H	TIM1 Capture/Compare register 4 high	0x00
0x00 52CD		TIM1_CCR4L	TIM1 Capture/Compare register 4 low	0x00
0x00 52CE		TIM1_BKR	TIM1 break register	0x00
0x00 52CF		TIM1_DTR	TIM1 dead-time register	0x00
0x00 52D0		TIM1_OISR	TIM1 output idle state register	0x00
0x00 52D1		TIM1_DCR1	DMA1 control register 1	0x00
0x00 52D2		TIM1_DCR2	TIM1 DMA1 control register 2	0x00
0x00 52D3		TIM1_DMA1R	TIM1 DMA1 address for burst mode	0x00
0x00 52D4 to 0x00 52DF	Reserved area (12 bytes)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 slave mode control register	0x00
0x00 52E3		TIM4_DER	TIM4 DMA1 request enable register	0x00
0x00 52E4		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 52E5		TIM4_SR1	TIM4 status register 1	0x00
0x00 52E6		TIM4_EGR	TIM4 event generation register	0x00
0x00 52E7		TIM4_CNTR	TIM4 counter	0x00
0x00 52E8		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E9		TIM4_ARR	TIM4 auto-reload register	0x00
0x00 52EA to 0x00 52FE	Reserved area (21 bytes)			
0x00 52FF	IRTIM	IR_CR	Infrared control register	0x00
0x00 5300 to 0x00 533F	Reserved area (64 bytes)			
0x00 5340	ADC1	ADC1_CR1	ADC1 configuration register 1	0x00
0x00 5341		ADC1_CR2	ADC1 configuration register 2	0x00
0x00 5342		ADC1_CR3	ADC1 configuration register 3	0x1F
0x00 5343		ADC1_SR	ADC1 status register	0x00
0x00 5344		ADC1_DRH	ADC1 data register high	0x00
0x00 5345		ADC1_DRL	ADC1 data register low	0x00
0x00 5346		ADC1_HTRH	ADC1 high threshold register high	0x0F
0x00 5347		ADC1_HTRL	ADC1 high threshold register low	0xFF
0x00 5348		ADC1_LTRH	ADC1 low threshold register high	0x00
0x00 5349		ADC1_LTRL	ADC1 low threshold register low	0x00
0x00 534A		ADC1_SQR1	ADC1 channel sequence 1 register	0x00
0x00 534B		ADC1_SQR2	ADC1 channel sequence 2 register	0x00
0x00 534C		ADC1_SQR3	ADC1 channel sequence 3 register	0x00
0x00 534D		ADC1_SQR4	ADC1 channel sequence 4 register	0x00
0x00 534E		ADC1_TRIGR1	ADC1 trigger disable 1	0x00
0x00 534F		ADC1_TRIGR2	ADC1 trigger disable 2	0x00
0x00 5350		ADC1_TRIGR3	ADC1 trigger disable 3	0x00
0x00 5351		ADC1_TRIGR4	ADC1 trigger disable 4	0x00

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 12* for details on option byte addresses.

The option bytes can also be modified ‘on the fly’ by the application in IAP mode, except for the ROP, and UBC values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L15x/STM8L16x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0320) for information on SWIM programming procedures.

Table 12. Option byte addresses

Address	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0xAA
0x00 4802	UBC (User Boot code size)	OPT1	UBC[7:0]								0x00
0x00 4807	Reserved										0x00
0x00 4808	Independent watchdog option	OPT3 [3:0]	Reserved				WWDG_HALT	WWDG_HW	IWDG_HALT	IWDG_HW	0x00
0x00 4809	Number of stabilization clock cycles for HSE and LSE oscillators	OPT4	Reserved				LSECNT[1:0]		HSECNT[1:0]		0x00
0x00 480A	Brownout reset (BOR)	OPT5 [3:0]	Reserved				BOR_TH			BOR_ON	0x01
0x00 480B	Bootloader option bytes (OPTBL)	OPTBL [15:0]	OPTBL[15:0]								0x00
0x00 480C											0x00

Table 13. Option byte description

Option byte no.	Option description
OPT0	**ROP[7:0]** Memory readout protection (ROP) 0xAA: Disable readout protection (write access via SWIM protocol) Refer to Readout protection section in STM8L05xx, STM8L15xx, STM8L162x, STM8AL31xx, STM8AL3Lxx, STM8AL31Exx and STM8AL3LExx MCU families reference manual (RM0031).
OPT1	**UBC[7:0]** Size of the user boot code area 0x00: No UBC 0x01: the UBC contains only the interrupt vectors. 0x02: Page 0 and 1 reserved for the UBC and read/write protected. Page 0 contains only the interrupt vectors. 0x03: Page 0 to 2 reserved for UBC, memory write-protected. 0xFF: Page 0 to 254 reserved for the UBC, memory write-protected. Refer to User boot code section in STM8L05xx, STM8L15xx, STM8L162x, STM8AL31xx, STM8AL3Lxx, STM8AL31Exx and STM8AL3LExx MCU families reference manual (RM0031).
OPT2	Reserved
OPT3	**IWDG_HW:** Independent watchdog 0: Independent watchdog activated by software 1: Independent watchdog activated by hardware
	IWDG_HALT: Independent watchdog off in Halt/Active-halt 0: Independent watchdog continues running in Halt/Active-halt mode 1: Independent watchdog stopped in Halt/Active-halt mode
	WWDG_HW: Window watchdog 0: Window watchdog activated by software 1: Window watchdog activated by hardware
	WWDG_HALT: Window window watchdog reset on Halt/Active-halt 0: Window watchdog stopped in Halt mode 1: Window watchdog generates a reset when MCU enters Halt mode
OPT4	**HSECNT**: Number of HSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles
	LSECNT: Number of LSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles Refer to *Table 33: LSE oscillator characteristics*

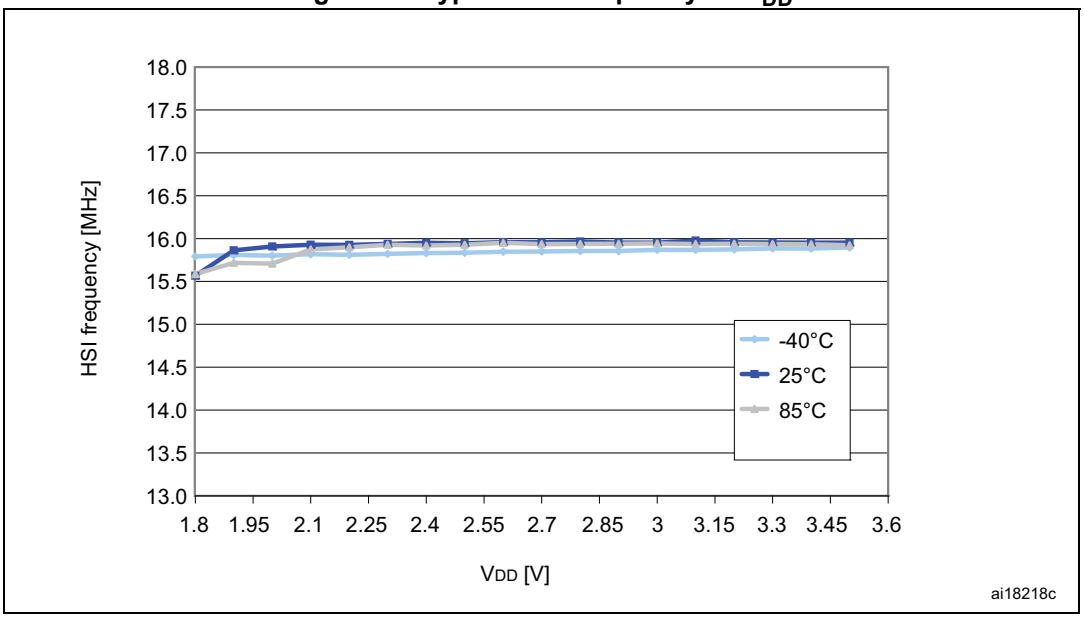
Current consumption of on-chip peripherals

Table 28. Peripheral current consumption

Symbol	Parameter		Typ. V_{DD} = 3.0 V	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)		13	µA/MHz
$I_{DD(TIM2)}$	TIM2 supply current (1)		8	
$I_{DD(TIM3)}$	TIM3 supply current (1)		8	
$I_{DD(TIM4)}$	TIM4 timer supply current (1)		3	
$I_{DD(USART1)}$	USART1 supply current (2)		6	
$I_{DD(SPI1)}$	SPI1 supply current (2)		3	
$I_{DD(I2C1)}$	I^2C1 supply current (2)		5	
$I_{DD(DMA1)}$	DMA1 supply current(2)		3	
$I_{DD(WWDG)}$	WWDG supply current(2)		2	
$I_{DD(ALL)}$	Peripherals ON(3)		44	
$I_{DD(ADC1)}$	ADC1 supply current(4)		1500	µA
$I_{DD(DAC)}$	DAC supply current(5)		370	
$I_{DD(COMP1)}$	Comparator 1 supply current(6)		0.160	
$I_{DD(COMP2)}$	Comparator 2 supply current(6)	Slow mode	2	
		Fast mode	5	
$I_{DD(PVD/BOR)}$	Power voltage detector and brownout Reset unit supply current (7)		2.6	
$I_{DD(BOR)}$	Brownout Reset unit supply current (7)		2.4	
$I_{DD(IDWDG)}$	Independent watchdog supply current	including LSI supply current	0.45	
		excluding LSI supply current	0.05	

1. Data based on a differential I_{DD} measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
3. Peripherals listed above the $I_{DD(ALL)}$ parameter ON: TIM1, TIM2, TIM3, TIM4, USART1, SPI1, I2C1, DMA1, WWDG.
4. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion.
5. Data based on a differential I_{DD} measurement between DAC in reset configuration and continuous DAC conversion of V_{DD} /2. Floating DAC output.
6. Data based on a differential I_{DD} measurement between COMP1 or COMP2 in reset configuration and COMP1 or COMP2 enabled with static inputs. Supply current of internal reference voltage excluded.
7. Including supply current of internal reference voltage.

Figure 17. Typical HSI frequency vs V_{DD}



Low speed internal RC oscillator (LSI)

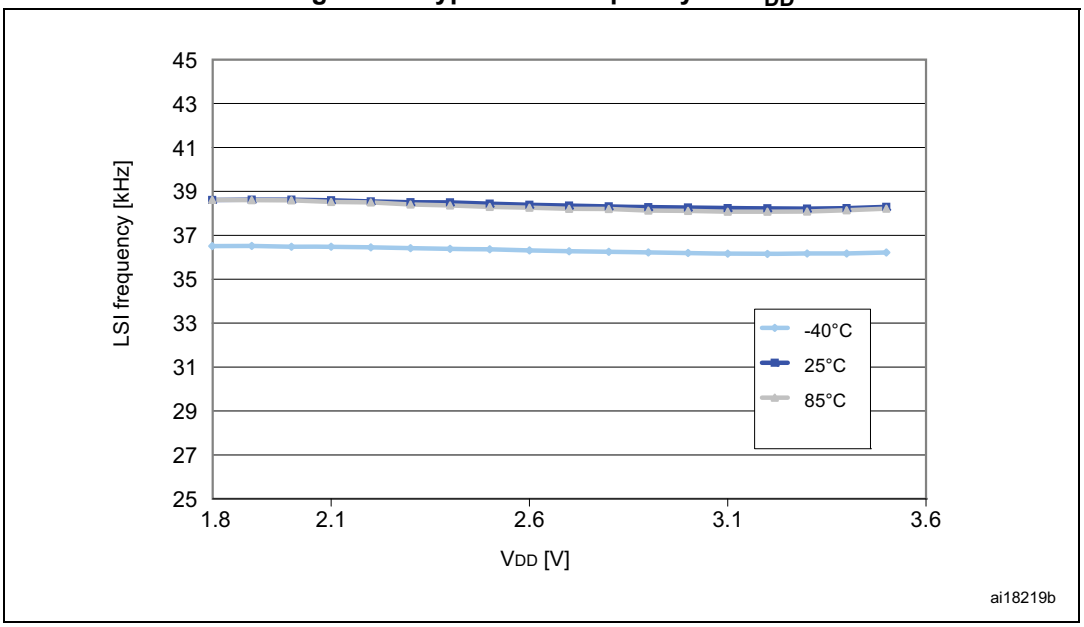
In the following table, data are based on characterization results, not tested in production.

Table 35. LSI oscillator characteristics

Symbol	Parameter (1)	Conditions(1)	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	26	38	56	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	200(2)	µs
$I_{DD(LSI)}$	LSI oscillator frequency drift(3)	0 °C ≤ T_A ≤ 85 °C	-12	-	11	%

1. V_{DD} = 1.65 V to 3.6 V, T_A = -40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. This is a deviation for an individual part, once the initial frequency has been measured.

Figure 18. Typical LSI frequency vs. V_{DD}



9.3.5 Memory characteristics

T_A = -40 to 125 °C unless otherwise specified.

Table 36. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization results.

Flash memory

Table 37. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{SYSCLK} = 16 MHz	1.65	-	3.6	V
t_{prog}	Programming time for 1 or 128 bytes (block) erase/write cycles (on programmed byte)	-	-	6	-	ms
	Programming time for 1 to 128 bytes (block) write cycles (on erased byte)	-	-	3	-	
I_{prog}	Programming/ erasing consumption	T_A = +25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A = +25 °C, V_{DD} = 1.8 V	-		-	

Figure 32. SPI1 timing diagram - slave mode and CPHA=0

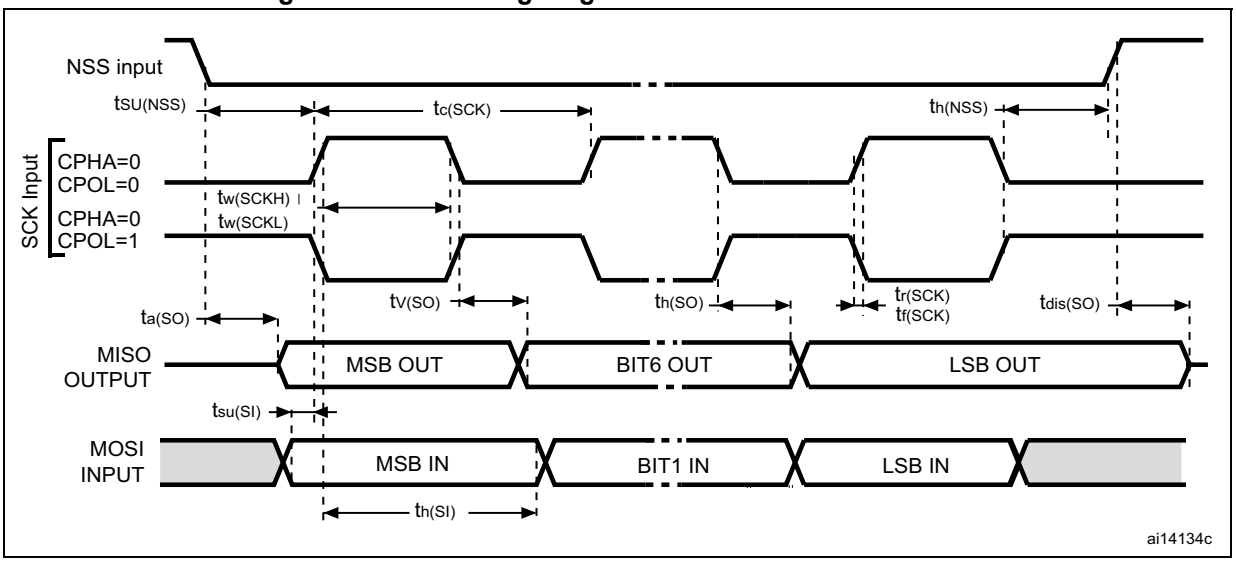
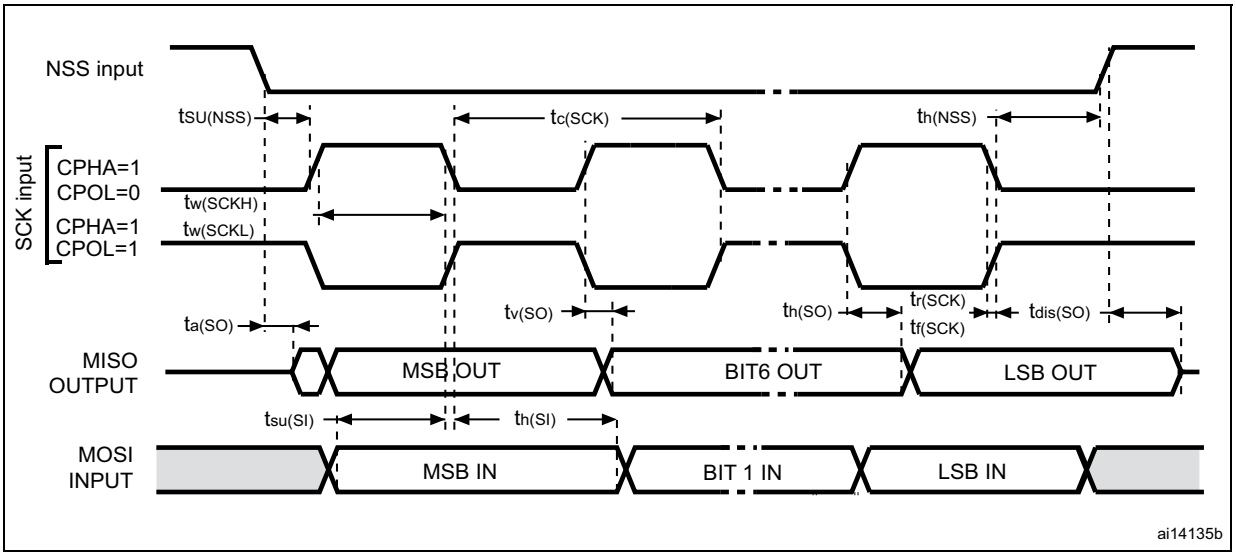


Figure 33. SPI1 timing diagram - slave mode and CPHA=1(1)



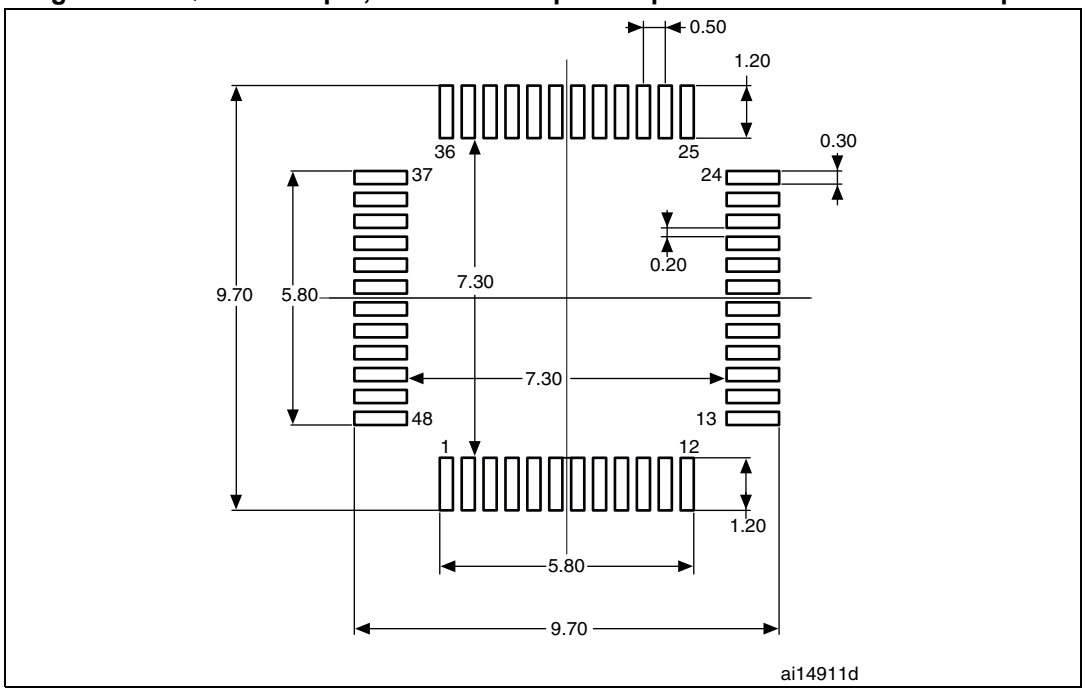
1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 56. ADC1 characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Sampling time	V_{AIN} on PF0 fast channel V_{DDA} < 2.4 V	0.43(4)(5)	-	-	µs
		V_{AIN} on PF0 fast channel 2.4 V ≤ V_{DDA} ≤ 3.6 V	0.22(4)(5)	-	-	
		V_{AIN} on slow channels V_{DDA} < 2.4 V	0.86(4)(5)	-	-	
		V_{AIN} on slow channels 2.4 V ≤ V_{DDA} ≤ 3.6 V	0.41(4)(5)	-	-	
t_{conv}	12-bit conversion time	-	12000000 / f_{ADC} + t_S			
		16 MHz	1(4)	-	-	
t_{WKUP}	Wakeup time from OFF state	-	-	-	3	
t_{IDLE}(6)	Time before a new conversion	-	-	-	∞	s
$t_{VREFINT}$	Internal reference voltage startup time	-	-	-	refer to *Table 49*	ms

1. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. V_{REF-} or V_{DDA} must be tied to ground.
3. Guaranteed by design.
4. Minimum sampling and conversion time is reached for maximum Rext = 0.5 kΩ.
5. Value obtained for continuous conversion on fast channel.
6. In STM8L05xx, STM8L15xx, STM8L162x, STM8AL31xx, STM8AL3Lxx, STM8AL31Exx and STM8AL3LExx MCU families reference manual (RM0031), t_{IDLE} defines the time between 2 conversions, or between ADC ON and the first conversion. t_{IDLE} is not relevant for this device.

Figure 42. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint

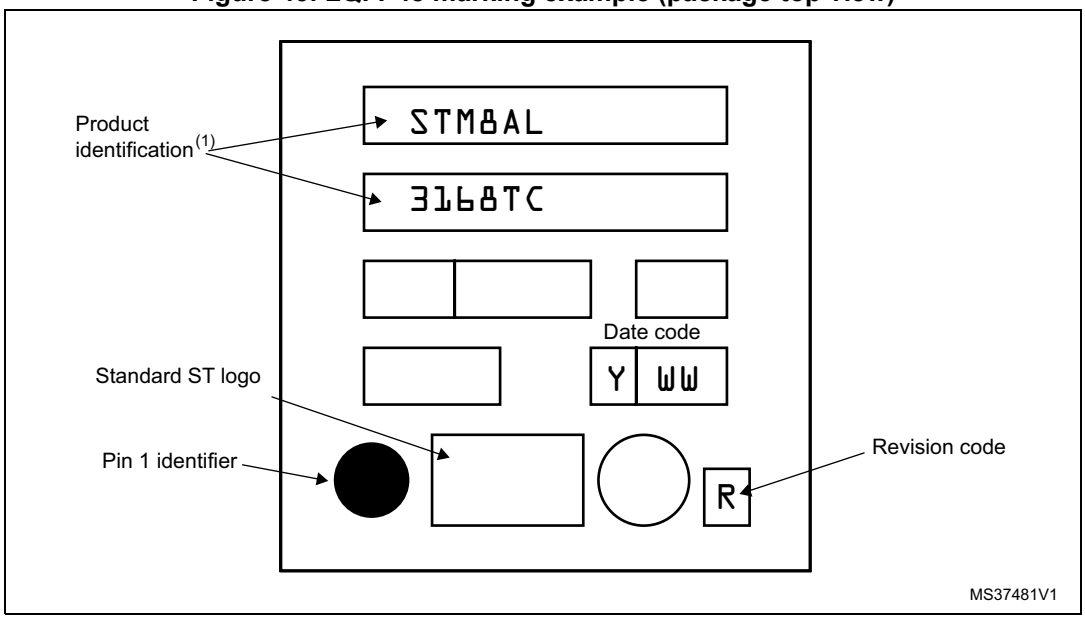


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

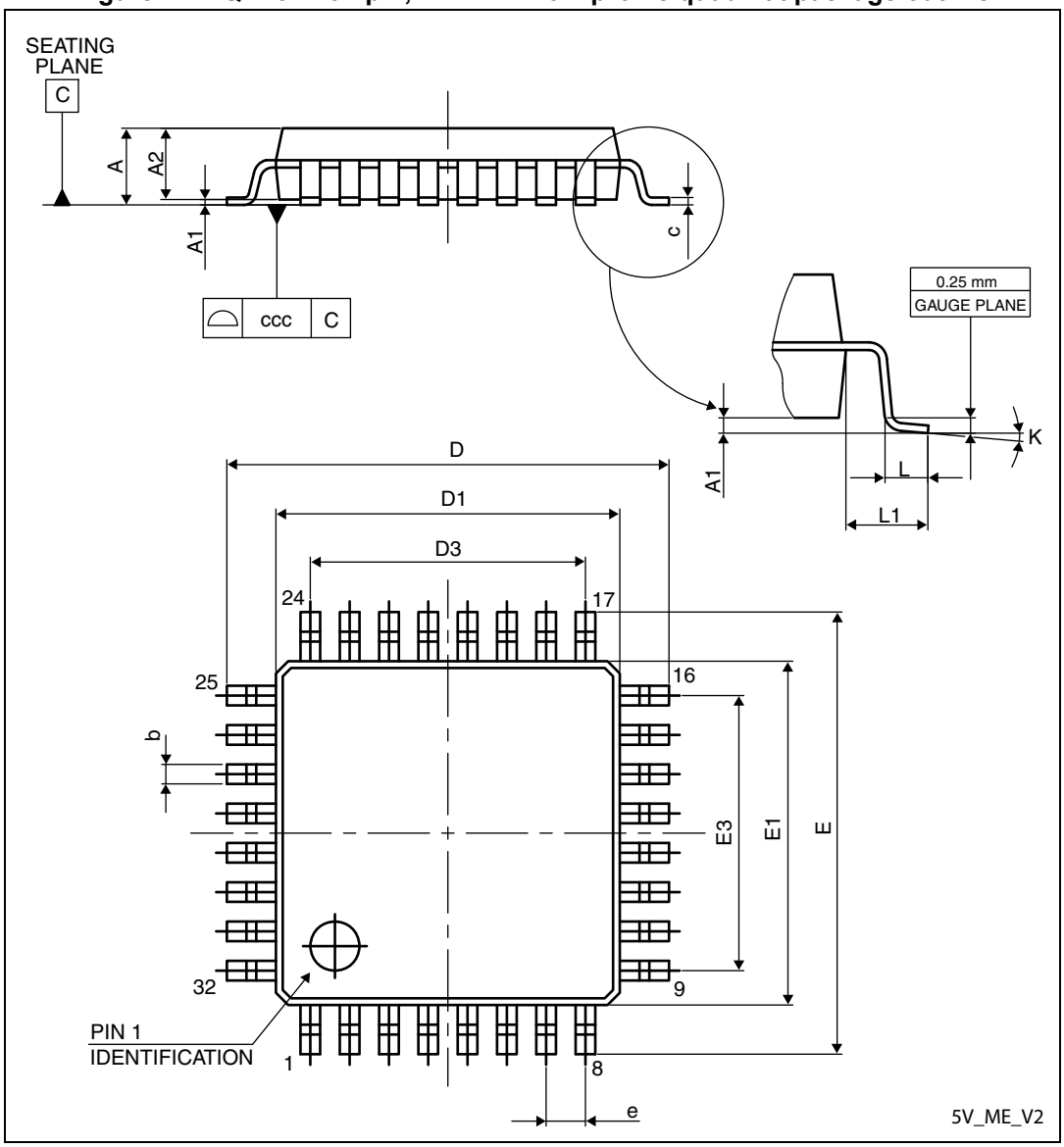
Figure 43. LQFP48 marking example (package top view)



1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

10.3 LQFP32 package information

Figure 44. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline



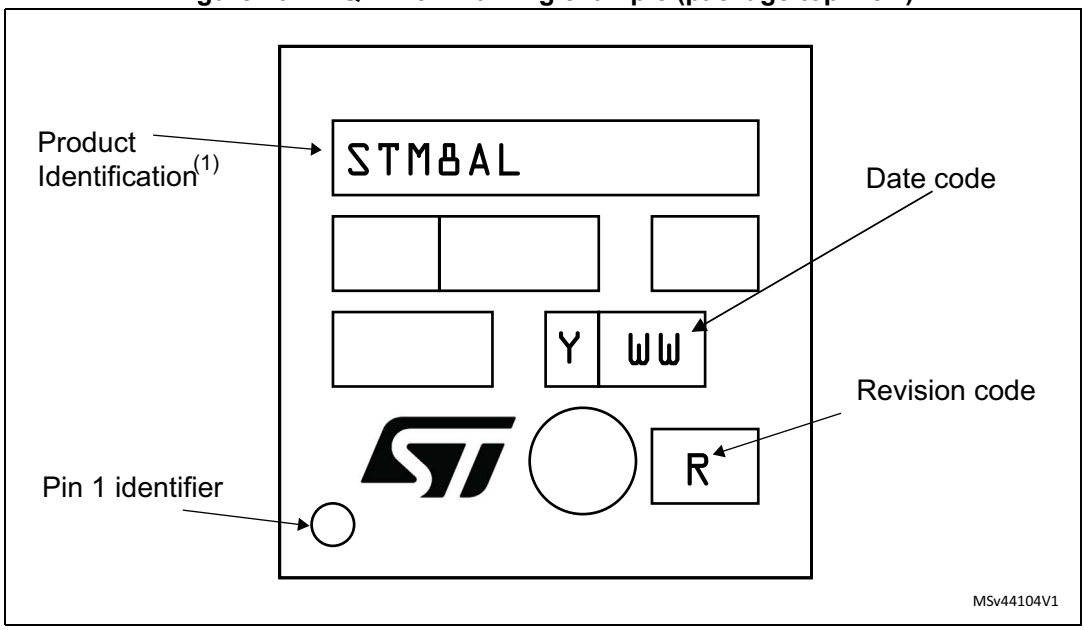
1. Drawing is not to scale.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 49. VFQFPN32 marking example (package top view)



1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Table 69. Document revision history (continued)

Date	Revision	Changes
18-Oct-2016	7	Added: – *Section 10.4: VFQFPN32 package information* – *Figure 7: STM8AL31x6U 32-pin pinout (without LCD)* – *Figure 8: STM8AL3Lx6U 32-pin pinout (with LCD)* Updated: – *Section 9.2: Absolute maximum ratings* – *Section : Device marking on page 110*, *Section : Device marking on page 113* and *Section : Device marking on page 117* – *Table 2: Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x low-power device features and peripheral counts* – *Table 5: Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x pin description* – *Table 19: General operating conditions* – *Table 68: Thermal characteristics* – *Figure 33: SPI1 timing diagram - slave mode and CPHA=1(1)* – *Figure 34: SPI1 timing diagram - master mode(1)* – *Figure 50: Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x ordering information scheme* – Footnotes on *Figure 43: LQFP48 marking example (package top view)* and *Figure 46: LQFP32 marking example (package top view)*
28-Mar-2017	8	Updated: – *Table 67: VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data* – *Figure 48: VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint*