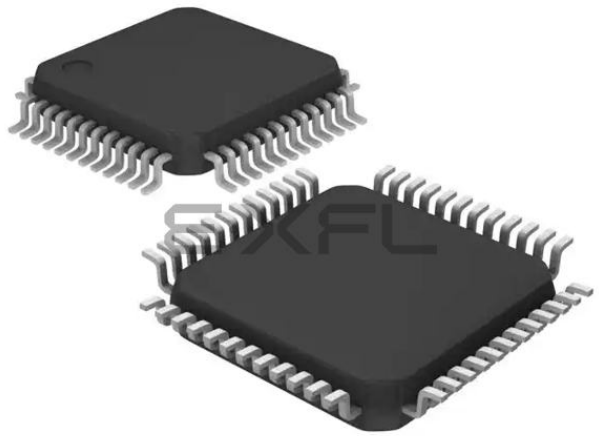

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	41
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 25x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3l68tay

1 Introduction

This document describes the features, pinout, mechanical data and ordering information of the medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x devices (microcontrollers with up to 32-Kbyte Flash memory density). These devices are referred to as medium-density devices in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031) and in STM8L and STM8AL Flash programming manual (PM0054).

For more details on the whole STMicroelectronics ultra-low-power family please refer to *Section 3: Functional overview on page 13*.

For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).

For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

Note: The medium-density devices provide the following benefits:

- Integrated system
  - Up to 32 Kbytes of medium-density embedded Flash program memory
  - 1 Kbytes of data EEPROM
  - Internal high speed and low-power low speed RC.
  - Embedded reset
- Ultra-low power consumption
  - 195 µA/MHZ + 440 µA (consumption)
  - 0.9 µA with LSI in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for Low power wait mode and Low power run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access.
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Wide choice of development tools

All devices offer 12-bit ADC, DAC, two comparators, Real-time clock three 16-bit timers, one 8-bit timer as well as standard communication interface such as SPI, I2C and USART. A 4x28-segment LCD is available on the medium-density STM8AL3Lxx line. *Table 2: Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x low-power device features and peripheral counts* and *Section 3: Functional overview* give an overview of the complete range of peripherals proposed in this family.

Figure 1 shows the general block diagram of the device family.

2.1 Device overview

Table 2. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x low-power device features and peripheral counts

Features		STM8AL3xx6			STM8AL3xx8		
Flash (Kbyte)		8	16	32	8	16	32
Data EEPROM (Kbyte)		1					
RAM-Kbyte		2			2		
LCD		4x17 (1)			4x28 (1)		
Timers	Basic	1 (8-bit)			1 (8-bit)		
	General purpose	2 (16-bit)			2 (16-bit)		
	Advanced control	1 (16-bit)			1 (16-bit)		
Communication interfaces	SPI	1			1		
	I2C	1			1		
	USART	1			1		
GPIOs		30 (2)(3) or 29 (1)(3)			41(3)		
12-bit synchronized ADC (number of channels)		1 (22 (2) or 21 (1))			1 (25)		
12-Bit DAC (number of channels)		1 (1)			1 (1)		
Comparators COMP1/COMP2		2			2		
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator					
CPU frequency		16 MHz					
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power down)					
Operating temperature		-40 to +85 °C/-40 to +125 °C					
Packages		LQFP32 (7 x7 mm) VFQFPN32 (5 x 5 mm)			LQFP48 (7x7) VFQFPN32 (5 x 5 mm)		

1. STM8AL3Lxx versions only
2. STM8AL31xx versions only
3. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

3.2 Central processing unit STM8

3.2.1 Advanced STM8 core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains six internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16 Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

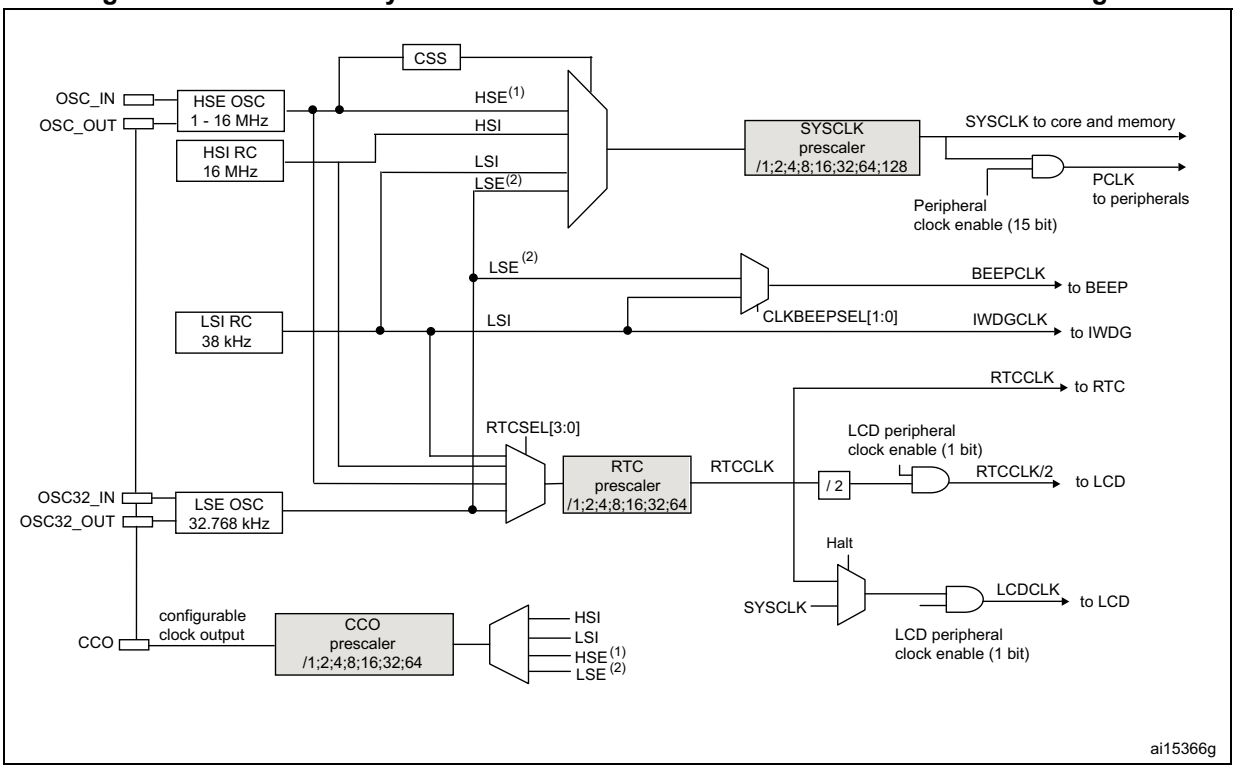
- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

3.2.2 Interrupt controller

The medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x feature a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts

Figure 2. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x clock tree diagram



1. The HSE clock source can be either an external crystal/ceramic resonator or an external source (HSE bypass). Refer to *Section HSE clock* in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).
2. The LSE clock source can be either an external crystal/ceramic resonator or a external source (LSE bypass). Refer to *Section LSE clock* in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).

3.5 Low power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours.
- Periodic alarms based on the calendar can also be generated from every second to every year.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

Bootloader

A bootloader is available to reprogram the Flash memory using the USART1 interface. The reference document for the bootloader is *UM0560: STM8 bootloader user manual*.

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5055 to 0x00 506F	Reserved area (27 bytes)			
0x00 5070	DMA1	DMA1_GCSR	DMA1 global configuration & status register	0xFC
0x00 5071		DMA1_GIR1	DMA1 global interrupt register 1	0x00
0x00 5072 to 0x00 5074		Reserved area (3 bytes)		
0x00 5075		DMA1_C0CR	DMA1 channel 0 configuration register	0x00
0x00 5076		DMA1_C0SPR	DMA1 channel 0 status & priority register	0x00
0x00 5077		DMA1_C0NDTR	DMA1 number of data to transfer register (channel 0)	0x00
0x00 5078		DMA1_C0PARH	DMA1 peripheral address high register (channel 0)	0x52
0x00 5079		DMA1_C0PARL	DMA1 peripheral address low register (channel 0)	0x00
0x00 507A		Reserved area (1 byte)		
0x00 507B		DMA1_C0M0ARH	DMA1 memory 0 address high register (channel 0)	0x00
0x00 507C		DMA1_C0M0ARL	DMA1 memory 0 address low register (channel 0)	0x00
0x00 507D to 0x00 507E	Reserved area (2 bytes)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50A9 to 0x00 50AF	Reserved area (7 bytes)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2	PWR	PWR_CSR1	Power control and status register 1	0x00
0x00 50B3		PWR_CSR2	Power control and status register 2	0x00
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_DIVR	Clock master divider register	0x03
0x00 50C1		CLK_CRTCR	Clock RTC register	0x00
0x00 50C2		CLK_ICKR	Internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	Peripheral clock gating register 1	0x00
0x00 50C4		CLK_PCKENR2	Peripheral clock gating register 2	0x80
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6		CLK_ECKR	External clock control register	0x00
0x00 50C7		CLK_SCSR	System clock status register	0x01
0x00 50C8		CLK_SWR	System clock switch register	0x01
0x00 50C9		CLK_SWCR	Clock switch control register	0bxxxx0000
0x00 50CA		CLK_CSSR	Clock security system register	0x00
0x00 50CB		CLK_CBEEPR	Clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	HSI calibration register	0xxx
0x00 50CD		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	Main regulator control status register	0bxx11100x
0x00 50D0 to 0x00 50D2	Reserved area (3 bytes)			
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDR window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF

Table 10. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register Label	Register Name	Reset Status
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM Debug module control register 1	0x00
0x00 7F97		DM_CR2	DM Debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM Debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM Debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 bytes)			

1. Accessible by debug module only

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 12* for details on option byte addresses.

The option bytes can also be modified ‘on the fly’ by the application in IAP mode, except for the ROP, and UBC values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L15x/STM8L16x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0320) for information on SWIM programming procedures.

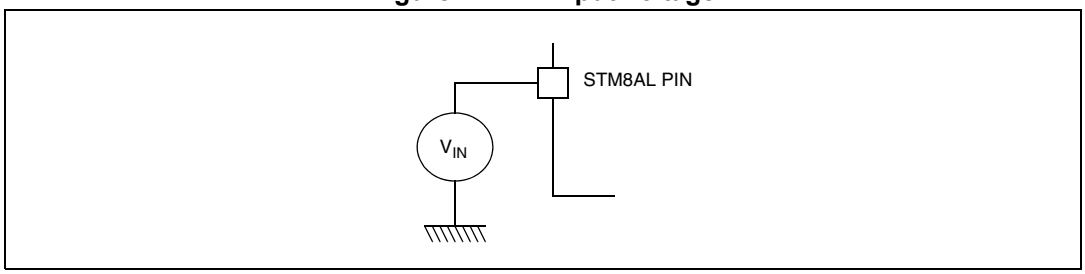
Table 12. Option byte addresses

Address	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0xAA
0x00 4802	UBC (User Boot code size)	OPT1	UBC[7:0]								0x00
0x00 4807	Reserved										0x00
0x00 4808	Independent watchdog option	OPT3 [3:0]	Reserved				WWDG_HALT	WWDG_HW	IWDG_HALT	IWDG_HW	0x00
0x00 4809	Number of stabilization clock cycles for HSE and LSE oscillators	OPT4	Reserved				LSECNT[1:0]		HSECNT[1:0]		0x00
0x00 480A	Brownout reset (BOR)	OPT5 [3:0]	Reserved				BOR_TH			BOR_ON	0x01
0x00 480B	Bootloader option bytes (OPTBL)	OPTBL [15:0]	OPTBL[15:0]								0x00
0x00 480C											0x00

9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 11. Pin input voltage



9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 15: Voltage characteristics*, *Table 16: Current characteristics* and *Table 17: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and a functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability.

The device's mission profile (application conditions) is compliant with the JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 15. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage (including V_{DDA} and V_{DD2})(1)	- 0.3	4.0	V
V_{IN}(2)	Input voltage on true open-drain pins (PC0 and PC1)	V_{SS} - 0.3	V_{DD} + 4.0	
	Input voltage on five-volt tolerant (FT) pins (PA7 and PE0)			
	Input voltage on 3.6 V tolerant (TT) pins		4.0	
	Input voltage on any other pin			
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 106*		V

1. All power (V_{DD1}, V_{DD2}, V_{DDA}) and ground (V_{SS1}, V_{SS2}, V_{SSA}) pins must always be connected to the external power supply.
2. V_{IN} maximum must always be respected. Refer to *Table 16* for maximum allowed injected current values.

Table 16. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by IR_TIM pin (with high sink LED driver capability)	80	
	Output current sunk by any other I/O and control pin	25	
	Output current sourced by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$	Injected current on true open-drain pins (PC0 and PC1)(1)	- 5/+0	
	Injected current on five-volt tolerant (FT) pins (PA7 and PE0)(1)	- 5/+0	
	Injected current on 3.6 V tolerant (TT) pins(1)	- 5/+0	
	Injected current on any other pin(2)	- 5/+5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(3)	± 25	

1. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15* for maximum allowed input voltage values.
2. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15* for maximum allowed input voltage values.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	° C
T_J	Maximum junction temperature	150	

Table 18. Operating lifetime (OLF)(1)

Symbol	Ratings	Value	Unit
OLF	Conforming to AEC-Q100	-40 to 125 °C	Grade 1

1. For detailed mission profile analysis, please contact the local ST Sales Office.

Table 26. Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal

Symbol	Parameter	Condition[1]		Typ	Unit
$I_{DD(AH)}$[2]	Supply current in Active-halt mode	V_{DD} = 1.8 V	LSE	1.15	µA
			LSE/32[3]	1.05	
		V_{DD} = 3 V	LSE	1.30	
			LSE/32[3]	1.20	
		V_{DD} = 3.6 V	LSE	1.45	
			LSE/32[3]	1.35	

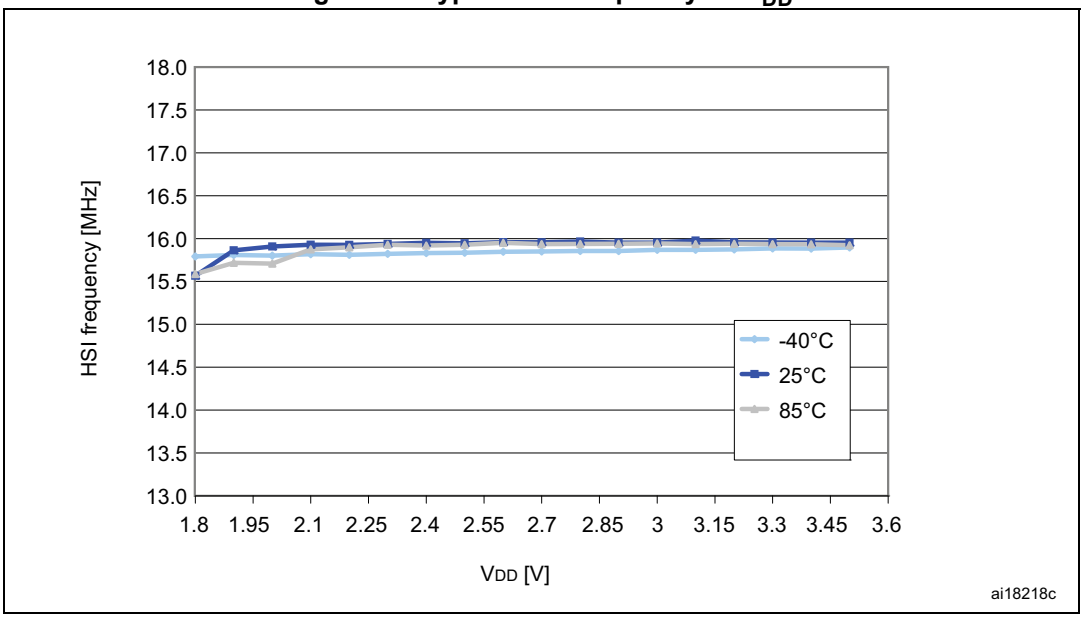
1. No floating I/O, unless otherwise specified.
2. Data based on measurements on bench, including 32.768 kHz external crystal oscillator consumption.
3. RTC clock is LSE divided by 32.

Table 27. Total current consumption and timing in Halt mode at V_{DD} = 1.65 to 3.6 V

Symbol	Parameter	Condition[1]	Typ	Max	Unit
$I_{DD(Halt)}$	Supply current in Halt mode (ultra low power ULP bit =1 in the PWR_CSR2 register)	T_A = -40 °C to 25 °C	0.4	0.9[4]	µA
		T_A = 85 °C	0.9	2.8[2]	
		T_A = 125 °C	4.4	13[2]	
$I_{DD(WUHalt)}$	Supply current during wakeup time from Halt mode (using HSI)	-	2.4	-	mA
$t_{WU\_HSI(Halt)}$[3][5]	Wakeup time from Halt to Run mode (using HSI)	-	4.7	7[4]	µs
$t_{WU\_LSI(Halt)}$[3][5]	Wakeup time from Halt mode to Run mode (using LSI)	-	150	-	

1. T_A = -40 to 125 °C, no floating I/O, unless otherwise specified.
2. Tested at 85°C for temperature range A or 125°C for temperature range C.
3. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.
4. Guaranteed by characterization results.
5. Wakeup time until start of interrupt vector fetch. The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.

Figure 17. Typical HSI frequency vs V_{DD}



Low speed internal RC oscillator (LSI)

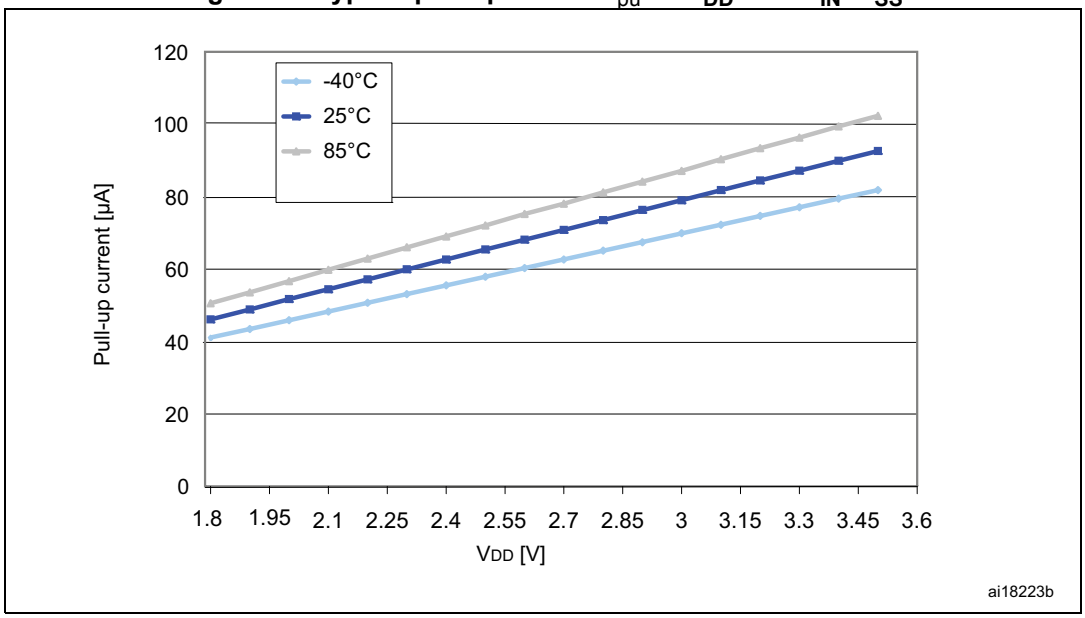
In the following table, data are based on characterization results, not tested in production.

Table 35. LSI oscillator characteristics

Symbol	Parameter (1)	Conditions(1)	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	26	38	56	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	200(2)	µs
$I_{DD(LSI)}$	LSI oscillator frequency drift(3)	0 °C ≤ T_A ≤ 85 °C	-12	-	11	%

1. V_{DD} = 1.65 V to 3.6 V, T_A = -40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. This is a deviation for an individual part, once the initial frequency has been measured.

Figure 22. Typical pull-up current I_{pu} vs V_{DD} with $V_{IN}=V_{SS}$



Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 42. Output driving current (high sink ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
High sink	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +2 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +2 mA, V_{DD} = 1.8 V	-	0.45	
			I_{IO} = +10 mA, V_{DD} = 3.0 V	-	0.7	
	V_{OH} (2)	Output high level voltage for an I/O pin	I_{IO} = -2 mA, V_{DD} = 3.0 V	V_{DD}-0.45	-	V
			I_{IO} = -1 mA, V_{DD} = 1.8 V	V_{DD}-0.45	-	
			I_{IO} = -10 mA, V_{DD} = 3.0 V	V_{DD}-0.7	-	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

Table 43. Output driving current (true open drain ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Open drain	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +3 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +1 mA, V_{DD} = 1.8 V	-	0.45	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Table 44. Output driving current (PA0 with high sink LED driver capability)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
IR	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA, V_{DD} = 2.0 V	-	0.45	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

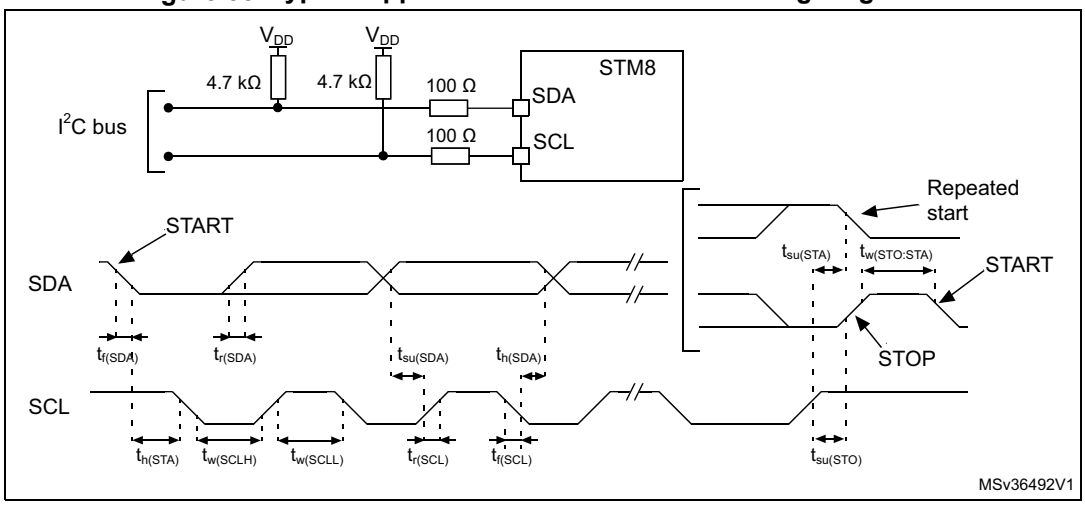
Table 47. I²C characteristics (continued)

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max (2)	Min (2)	Max (2)	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0		0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{SYSCLK} must be at least equal to 8 MHz to achieve max fast I²C speed (400 kHz).
2. Data based on standard I²C protocol requirements, not tested in production.

Note: For speeds around 200 kHz, the achieved speed can have a ± 5% tolerance
For other speed ranges, the achieved speed can have a ± 2% tolerance
The above variations depend on the accuracy of the external components used.

Figure 35. Typical application with I²C bus and timing diagram(1)



1. Measurement points are done at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}

Table 49. Reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max.	Unit
I_{REFINT}	Internal reference voltage consumption	-	-	1.4	-	µA
$T_{S\_VREFINT}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	-	5	10	µs
I_{BUF}(2)	Internal reference voltage buffer consumption (used for ADC)	-	-	13.5	25	µA
$V_{REFINT\ out}$	Reference voltage output	-	1.202 (3)	1.224	1.242 (3)	V
I_{LPBUF}(2)	Internal reference voltage low power buffer consumption (used for comparators or output)	-	-	730	1200	nA
I_{REFOUT}(2)	Buffer output current(4)	-	-	-	1	µA
C_{REFOUT}	Reference voltage output load	-	-	-	50	pF
$t_{VREFINT}$	Internal reference voltage startup time	-	-	2	3	ms
t_{BUFEN}(2)	Internal reference voltage buffer startup time once enabled (1)	-	-	-	10	µs
$ACC_{VREFINT}$	Accuracy of V_{REFINT} stored in the VREFINT_Factory_CONV byte(5)	-	-	-	± 5	mV
$STAB_{VREFINT}$(2)	Stability of V_{REFINT} over temperature	-40 °C ≤ T_A ≤ 125 °C	-	20	50	ppm/°C
	Stability of V_{REFINT} over temperature	0 °C ≤ T_A ≤ 50 °C	-	-	20	
$STAB_{VREFINT}$(2)	Stability of V_{REFINT} after 1000 hours	-	-	-	1000	ppm

1. Defined when ADC output reaches its final value ±1/2LSB
2. Guaranteed by design.
3. Tested in production at V_{DD} = 3 V ±10 mV.
4. To guaranty less than 1% V_{REFOUT} deviation.
5. Measured at V_{DD} = 3 V ±10 mV. This value takes into account V_{DD} accuracy and ADC conversion accuracy.

9.3.11 Temperature sensor

In the following table, data are based on characterization results, not tested in production, unless otherwise specified.

Table 50. TS characteristics

Symbol	Parameter	Min	Typ	Max.	Unit
V_{125}(1)	Sensor reference voltage at 125 °C ±5 °C	0.640	0.660	0.680	V
T_L	V_{SENSOR} linearity with temperature	-	±1	±2	°C
Avg_slope	Average slope	1.59(2)	1.62	1.65(2)	mV/°C
$I_{DD(TEMP)}$	Consumption	-	3.4	6(2)	µA

In the following table, data based on characterization results, not tested in production.

Table 54. DAC accuracy

Symbol	Parameter	Conditions	Typ.	Max(1)	Unit
DNL	Differential non linearity(2)	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF, DACOUT buffer ON(3)	1.5	3	12-bit LSB
		No load, DACOUT buffer OFF	1.5	3	
INL	Integral non linearity(4)	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF,DACOUT buffer ON(3)	2	4	
		No load, DACOUT buffer OFF	2	4	
Offset	Offset error(5)	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF, DACOUT buffer ON(3)	±10	±25	
		No load, DACOUT buffer OFF	±5	±8	
Offset1	Offset error at Code 1 (6)	DACOUT buffer OFF	±1.5	±5	
Gain error	Gain error(7)	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF,DACOUT buffer ON(3)	+0.1/-0.2	+0.2/-0.5	%
		No load, DACOUT buffer OFF	+0/-0.2	+0/-0.4	
TUE	Total unadjusted error	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF, DACOUT buffer ON(3)	12	30	12-bit LSB
		No load, DACOUT buffer OFF	8	12	

1. Not tested in production.
2. Difference between two consecutive codes - 1 LSB.
3. For 48-pin packages only. For 28-pin and 32-pin packages, DAC output buffer must be kept off and no load must be applied.
4. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023.
5. Difference between the value measured at Code (0x800) and the ideal value = $V_{REF+}/2$.
6. Difference between the value measured at Code (0x001) and the ideal value.
7. Difference between the ideal slope of the transfer function and the measured slope computed from Code 0x000 and 0xFFF when buffer is ON, and from Code giving 0.2 V and (V_{DDA} -0.2) V when buffer is OFF.

In the following table, data are guaranteed by design, not tested in production.

Table 55. DAC output on PB4-PB5-PB6(1)

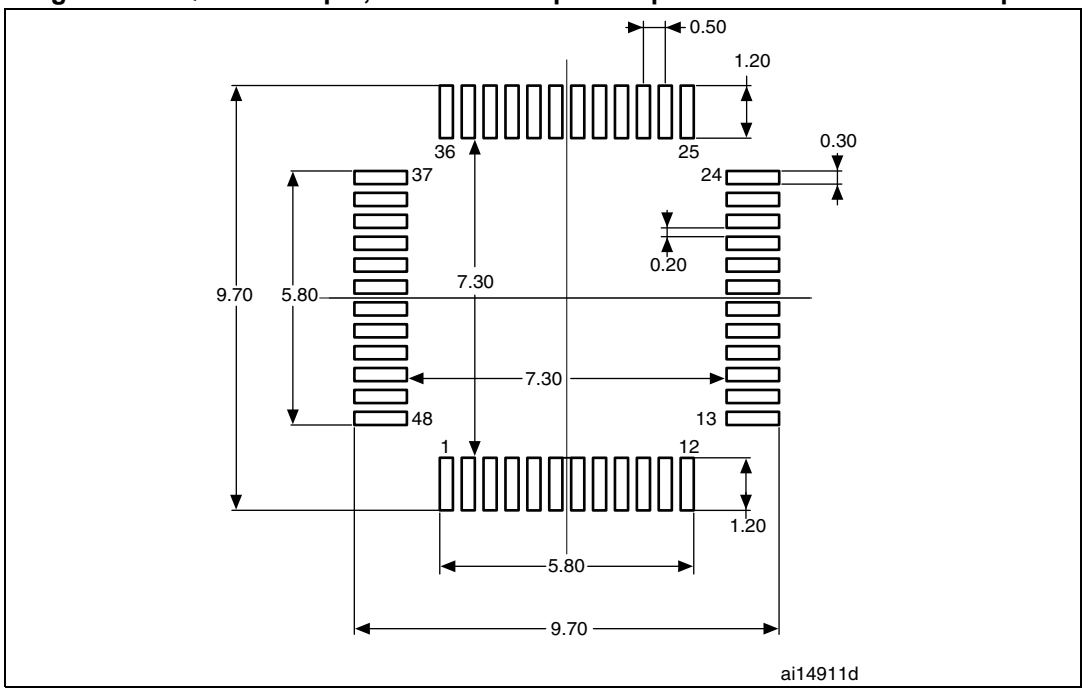
Symbol	Parameter	Conditions	Max	Unit
R_{int}	Internal resistance between DAC output and PB4-PB5-PB6 output	2.7 V < V_{DD} < 3.6 V	1.4	kΩ
		2.4 V < V_{DD} < 3.6 V	1.6	
		2.0 V < V_{DD} < 3.6 V	3.2	
		1.8 V < V_{DD} < 3.6 V	8.2	

1. 32 or 28-pin packages only. The DAC channel can be routed either on PB4, PB5 or PB6 using the routing interface I/O switch registers.

9.3.14 12-bit ADC1 characteristics

In the following table, data are guaranteed by design, not tested in production.

Figure 42. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint

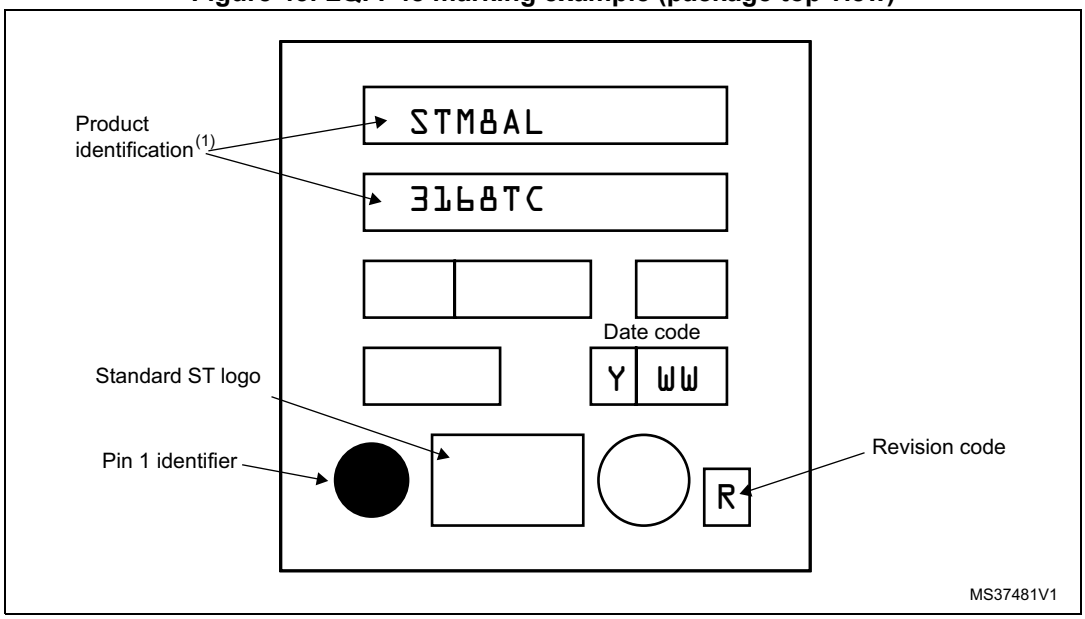


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 43. LQFP48 marking example (package top view)



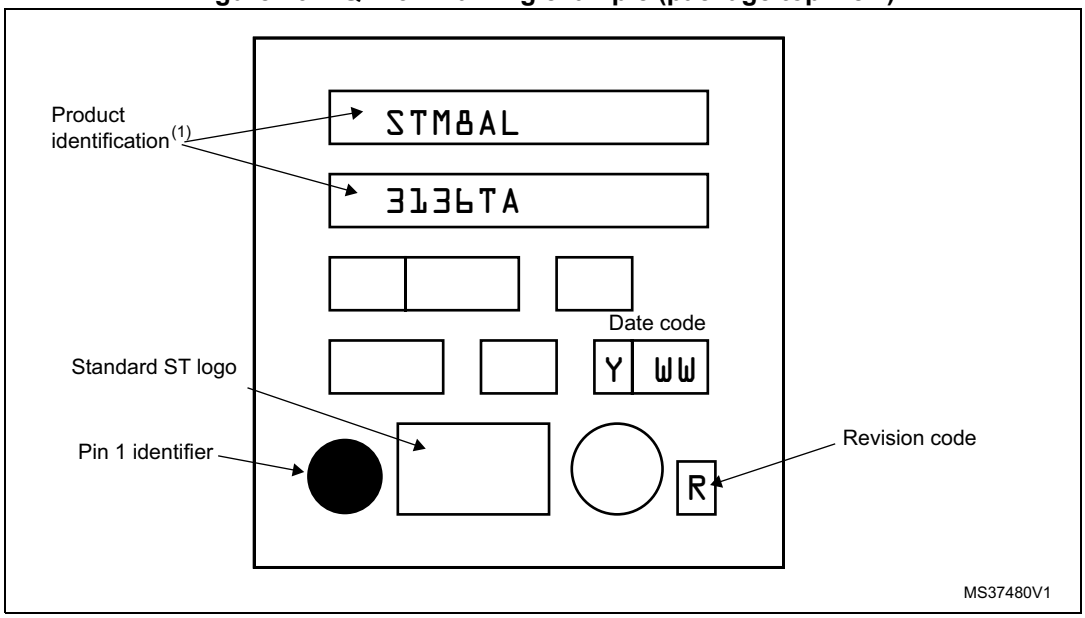
1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 46. LQFP32 marking example (package top view)



1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.