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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	41
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 25x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3l68tcy

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

Bootloader

A bootloader is available to reprogram the Flash memory using the USART1 interface. The reference document for the bootloader is *UM0560: STM8 bootloader user manual*.

Figure 7. STM8AL31x6U 32-pin pinout (without LCD)

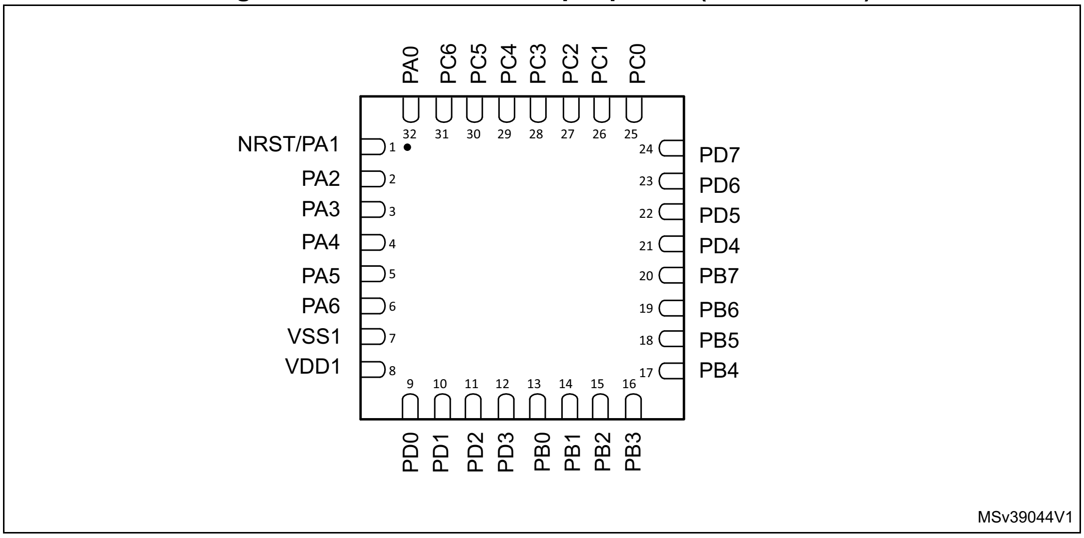


Figure 8. STM8AL3Lx6U 32-pin pinout (with LCD)

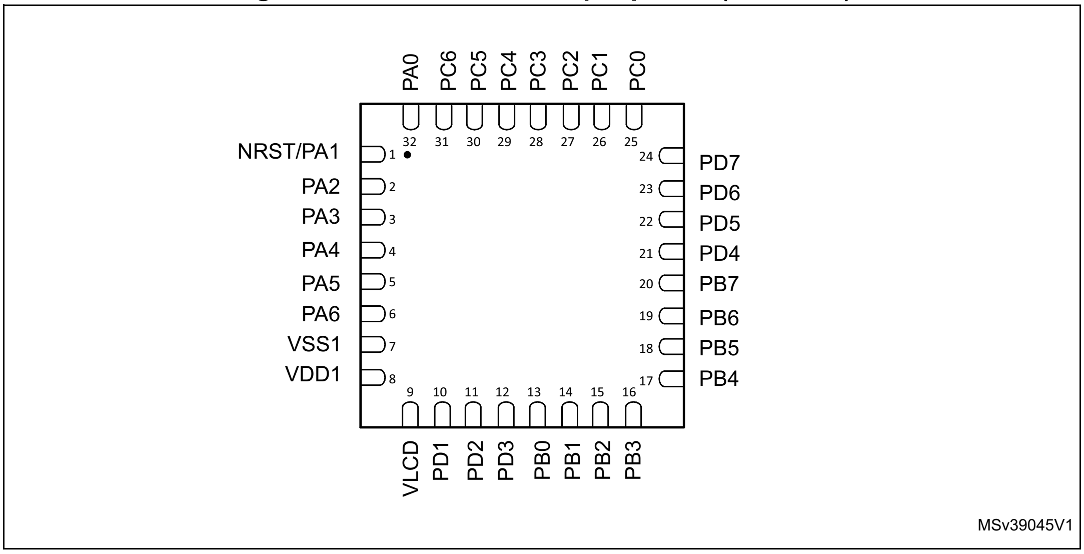


Table 4. Legend/abbreviation

Type	I= input, O = output, S = power supply	
I/O level	TT	3.6 V tolerant
	FT	Five-volt tolerant
Port and control configuration	Input	– floating – wpu = weak pull-up – Ext. interrupt = external interrupt
	Output	– HS = high sink/source – OD = open drain (where T defines a true open drain) – PP = push pull
Reset state	Underlined X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 5. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x pin description

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48	VFQFPN32	LQFP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
2	1	1	NRST/PA1[1]	I/O	-	-	X	-	HS	-	X	Reset	PA1
3	2	2	PA2/OSC_IN/ *[USART1_TX]*[4]/ *[SPI1_MISO]*[4]	I/O	-	X	X	X	HS	X	X	Port A2	HSE oscillator input / *[USART1 transmit] / [SPI1 master in- slave out]*
4	3	3	PA3/OSC_OUT/*[USART1 _RX]*[4]/*[SPI1_MOSI]*[4]	I/O	-	X	X	X	HS	X	X	Port A3	HSE oscillator output / *[USART1 receive]/ [SPI1 master out/slave in]*
5	-	-	PA4/TIM2_BKIN/ LCD_COM0[2]/ADC1_IN2 /COMP1_INP	I/O	TT[3]	X	X	X	HS	X	X	Port A4	Timer 2 - break input / LCD COM 0 / ADC1 input 2 / Comparator 1 positive input
-	4	4	PA4/TIM2_BKIN/ *[TIM2_ETR]*[4]/ LCD_COM0[2]/ ADC1_IN2/COMP1_INP	I/O	TT[3]	X	X	X	HS	X	X	Port A4	Timer 2 - break input / *[Timer 2 - trigger]* / LCD_COM 0 / ADC1 input 2 / Comparator 1 positive input
6	-	-	PA5/TIM3_BKIN/ LCD_COM1[2]/ADC1_IN1 /COMP1_INP	I/O	TT[3]	X	X	X	HS	X	X	Port A5	Timer 3 - break input / LCD_COM 1 / ADC1 input 1/ Comparator 1 positive input

Table 5. Medium-density STM8AL313x/4x/6x and STM8AL3L4x/6x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48	VFQFPN32	LQFP32				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
34	22	22	PD5/TIM1_CH3 /LCD_SEG19[2]/ ADC1_IN9/COMP1_INP	I/O	TT[3]	X	X	X	HS	X	X	Port D5	Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9/ Comparator 1 positive input
35	23	23	PD6/TIM1_BKIN /LCD_SEG20[2]/ ADC1_IN8/RTC_CALIB/ /VREFINT/ COMP1_INP	I/O	TT[3]	X	X	X	HS	X	X	Port D6	Timer 1 - break input / LCD segment 20 / ADC1_IN8 / RTC calibration / Internal voltage reference output / Comparator 1 positive input
36	24	24	PD7/TIM1_CH1N /LCD_SEG21[2]/ ADC1_IN7/RTC_ALARM/ VREFINT/ COMP1_INP	I/O	TT[3]	X	X	X	HS	X	X	Port D7	Timer 1 - inverted channel 1/ LCD segment 21 / ADC1_IN7 / RTC alarm / Internal voltage reference output /Comparator 1 positive input
14	-	-	PE0[5]/LCD_SEG1[2]	I/O	FT	X	X	X	HS	X	X	Port E0	LCD segment 1
15	-	-	PE1/TIM1_CH2N /LCD_SEG2[2]	I/O	TT[3]	X	X	X	HS	X	X	Port E1	Timer 1 - inverted channel 2 / LCD segment 2
16	-	-	PE2/TIM1_CH3N /LCD_SEG3[2]	I/O	TT[3]	X	X	X	HS	X	X	Port E2	Timer 1 - inverted channel 3 / LCD segment 3
17	-	-	PE3/LCD_SEG4[2]	I/O	TT[3]	X	X	X	HS	X	X	Port E3	LCD segment 4
18	-	-	PE4/LCD_SEG5[2]	I/O	TT[3]	X	X	X	HS	X	X	Port E4	LCD segment 5
19	-	-	PE5/LCD_SEG6[2]/ ADC1_IN23/COMP2_INP / COMP1_INP	I/O	TT[3]	X	X	X	HS	X	X	Port E5	LCD segment 6 / ADC1_IN23 / Comparator 2 positive input / Comparator 1 positive input
47	-	-	PE6/LCD_SEG26[2]/ PVD_IN	I/O	TT[3]	X	X	X	HS	X	X	Port E6	LCD segment 26/PVD_IN
48	-	-	PE7/LCD_SEG27[2]	I/O	TT[3]	X	X	X	HS	X	X	Port E7	LCD segment 27
32	-	-	PF0/ADC1_IN24/ DAC_OUT	I/O	TT[3]	X	X	X	HS	X	X	Port F0	ADC1_IN24 / DAC_OUT

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5055 to 0x00 506F	Reserved area (27 bytes)			
0x00 5070	DMA1	DMA1_GCSR	DMA1 global configuration & status register	0xFC
0x00 5071		DMA1_GIR1	DMA1 global interrupt register 1	0x00
0x00 5072 to 0x00 5074		Reserved area (3 bytes)		
0x00 5075		DMA1_C0CR	DMA1 channel 0 configuration register	0x00
0x00 5076		DMA1_C0SPR	DMA1 channel 0 status & priority register	0x00
0x00 5077		DMA1_C0NDTR	DMA1 number of data to transfer register (channel 0)	0x00
0x00 5078		DMA1_C0PARH	DMA1 peripheral address high register (channel 0)	0x52
0x00 5079		DMA1_C0PARL	DMA1 peripheral address low register (channel 0)	0x00
0x00 507A		Reserved area (1 byte)		
0x00 507B		DMA1_C0M0ARH	DMA1 memory 0 address high register (channel 0)	0x00
0x00 507C		DMA1_C0M0ARL	DMA1 memory 0 address low register (channel 0)	0x00
0x00 507D to 0x00 507E	Reserved area (2 bytes)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5440	COMP	COMP_CSR1	Comparator control and status register 1	0x00
0x00 5441		COMP_CSR2	Comparator control and status register 2	0x00
0x00 5442		COMP_CSR3	Comparator control and status register 3	0x00
0x00 5443		COMP_CSR4	Comparator control and status register 4	0x00
0x00 5444		COMP_CSR5	Comparator control and status register 5	0x00

1. These registers are not impacted by a system reset. They are reset at power-on.

Table 10. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register Label	Register Name	Reset Status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 bytes)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC-SPR	ITC_SPR1	Interrupt Software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt Software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt Software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt Software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt Software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt Software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt Software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt Software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 bytes)			

Table 13. Option byte description (continued)

Option byte no.	Option description
OPT5	**BOR_ON**: 0: Brownout reset off 1: Brownout reset on
	BOR_TH[3:1]: Brownout reset thresholds. Refer to *Table 20* for details on the thresholds according to the value of BOR_TH bits.
OPTBL	**OPTBL[15:0]**: This option is checked by the boot ROM code after reset. Depending on the content of addresses Ox00 480B, Ox00 480C and 0x8000 (reset vector) the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 bootloader user manual for more details.

Table 22. Total current consumption in Wait mode (continued)

Symbol	Parameter	Conditions[1]			Typ	Max	Unit
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.38	0.55[3]	mA
				f_{CPU} = 1 MHz	0.40	0.60[3]	
				f_{CPU} = 4 MHz	0.50	0.65[3]	
				f_{CPU} = 8 MHz	0.60	0.75[3]	
				f_{CPU} = 16 MHz	0.80	0.90	
			HSE[4] external clock (f_{CPU}=HSE)	f_{CPU} = 125 kHz	0.05	0.10[3]	
				f_{CPU} = 1 MHz	0.10	0.20[3]	
				f_{CPU} = 4 MHz	0.25	0.45[3]	
				f_{CPU} = 8 MHz	0.50	0.65[3]	
				f_{CPU} = 16 MHz	1.00	1.20[3]	
			LSI	$f_{CPU} = f_{LSI}$	0.05	0.10[3]	
			LSE[5] external clock (32.768 kHz)	$f_{CPU} = f_{LSE}$	0.05	0.08[3]	

1. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU} = f_{SYSCLK}$
2. Flash is configured in I_{DDQ} mode in Wait mode by setting the EPM or WAITM bit in the Flash_CR1 register.
3. Guaranteed by characterization results.
4. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 32*.
5. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 33*.

Table 24. Total current consumption in low-power wait mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions[1]			Typ	Max	Unit
$I_{DD(LPW)}$	Supply current in Low power wait mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	3.00	3.30[2]	µA
				T_A = 85 °C	4.40	9[3]	
				T_A = 125 °C	11.00	18[3]	
		LSE external clock[4] (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	2.35	2.70[2]	
				T_A = 85 °C	3.10	3.70[2]	
				T_A = 125 °C	7.20	11.00[2]	

1. No floating I/Os.
2. Guaranteed by characterization results.
3. Tested at 85°C for temperature range A or 125°C for temperature range C.
4. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 33*.

Table 25. Total current consumption and timing in active-halt mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions [1]			Typ	Max[2]	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSI RC (at 38 kHz)	LCD OFF[3]	T_A = -40 °C to 25 °C	0.90	2.10	µA
				T_A = 85 °C	1.50	3.40	
				T_A = 125 °C	5.10	12.00	
			LCD ON (static duty/ external V_{LCD}) [4]	T_A = -40 °C to 25 °C	1.40	3.10	
				T_A = 85 °C	1.90	4.30	
				T_A = 125 °C	5.50	13.00	
			LCD ON (1/4 duty/ external V_{LCD}) [5]	T_A = -40 °C to 25 °C	1.90	4.30	
				T_A = 85 °C	2.40	5.40	
				T_A = 125 °C	6.00	15.00	
			LCD ON (1/4 duty/ internal V_{LCD}) [6]	T_A = -40 °C to 25 °C	3.90	8.75	
				T_A = 85 °C	4.50	10.20	
				T_A = 125 °C	6.80	16.30	

Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 42. Output driving current (high sink ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
High sink	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +2 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +2 mA, V_{DD} = 1.8 V	-	0.45	
			I_{IO} = +10 mA, V_{DD} = 3.0 V	-	0.7	
	V_{OH} (2)	Output high level voltage for an I/O pin	I_{IO} = -2 mA, V_{DD} = 3.0 V	V_{DD}-0.45	-	V
			I_{IO} = -1 mA, V_{DD} = 1.8 V	V_{DD}-0.45	-	
			I_{IO} = -10 mA, V_{DD} = 3.0 V	V_{DD}-0.7	-	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

Table 43. Output driving current (true open drain ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Open drain	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +3 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +1 mA, V_{DD} = 1.8 V	-	0.45	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Table 44. Output driving current (PA0 with high sink LED driver capability)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
IR	V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA, V_{DD} = 2.0 V	-	0.45	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Figure 23. Typ. V_{OL} @ V_{DD} = 3.0 V (high sink ports)

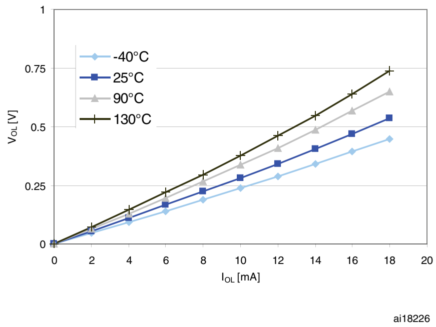


Figure 24. Typ. V_{OL} @ V_{DD} = 1.8 V (high sink ports)

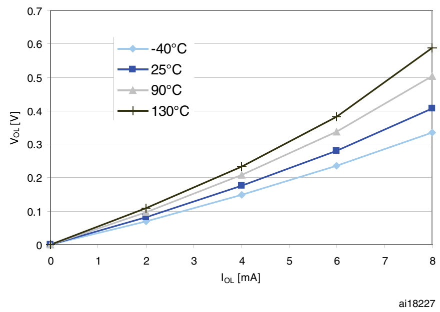


Figure 25. Typ. V_{OL} @ V_{DD} = 3.0 V (true open drain ports)

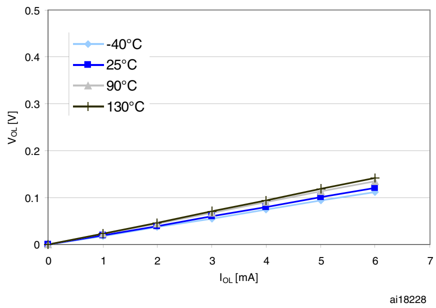


Figure 26. Typ. V_{OL} @ V_{DD} = 1.8 V (true open drain ports)

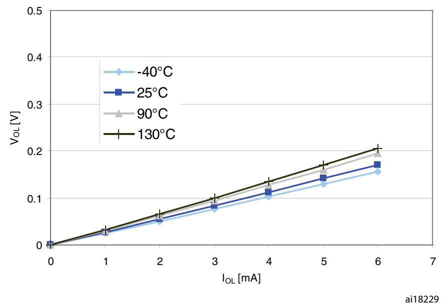


Figure 27. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.0 V (high sink ports)

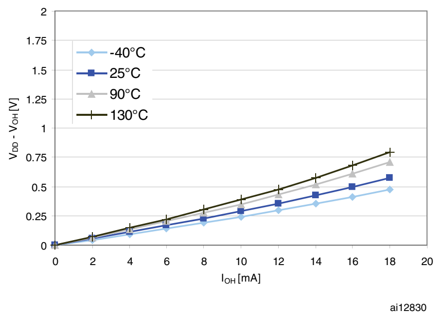
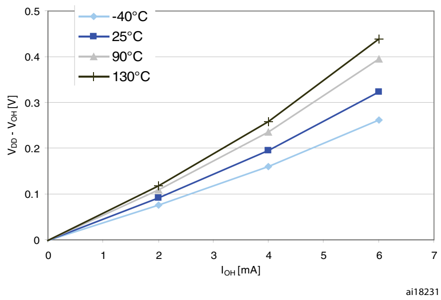


Figure 28. Typ. V_{DD} - V_{OH} @ V_{DD} = 1.8 V (high sink ports)



9.3.8 Communication interfaces

SPI1 - Serial peripheral interface

Unless otherwise specified, the parameters given in Table 46 are derived from tests performed under ambient temperature, f_{SYSCLK} frequency and V_{DD} supply voltage conditions summarized in Section 9.3.1. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 46. SPI1 characteristics

Symbol	Parameter	Conditions(1)	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI1 clock frequency	Master mode	0	8	MHz
		Slave mode	0	8	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI1 clock rise and fall time	Capacitive load: C = 30 pF	-	30	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 x $1/f_{SYSCLK}$	-	
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	80	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{MASTER} = 8 MHz, f_{SCK}= 4 MHz	105	145	
$t_{su(MI)}$(2) $t_{su(SI)}$(2)	Data input setup time	Master mode	30	-	
		Slave mode	3	-	
$t_{h(MI)}$(2) $t_{h(SI)}$(2)	Data input hold time	Master mode	15	-	
		Slave mode	0	-	
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode	-	3x $1/f_{SYSCLK}$	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	30	-	
$t_{v(SO)}$(2)	Data output valid time	Slave mode (after enable edge)	-	60	
$t_{v(MO)}$(2)	Data output valid time	Master mode (after enable edge)	-	20	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$(2)		Master mode (after enable edge)	1	-	

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and max time is for the maximum time to put the data in Hi-Z.

9.3.9 LCD controller (STM8AL3Lxx only)

In the following table, data are guaranteed by design and are not tested in production.

Table 48. LCD characteristics

Symbol	Parameter	Min	Typ	Max.	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.7	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.8	-	
V_{LCD3}	LCD internal reference voltage 3	-	2.9	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.0	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.1	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.2	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.3	-	
C_{EXT}	V_{LCD} external capacitance	0.1	-	2	µF
I_{DD}	Supply current(1) at V_{DD} = 1.8 V	-	3	-	µA
	Supply current(1) at V_{DD} = 3 V	-	3	-	
R_{HN} (2)	High value resistive network (low drive)	-	6.6	-	MΩ
R_{LN} (3)	Low value resistive network (high drive)	-	360	-	kΩ
V_{33}	Segment/Common higher level voltage	-	-	V_{LCDx}	V
V_{23}	Segment/Common 2/3 level voltage	-	$2/3V_{LCDx}$	-	
V_{12}	Segment/Common 1/2 level voltage	-	$1/2V_{LCDx}$	-	
V_{13}	Segment/Common 1/3 level voltage	-	$1/3V_{LCDx}$	-	
V_0	Segment/Common lowest level voltage	0	-	-	

1. LCD enabled with 3 V internal booster (LCD_CR1 = 0x08), 1/4 duty, 1/3 bias, division ratio= 64, all pixels active, no LCD connected.
2. R_{HN} is the total high value resistive network.
3. R_{LN} is the total low value resistive network.

VLCD external capacitor (STM8AL3Lxx only)

The application can achieve a stabilized LCD reference voltage by connecting an external capacitor C_{EXT} to the V_{LCD} pin. C_{EXT} is specified in *Table 48*.

9.3.10 Embedded reference voltage

In the following table, data are based on characterization results, not tested in production, unless otherwise specified.

Table 49. Reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max.	Unit
I_{REFINT}	Internal reference voltage consumption	-	-	1.4	-	µA
$T_{S\_VREFINT}$ (1)(2)	ADC sampling time when reading the internal reference voltage	-	-	5	10	µs
I_{BUF} (2)	Internal reference voltage buffer consumption (used for ADC)	-	-	13.5	25	µA
$V_{REFINT\ out}$	Reference voltage output	-	1.202 (3)	1.224	1.242 (3)	V
I_{LPBUF} (2)	Internal reference voltage low power buffer consumption (used for comparators or output)	-	-	730	1200	nA
I_{REFOUT} (2)	Buffer output current (4)	-	-	-	1	µA
C_{REFOUT}	Reference voltage output load	-	-	-	50	pF
$t_{VREFINT}$	Internal reference voltage startup time	-	-	2	3	ms
t_{BUFEN} (2)	Internal reference voltage buffer startup time once enabled (1)	-	-	-	10	µs
$ACC_{VREFINT}$	Accuracy of V_{REFINT} stored in the VREFINT_Factory_CONV byte (5)	-	-	-	± 5	mV
$STAB_{VREFINT}$ (2)	Stability of V_{REFINT} over temperature	-40 °C ≤ T_A ≤ 125 °C	-	20	50	ppm/°C
	Stability of V_{REFINT} over temperature	0 °C ≤ T_A ≤ 50 °C	-	-	20	
$STAB_{VREFINT}$ (2)	Stability of V_{REFINT} after 1000 hours	-	-	-	1000	ppm

1. Defined when ADC output reaches its final value ±1/2LSB
2. Guaranteed by design.
3. Tested in production at V_{DD} = 3 V ±10 mV.
4. To guaranty less than 1% V_{REFOUT} deviation.
5. Measured at V_{DD} = 3 V ±10 mV. This value takes into account V_{DD} accuracy and ADC conversion accuracy.

9.3.11 Temperature sensor

In the following table, data are based on characterization results, not tested in production, unless otherwise specified.

Table 50. TS characteristics

Symbol	Parameter	Min	Typ	Max.	Unit
V_{125} (1)	Sensor reference voltage at 125 °C ±5 °C	0.640	0.660	0.680	V
T_L	V_{SENSOR} linearity with temperature	-	±1	±2	°C
Avg_slope	Average slope	1.59 (2)	1.62	1.65 (2)	mV/°C
$I_{DD(TEMP)}$	Consumption	-	3.4	6 (2)	µA

Table 59. ADC1 accuracy with $V_{DDA} = V_{REF}^{+}$ = 1.8 V to 2.4 V

Symbol	Parameter	Typ.	Max(1)	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	2	3	
TUE	Total unadjusted error	3	5	
Offset	Offset error	2	3	
Gain	Gain error	2	3	

1. Not tested in production.

Figure 36. ADC1 accuracy characteristics

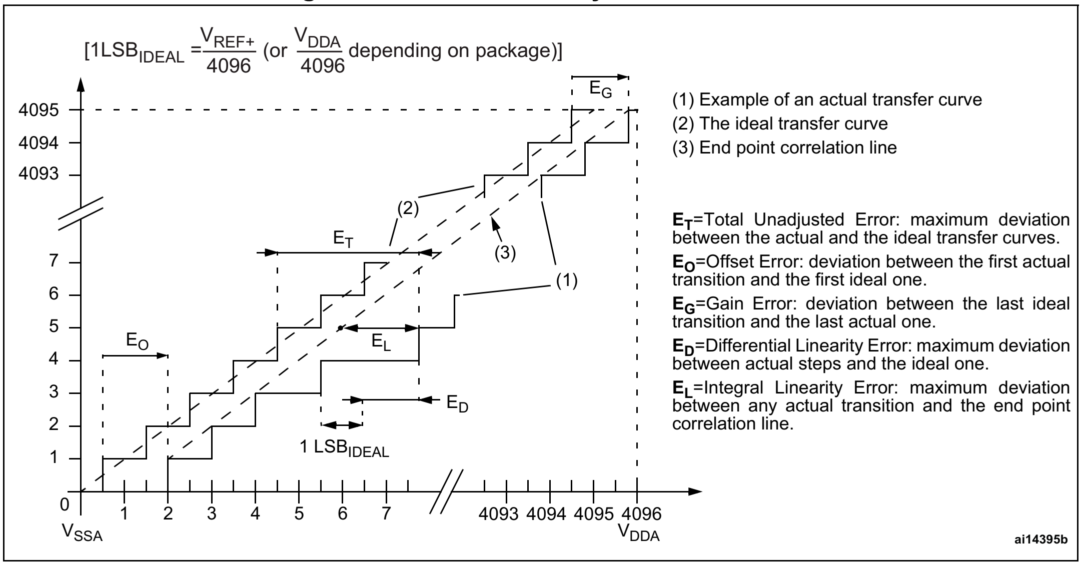
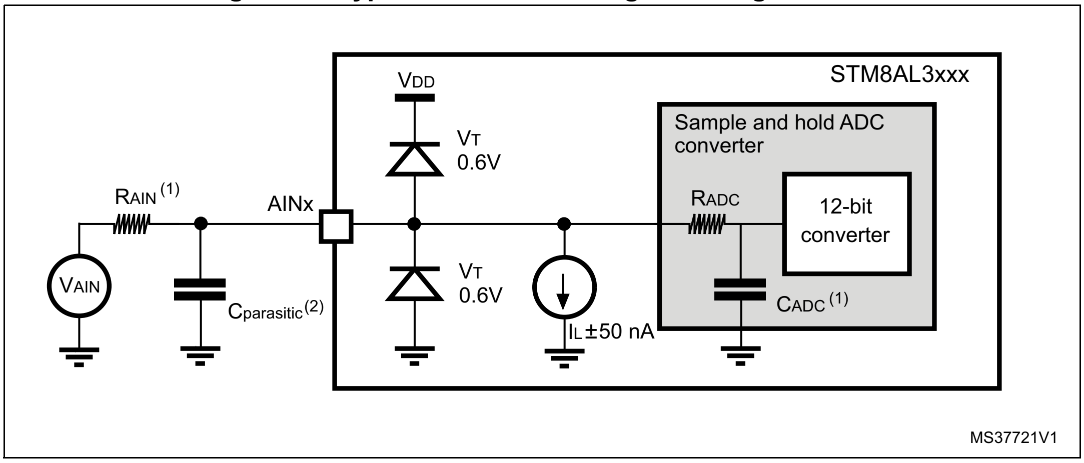


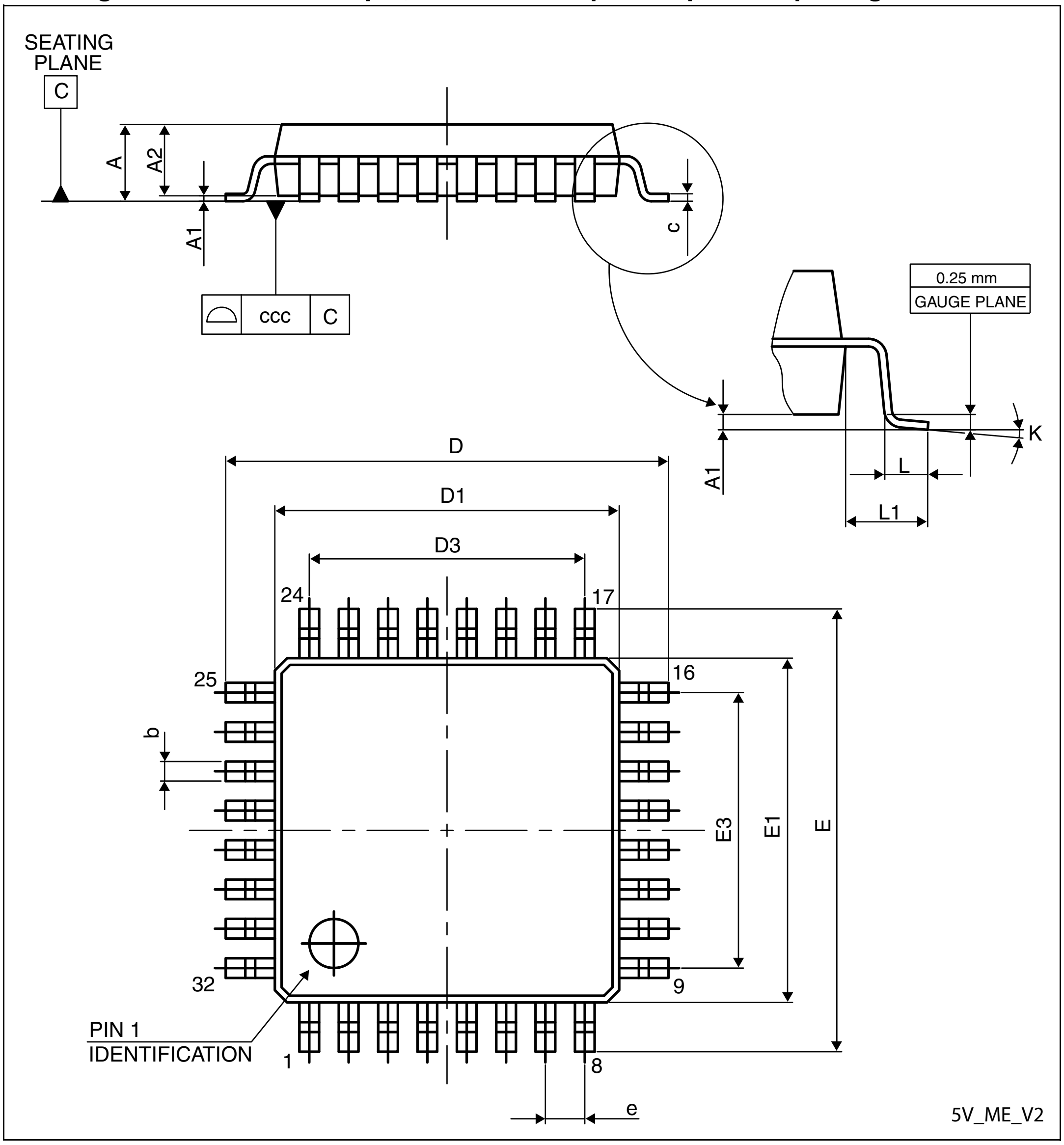
Figure 37. Typical connection diagram using the ADC



1. Refer to *Table 56* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

10.3 LQFP32 package information

Figure 44. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline



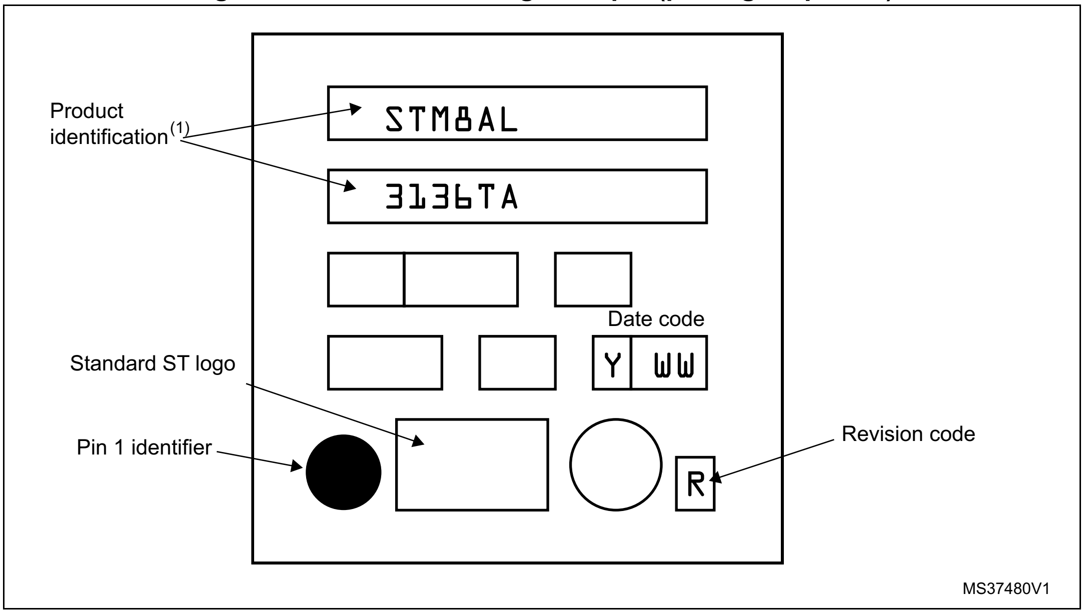
1. Drawing is not to scale.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

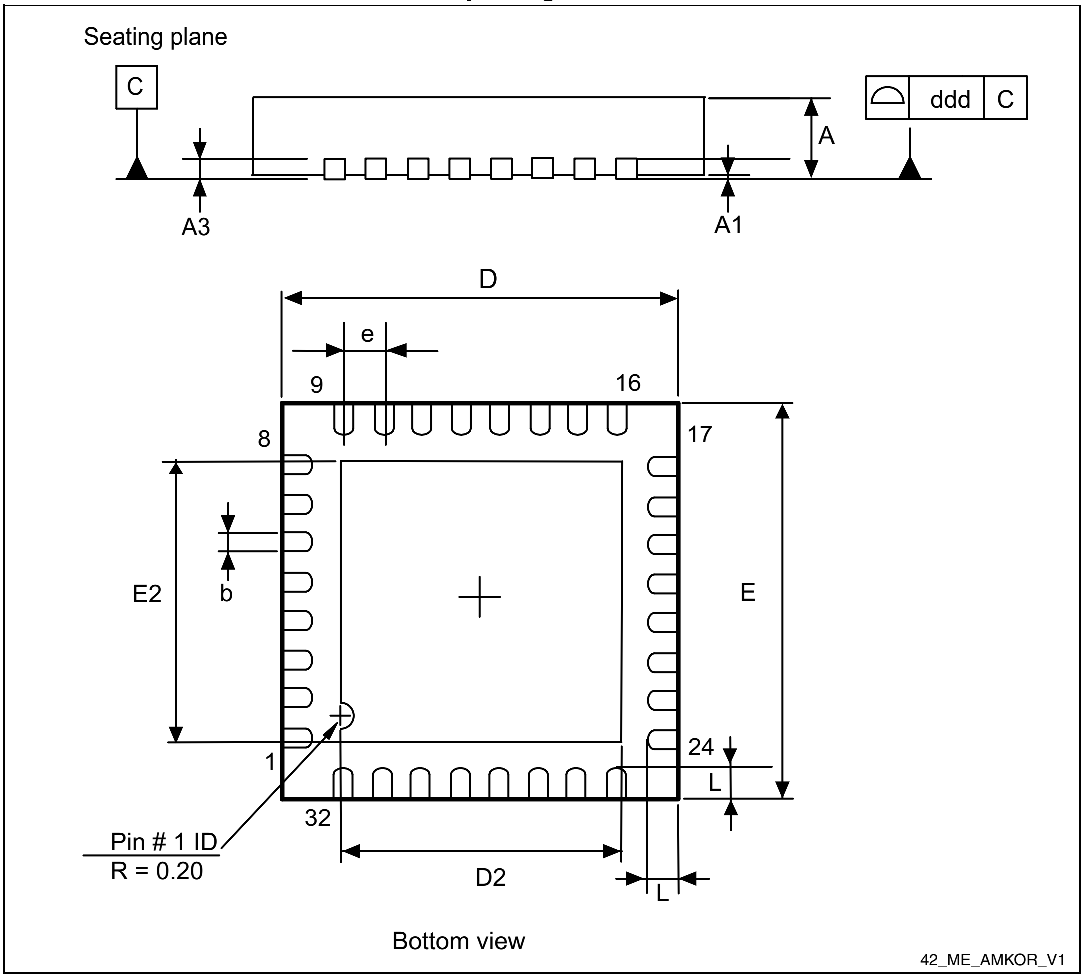
Figure 46. LQFP32 marking example (package top view)



1. Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

10.4 VFQFPN32 package information

Figure 47. VFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch very thin profile fine pitch quad flat package outline



1. Drawing is not to scale.
2. There is an exposed die pad on the underside of the VQFPN package. It is recommended to connect and solder this backside pad to the PCB ground.

10.5 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 19: General operating conditions*.

The maximum chip-junction temperature, T_{Jmax}, in degree Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma(V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,

  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 68. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP48- 7 x 7 mm	65	°C/W
	Thermal resistance junction-ambient LQFP32 - 7 x 7 mm	59	
	Thermal resistance junction-ambient VFQFPN32 - 5 x 5 mm	62	

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.