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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x12b SAR
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08dn16aclc

1.2 MCU Block Diagram

Figure 1-1 is the MC9S08DN60 Series system-level block diagram.

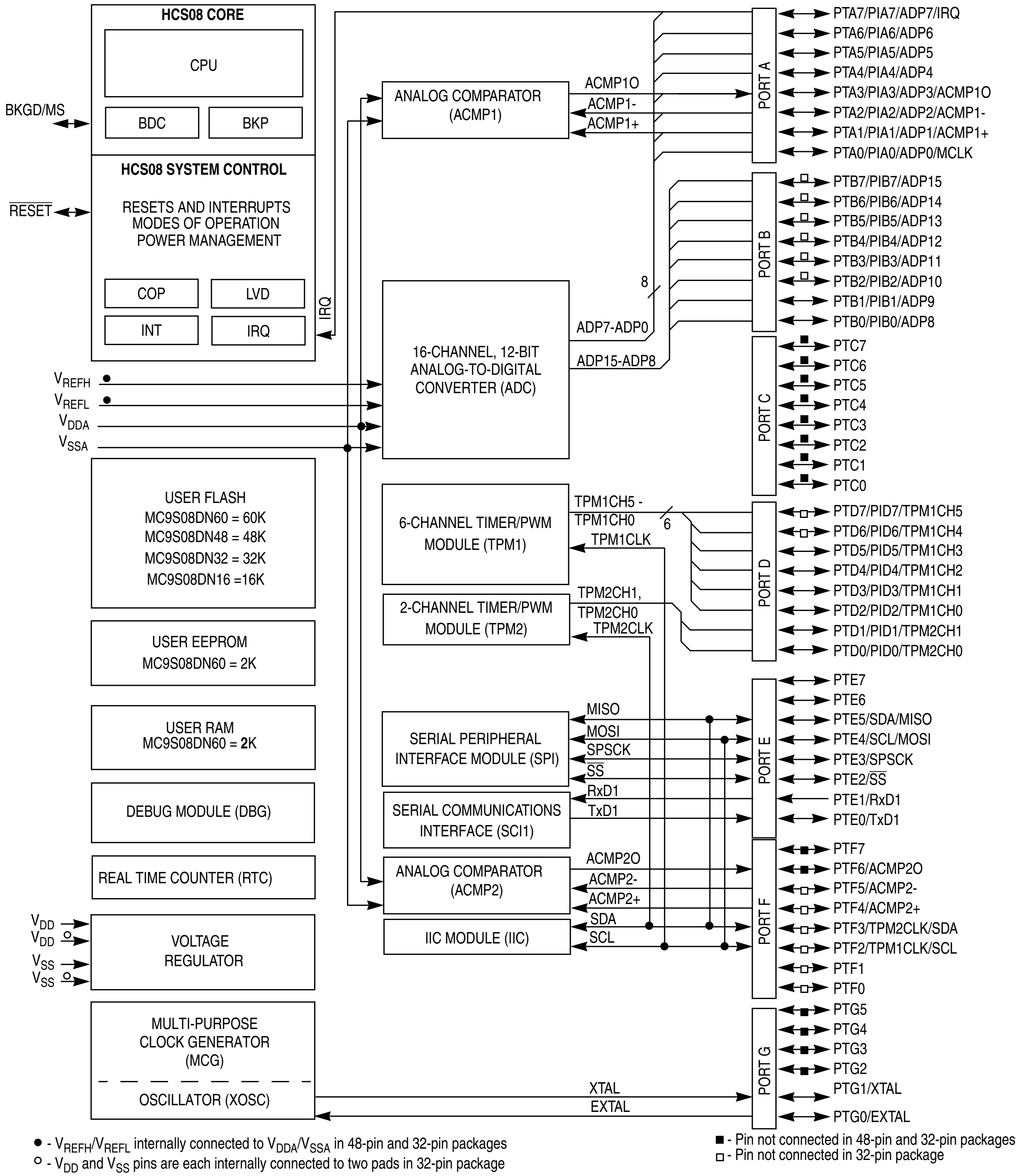


Figure 1-1. MC9S08DN60 Block Diagram

Table 2-1. Pin Availability by Package Pin-Count

Pin Number			<-- Lowest	Priority		--> Highest
64	48	32	Port Pin/Interrupt		Alt 1	Alt 2
1	1	—	PTB6	PIB6	ADP14	
2	—	—	PTC5			
3	2	1	PTA7	PIA7	ADP7	IRQ
4	—	—	PTC6			
5	3	—	PTB7	PIB7	ADP15	
6	—	—	PTC7			
7	4	2				V_{DD}
8	5	3				V_{SS}
9	6	4	PTG0		EXTAL	
10	7	5	PTG1		XTAL	
11	8	6				$\overline{RESET}$
12	9	—	PTF4			ACMP2+
13	10	—	PTF5			ACMP2-
14	—	—	PTF6			ACMP2O
15	11	7	PTE0		TxD1	
16	12	8	PTE1[2]		RxD1[2]	
17	13	9	PTE2			$\overline{SS}$
18	14	10	PTE3			SPSCK
19	15	11	PTE4		SCL[3]	MOSI
20	16	12	PTE5		SDA[3]	MISO
21	—	—	PTG2			
22	—	—	PTG3			
23	17	—	PTF0			
24	18	—	PTF1			
25	19	—	PTF2		TPM1CLK	SCL[3]
26	20	—	PTF3		TPM2CLK	SDA[3]
27	—	—	PTG4			
28	—	—	PTG5			
29	21	13	PTE6			
30	22	14	PTE7			
31	23	15	PTD0	PID0		TPM2CH0
32	24	16	PTD1	PID1		TPM2CH1
33	25	17	PTD2	PID2		TPM1CH0
34	26	18	PTD3	PID3		TPM1CH1
35	27	19	PTD4	PID4		TPM1CH2
36	28	20	PTD5	PID5		TPM1CH3
37	—	—	PTF7			
38	29	—				V_{SS}
39	30	—				V_{DD}
40	31	—	PTD6	PID6		TPM1CH4
41	32	—	PTD7	PID7		TPM1CH5
42	33	21			BKGD	MS
43	—	—	PTC0			
44	34	22	PTB0	PIB0	ADP8	
45	—	—	PTC1			
46	35	23	PTA0	PIA0	ADP0	MCLK
47	—	—	PTC2			
48	36	24	PTB1	PIB1	ADP9	
49	37	25	PTA1	PIA1	ADP1[1]	ACMP1+[1]
50	38	—	PTB2	PIB2	ADP10	
51	39	26	PTA2	PIA2	ADP2[1]	ACMP1-[1]
52	—	—	PTC3			
53	40	—	PTB3	PIB3	ADP11	
54	41	27	PTA3	PIA3	ADP3	ACMP1O
55	42	28				V_{SSA}
56						V_{REFL}
57	43	29				V_{REFH}
58						V_{DDA}
59	44	30	PTA4	PIA4	ADP4	
60	45	—	PTB4	PIB4	ADP12	
61	—	—	PTC4			
62	46	31	PTA5	PIA5	ADP5	
63	47	—	PTB5	PIB5	ADP13	
64	48	32	PTA6	PIA6	ADP6	

1. If both of these analog modules are enabled, they both will have access to the pin.
2. Pin does not contain a clamp diode to V_{DD} and should not be driven above V_{DD}. The voltage measured on this pin when internal pull-up is enabled may be as low as V_{DD} – 0.7 V. The internal gates connected to this pin are pulled to V_{DD}.
3. The IIC module pins can be repositioned using IICPS bit in the SOPT1 register. The default reset locations are on PTF2 and PTF3.

3.6 Stop Modes

One of two stop modes is entered upon execution of a STOP instruction when the STOPE bit in SOPT1 register is set. In both stop modes, all internal clocks are halted. The MCG module can be configured to leave the reference clocks running. See Chapter 8, “Multi-Purpose Clock Generator (S08MCGV1),” for more information.

Table 3-1 shows all of the control bits that affect stop mode selection and the mode selected under various conditions. The selected mode is entered following the execution of a STOP instruction.

Table 3-1. Stop Mode Selection

STOPE	ENBDM [1]	LVDE	LVDSE	PPDC	Stop Mode
0	x	x		x	Stop modes disabled; illegal opcode reset if STOP instruction executed
1	1	x		x	Stop3 with BDM enabled [2]
1	0	Both bits must be 1		x	Stop3 with voltage regulator active
1	0	Either bit a 0		0	Stop3
1	0	Either bit a 0		1	Stop2

[1] ENBDM is located in the BDCSCR, which is only accessible through BDC commands, see Section 16.4.1.1, “BDC Status and Control Register (BDCSCR)”.

[2] When in Stop3 mode with BDM enabled, The S_{IDD} will be near R_{IDD} levels because internal clocks are enabled.

3.6.1 Stop3 Mode

Stop3 mode is entered by executing a STOP instruction under the conditions as shown in Table 3-1. The states of all of the internal registers and logic, RAM contents, and I/O pin states are maintained.

Exit from stop3 is done by asserting $\overline{\text{RESET}}$ or an asynchronous interrupt pin. The asynchronous interrupt pins are IRQ, PIA0–PIA7, PIB0–PIB7, and PID0–PID7. Exit from stop3 can also be done by the low-voltage detect (LVD) reset, low-voltage warning (LVW) interrupt, ADC conversion complete interrupt, real-time clock (RTC) interrupt or SCI receiver interrupt.

If stop3 is exited by means of the $\overline{\text{RESET}}$ pin, the MCU will be reset and operation will resume after fetching the reset vector. Exit by means of an interrupt will result in the MCU fetching the appropriate interrupt vector.

3.6.1.1 LVD Enabled in Stop3 Mode

The LVD system is capable of generating either an interrupt or a reset when the supply voltage drops below the LVD voltage. If the LVD is enabled in stop (LVDE and LVDSE bits in SPMSC1 both set) at the time the CPU executes a STOP instruction, then the voltage regulator remains active during stop mode.

For the ADC to operate the LVD must be left enabled when entering stop3.

Chapter 6
Parallel Input/Output Control

This section explains software controls related to parallel input/output (I/O) and pin control. The MC9S08DN60 Series has seven parallel I/O ports which include a total of up to 53 I/O pins and one input-only pin. See Chapter 2, “Pins and Connections,” for more information about pin assignments and external hardware considerations of these pins.

Many of these pins are shared with on-chip peripherals such as timer systems, communication systems, or pin interrupts as shown in Table 2-1. The peripheral modules have priority over the general-purpose I/O functions so that when a peripheral is enabled, the I/O functions associated with the shared pins are disabled.

After reset, the shared peripheral functions are disabled and the pins are configured as inputs (PTxDDn = 0). The pin control functions for each pin are configured as follows: slew rate control enabled (PTxSEn = 1), low drive strength selected (PTxDSn = 0), and internal pull-ups disabled (PTxPEn = 0).

NOTE

- Not all general-purpose I/O pins are available on all packages. To avoid extra current drain from floating input pins, the user’s reset initialization routine in the application program must either enable on-chip pull-up devices or change the direction of unconnected pins to outputs so the pins do not float.
- The PTE1 pin does not contain a clamp diode to V_{DD} and should not be driven above V_{DD}. The voltage measured on the internally pulled up PTE1 pin may be as low as V_{DD} – 0.7 V. The internal gates connected to this pin are pulled all the way to V_{DD}.

6.1 Port Data and Data Direction

Reading and writing of parallel I/Os are performed through the port data registers. The direction, either input or output, is controlled through the port data direction registers. The parallel I/O port function for an individual pin is illustrated in the block diagram shown in Figure 6-1.

The data direction control bit (PTxDDn) determines whether the output buffer for the associated pin is enabled, and also controls the source for port data register reads. The input buffer for the associated pin is always enabled unless the pin is enabled as an analog function or is an output-only pin.

When a shared digital function is enabled for a pin, the output buffer is controlled by the shared function. However, the data direction register bit will continue to control the source for reads of the port data register.

When a shared analog function is enabled for a pin, both the input and output buffers are disabled. A value of 0 is read for any port data bit where the bit is an input (PTxDDn = 0) and the input buffer is disabled.

6.5.1.7 Port A Interrupt Pin Select Register (PTAPS)

	7	6	5	4	3	2	1	0
R W	PTAPS7	PTAPS6	PTAPS5	PTAPS4	PTAPS3	PTAPS2	PTAPS1	PTAPS0
Reset:	0	0	0	0	0	0	0	0

Figure 6-9. Port A Interrupt Pin Select Register (PTAPS)

Table 6-7. PTAPS Register Field Descriptions

Field	Description
7:0 PTAPS[7:0]	**Port A Interrupt Pin Selects** — Each of the PTAPSn bits enable the corresponding port A interrupt pin. 0 Pin not enabled as interrupt. 1 Pin enabled as interrupt.

6.5.1.8 Port A Interrupt Edge Select Register (PTAES)

	7	6	5	4	3	2	1	0
R W	PTAES7	PTAES6	PTAES5	PTAES4	PTAES3	PTAES2	PTAES1	PTAES0
Reset:	0	0	0	0	0	0	0	0

Figure 6-10. Port A Edge Select Register (PTAES)

Table 6-8. PTAES Register Field Descriptions

Field	Description
7:0 PTAES[7:0]	**Port A Edge Selects** — Each of the PTAESn bits serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled. 0 A pull-up device is connected to the associated pin and detects falling edge/low level for interrupt generation. 1 A pull-down device is connected to the associated pin and detects rising edge/high level for interrupt generation.

6.5.7.3 Port G Pull Enable Register (PTGPE)

	7	6	5	4	3	2	1	0
R	0	0	PTGPE5	PTGPE4	PTGPE3	PTGPE2	PTGPE1	PTGPE0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 6-44. Internal Pull Enable for Port G Register (PTGPE)

Table 6-42. PTGPE Register Field Descriptions

Field	Description
5:0 PTGPE[5:0]	**Internal Pull Enable for Port G Bits** — Each of these control bits determines if the internal pull-up device is enabled for the associated PTG pin. For port G pins that are configured as outputs, these bits have no effect and the internal pull devices are disabled. 0 Internal pull-up device disabled for port G bit n. 1 Internal pull-up device enabled for port G bit n.

NOTE

Pull-down devices only apply when using pin interrupt functions, when corresponding edge select and pin select functions are configured.

6.5.7.4 Port G Slew Rate Enable Register (PTGSE)

	7	6	5	4	3	2	1	0
R	0	0	PTGSE5	PTGSE4	PTGSE3	PTGSE2	PTGSE1	PTGSE0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

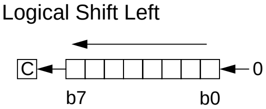
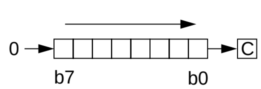
Figure 6-45. Slew Rate Enable for Port G Register (PTGSE)

Table 6-43. PTGSE Register Field Descriptions

Field	Description
5:0 PTGSE[5:0]	**Output Slew Rate Enable for Port G Bits** — Each of these control bits determines if the output slew rate control is enabled for the associated PTG pin. For port G pins that are configured as inputs, these bits have no effect. 0 Output slew rate control disabled for port G bit n. 1 Output slew rate control enabled for port G bit n.

Note: Slew rate reset default values may differ between engineering samples and final production parts. Always initialize slew rate control to the desired value to ensure correct operation.

Table 7-2. Instruction Set Summary (Sheet 5 of 9)

Source Form	Operation	Address Mode	Object Code	Cycles	Cyc-by-Cyc Details	Affect on CCR V 1 1 H	Affect on CCR I N Z C
INC *opr8a*	Increment M ← (M) + $01	DIR	3C dd	5	rfwpp	↕ 1 1 –	– ↕ ↕ –
INCA	A ← (A) + $01	INH	4C	1	p		
INCX	X ← (X) + $01	INH	5C	1	p		
INC *oprx8*,X	M ← (M) + $01	IX1	6C ff	5	rfwpp		
INC ,X	M ← (M) + $01	IX	7C	4	rfwp		
INC *oprx8*,SP	M ← (M) + $01	SP1	9E 6C ff	6	prfwpp		
JMP *opr8a*	Jump PC ← Jump Address	DIR	BC dd	3	ppp	– 1 1 –	– – – –
JMP *opr16a*		EXT	CC hh ll	4	pppp		
JMP *oprx16*,X		IX2	DC ee ff	4	pppp		
JMP *oprx8*,X		IX1	EC ff	3	ppp		
JMP ,X		IX	FC	3	ppp		
JSR *opr8a*	Jump to Subroutine	DIR	BD dd	5	ssppp	– 1 1 –	– – – –
JSR *opr16a*	PC ← (PC) + *n* (*n* = 1, 2, or 3)	EXT	CD hh ll	6	pssppp		
JSR *oprx16*,X	Push (PCL); SP ← (SP) – $0001	IX2	DD ee ff	6	pssppp		
JSR *oprx8*,X	Push (PCH); SP ← (SP) – $0001	IX1	ED ff	5	ssppp		
JSR ,X	PC ← Unconditional Address	IX	FD	5	ssppp		
LDA #*opr8i*	Load Accumulator from Memory A ← (M)	IMM	A6 ii	2	pp	0 1 1 –	– ↕ ↕ –
LDA *opr8a*		DIR	B6 dd	3	rpp		
LDA *opr16a*		EXT	C6 hh ll	4	prpp		
LDA *oprx16*,X		IX2	D6 ee ff	4	prpp		
LDA *oprx8*,X		IX1	E6 ff	3	rpp		
LDA ,X		IX	F6	3	rfp		
LDA *oprx16*,SP		SP2	9E D6 ee ff	5	pprpp		
LDA *oprx8*,SP		SP1	9E E6 ff	4	prpp		
LDHX #*opr16i*	Load Index Register (H:X) H:X ← (M:M + $0001)	IMM	45 jj kk	3	ppp	0 1 1 –	– ↕ ↕ –
LDHX *opr8a*		DIR	55 dd	4	rrpp		
LDHX *opr16a*		EXT	32 hh ll	5	prrpp		
LDHX ,X		IX	9E AE	5	prrfp		
LDHX *oprx16*,X		IX2	9E BE ee ff	6	pprrpp		
LDHX *oprx8*,X		IX1	9E CE ff	5	prrpp		
LDHX *oprx8*,SP		SP1	9E FE ff	5	prrpp		
LDX #*opr8i*	Load X (Index Register Low) from Memory X ← (M)	IMM	AE ii	2	pp	0 1 1 –	– ↕ ↕ –
LDX *opr8a*		DIR	BE dd	3	rpp		
LDX *opr16a*		EXT	CE hh ll	4	prpp		
LDX *oprx16*,X		IX2	DE ee ff	4	prpp		
LDX *oprx8*,X		IX1	EE ff	3	rpp		
LDX ,X		IX	FE	3	rfp		
LDX *oprx16*,SP		SP2	9E DE ee ff	5	pprpp		
LDX *oprx8*,SP		SP1	9E EE ff	4	prpp		
LSL *opr8a*	Logical Shift Left  (Same as ASL)	DIR	38 dd	5	rfwpp	↕ 1 1 –	– ↕ ↕ ↕
LSLA		INH	48	1	p		
LSLX		INH	58	1	p		
LSL *oprx8*,X		IX1	68 ff	5	rfwpp		
LSL ,X		IX	78	4	rfwp		
LSL *oprx8*,SP		SP1	9E 68 ff	6	prfwpp		
LSR *opr8a*	Logical Shift Right 	DIR	34 dd	5	rfwpp	↕ 1 1 –	– 0 ↕ ↕
LSRA		INH	44	1	p		
LSRX		INH	54	1	p		
LSR *oprx8*,X		IX1	64 ff	5	rfwpp		
LSR ,X		IX	74	4	rfwp		
LSR *oprx8*,SP		SP1	9E 64 ff	6	prfwpp		

8.4.7 Fixed Frequency Clock

The MCG presents the divided reference clock as MCGFFCLK for use as an additional clock source. The MCGFFCLK frequency must be no more than 1/4 of the MCGOUT frequency to be valid. Because of this requirement, the MCGFFCLK is not valid in bypass modes for the following combinations of BDIV and RDIV values:

- BDIV=00 (divide by 1), RDIV < 010
- BDIV=01 (divide by 2), RDIV < 011

When MCGFFCLK is valid then MCGFFCLKVALID is set to 1. When MCGFFCLK is not valid then MCGFFCLKVALID is set to 0.

8.5 Initialization / Application Information

This section describes how to initialize and configure the MCG module in application. The following sections include examples on how to initialize the MCG and properly switch between the various available modes.

8.5.1 MCG Module Initialization Sequence

The MCG comes out of reset configured for FEI mode with the BDIV set for divide-by-2. The internal reference will stabilize in t_{irefst} microseconds before the FLL can acquire lock. As soon as the internal reference is stable, the FLL will acquire lock in t_{fll_lock} milliseconds.

Upon POR, the internal reference will require trimming to guarantee an accurate clock. Freescale recommends using FLASH location 0xFFAE for storing the fine trim bit, FTRIM in the MCGSC register, and 0xFFAF for storing the 8-bit trim value in the MCGTRM register. The MCU will not automatically copy the values in these FLASH locations to the respective registers. Therefore, user code must copy these values from FLASH to the registers.

NOTE

The BDIV value should not be changed to divide-by-1 without first trimming the internal reference. Failure to do so could result in the MCU running out of specification.

8.5.1.1 Initializing the MCG

Because the MCG comes out of reset in FEI mode, the only MCG modes which can be directly switched to upon reset are FEE, FBE, and FBI modes (see Figure 8-8). Reaching any of the other modes requires first configuring the MCG for one of these three initial modes. Care must be taken to check relevant status bits in the MCGSC register reflecting all configuration changes within each mode.

To change from FEI mode to FEE or FBE modes, follow this procedure:

1. Enable the external clock source by setting the appropriate bits in MCGC2.
2. Write to MCGC1 to select the clock mode.

9.3 Memory Map/Register Definition

The ACMP includes one register:

- An 8-bit status and control register

Refer to the direct-page register summary in the memory section of this document for the absolute address assignments for the ACMP register.This section refers to register and control bits only by their names and relative address offsets.

Some MCUs may have more than one ACMP, so register names include placeholder characters (x) to identify which ACMP is being referenced.

Table 9-2. ACMP Register Summary

Name		7	6	5	4	3	2	1	0
ACMPxSC	R	ACME	ACBGS	ACF	ACIE	ACO	ACOPE	ACMOD	
	W								

9.3.1 ACMPx Status and Control Register (ACMPxSC)

ACMPxSC contains the status flag and control bits used to enable and configure the ACMP.

	7	6	5	4	3	2	1	0
R	ACME	ACBGS	ACF	ACIE	ACO	ACOPE	ACMOD	
W								
Reset:	0	0	0	0	0	0	0	0

Figure 9-3. ACMPx Status and Control Register (ACMPxSC)

Table 9-3. ACMPxSC Field Descriptions

Field	Description
7 ACME	Analog Comparator Module Enable. Enables the ACMP module. 0 ACMP not enabled 1 ACMP is enabled
6 ACBGS	Analog Comparator Bandgap Select. Selects between the bandgap reference voltage or the ACMPx+ pin as the input to the non-inverting input of the analog comparator. 0 External pin ACMPx+ selected as non-inverting input to comparator 1 Internal reference select as non-inverting input to comparator
5 ACF	Analog Comparator Flag. ACF is set when a compare event occurs. Compare events are defined by ACMOD. ACF is cleared by writing a one to it. 0 Compare event has not occurred 1 Compare event has occurred
4 ACIE	Analog Comparator Interrupt Enable. Enables the interrupt from the ACMP. When ACIE is set, an interrupt is asserted when ACF is set. 0 Interrupt disabled 1 Interrupt enabled

Table 9-3. ACMPxSC Field Descriptions (continued)

Field	Description
3 ACO	Analog Comparator Output. Reading ACO returns the current value of the analog comparator output. ACO is reset to a 0 and reads as a 0 when the ACMP is disabled (ACME = 0).
2 ACOPE	Analog Comparator Output Pin Enable. Enables the comparator output to be placed onto the external pin, ACMPxO. 0 Analog comparator output not available on ACMPxO 1 Analog comparator output is driven out on ACMPxO
1:0 ACMOD	Analog Comparator Mode. ACMOD selects the type of compare event which sets ACF. 00 Encoding 0 — Comparator output falling edge 01 Encoding 1 — Comparator output rising edge 10 Encoding 2 — Comparator output falling edge 11 Encoding 3 — Comparator output rising or falling edge

9.4 Functional Description

The analog comparator can compare two analog input voltages applied to ACMPx+ and ACMPx–, or it can compare an analog input voltage applied to ACMPx– with an internal bandgap reference voltage. ACBGS selects between the bandgap reference voltage or the ACMPx+ pin as the input to the non-inverting input of the analog comparator. The comparator output is high when the non-inverting input is greater than the inverting input, and is low when the non-inverting input is less than the inverting input. ACMOD selects the condition that causes ACF to be set. ACF can be set on a rising edge of the comparator output, a falling edge of the comparator output, or a rising or a falling edge (toggle). The comparator output can be read directly through ACO. The comparator output can be driven onto the ACMPxO pin using ACOPE.

Table 10-12. APCTL3 Register Field Descriptions

Field	Description
7 ADPC23	ADC Pin Control 23. ADPC23 controls the pin associated with channel AD23. 0 AD23 pin I/O control enabled 1 AD23 pin I/O control disabled
6 ADPC22	ADC Pin Control 22. ADPC22 controls the pin associated with channel AD22. 0 AD22 pin I/O control enabled 1 AD22 pin I/O control disabled
5 ADPC21	ADC Pin Control 21. ADPC21 controls the pin associated with channel AD21. 0 AD21 pin I/O control enabled 1 AD21 pin I/O control disabled
4 ADPC20	ADC Pin Control 20. ADPC20 controls the pin associated with channel AD20. 0 AD20 pin I/O control enabled 1 AD20 pin I/O control disabled
3 ADPC19	ADC Pin Control 19. ADPC19 controls the pin associated with channel AD19. 0 AD19 pin I/O control enabled 1 AD19 pin I/O control disabled
2 ADPC18	ADC Pin Control 18. ADPC18 controls the pin associated with channel AD18. 0 AD18 pin I/O control enabled 1 AD18 pin I/O control disabled
1 ADPC17	ADC Pin Control 17. ADPC17 controls the pin associated with channel AD17. 0 AD17 pin I/O control enabled 1 AD17 pin I/O control disabled
0 ADPC16	ADC Pin Control 16. ADPC16 controls the pin associated with channel AD16. 0 AD16 pin I/O control enabled 1 AD16 pin I/O control disabled

10.4 Functional Description

The ADC module is disabled during reset or when the ADCH bits are all high. The module is idle when a conversion has completed and another conversion has not been initiated. When idle, the module is in its lowest power state.

The ADC can perform an analog-to-digital conversion on any of the software selectable channels. In 12-bit and 10-bit mode, the selected channel voltage is converted by a successive approximation algorithm into a 12-bit digital result. In 8-bit mode, the selected channel voltage is converted by a successive approximation algorithm into a 9-bit digital result.

When the conversion is completed, the result is placed in the data registers (ADCRH and ADCRL). In 10-bit mode, the result is rounded to 10 bits and placed in the data registers (ADCRH and ADCRL). In 8-bit mode, the result is rounded to 8 bits and placed in ADCRL. The conversion complete flag (COCO) is then set and an interrupt is generated if the conversion complete interrupt has been enabled (AIEN = 1).

The ADC module has the capability of automatically comparing the result of a conversion with the contents of its compare registers. The compare function is enabled by setting the ACFE bit and operates with any of the conversion modes and configurations.

Table 11-8. IICC2 Field Descriptions

Field	Description
7 GCAEN	**General Call Address Enable.** The GCAEN bit enables or disables general call address. 0 General call address is disabled 1 General call address is enabled
6 ADEXT	**Address Extension.** The ADEXT bit controls the number of bits used for the slave address. 0 7-bit address scheme 1 10-bit address scheme
2–0 AD[10:8]	Slave Address. The AD[10:8] field contains the upper three bits of the slave address in the 10-bit address scheme. This field is only valid when the ADEXT bit is set.

11.4 Functional Description

This section provides a complete functional description of the IIC module.

11.4.1 IIC Protocol

The IIC bus system uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. All devices connected to it must have open drain or open collector outputs. A logic AND function is exercised on both lines with external pull-up resistors. The value of these resistors is system dependent.

Normally, a standard communication is composed of four parts:

- Start signal
- Slave address transmission
- Data transfer
- Stop signal

The stop signal should not be confused with the CPU stop instruction. The IIC bus system communication is described briefly in the following sections and illustrated in Figure 11-9.

message characters. At the end of a message, or at the beginning of the next message, all receivers automatically force RWU to 0 so all receivers wake up in time to look at the first character(s) of the next message.

13.3.3.2.1 Idle-Line Wakeup

When WAKE = 0, the receiver is configured for idle-line wakeup. In this mode, RWU is cleared automatically when the receiver detects a full character time of the idle-line level. The M control bit selects 8-bit or 9-bit data mode that determines how many bit times of idle are needed to constitute a full character time (10 or 11 bit times because of the start and stop bits).

When RWU is one and RWUID is zero, the idle condition that wakes up the receiver does not set the IDLE flag. The receiver wakes up and waits for the first data character of the next message which will set the RDRF flag and generate an interrupt if enabled. When RWUID is one, any idle condition sets the IDLE flag and generates an interrupt if enabled, regardless of whether RWU is zero or one.

The idle-line type (ILT) control bit selects one of two ways to detect an idle line. When ILT = 0, the idle bit counter starts after the start bit so the stop bit and any logic 1s at the end of a character count toward the full character time of idle. When ILT = 1, the idle bit counter does not start until after a stop bit time, so the idle detection is not affected by the data in the last character of the previous message.

13.3.3.2.2 Address-Mark Wakeup

When WAKE = 1, the receiver is configured for address-mark wakeup. In this mode, RWU is cleared automatically when the receiver detects a logic 1 in the most significant bit of a received character (eighth bit in M = 0 mode and ninth bit in M = 1 mode).

Address-mark wakeup allows messages to contain idle characters but requires that the MSB be reserved for use in address frames. The logic 1 MSB of an address frame clears the RWU bit before the stop bit is received and sets the RDRF flag. In this case the character with the MSB set is received even though the receiver was sleeping during most of this character time.

13.3.4 Interrupts and Status Flags

The SCI system has three separate interrupt vectors to reduce the amount of software needed to isolate the cause of the interrupt. One interrupt vector is associated with the transmitter for TDRE and TC events. Another interrupt vector is associated with the receiver for RDRF, IDLE, RXEDGIF and LBKDIF events, and a third vector is used for OR, NF, FE, and PF error conditions. Each of these ten interrupt sources can be separately masked by local interrupt enable masks. The flags can still be polled by software when the local masks are cleared to disable generation of hardware interrupt requests.

The SCI transmitter has two status flags that optionally can generate hardware interrupt requests. Transmit data register empty (TDRE) indicates when there is room in the transmit data buffer to write another transmit character to SCI1D. If the transmit interrupt enable (TIE) bit is set, a hardware interrupt will be requested whenever TDRE = 1. Transmit complete (TC) indicates that the transmitter is finished transmitting all data, preamble, and break characters and is idle with TxD at the inactive level. This flag is often used in systems with modems to determine when it is safe to turn off the modem. If the transmit complete interrupt enable (TCIE) bit is set, a hardware interrupt will be requested whenever TC = 1.

When the TPM is configured for center-aligned PWM (and ELSnB:ELSnA not = 0:0), the data direction for all channels in this TPM are overridden, the TPMxCHn pins are forced to be outputs controlled by the TPM, and the ELSnA bits control the polarity of each TPMxCHn output. If ELSnB:ELSnA=1:0, the corresponding TPMxCHn pin is cleared when the timer counter is counting up, and the channel value register matches the timer counter; the TPMxCHn pin is set when the timer counter is counting down, and the channel value register matches the timer counter. If ELSnA=1, the corresponding TPMxCHn pin is set when the timer counter is counting up and the channel value register matches the timer counter; the TPMxCHn pin is cleared when the timer counter is counting down and the channel value register matches the timer counter.

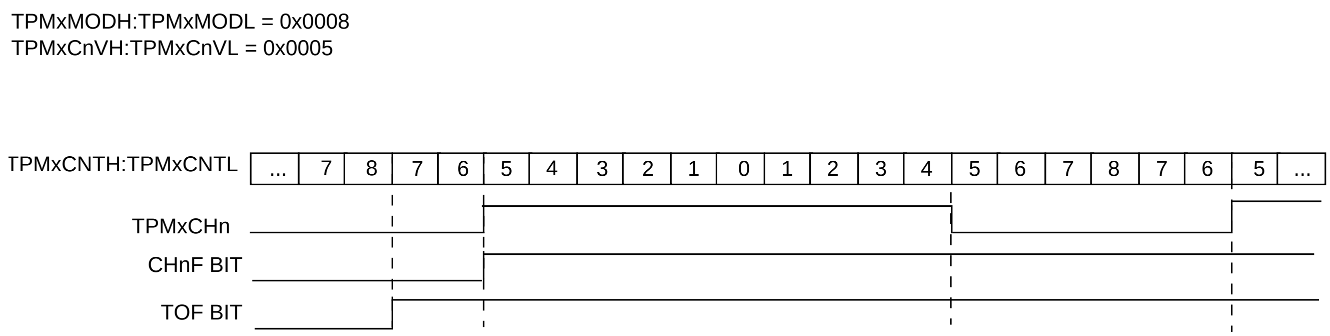


Figure 15-5. High-True Pulse of a Center-Aligned PWM

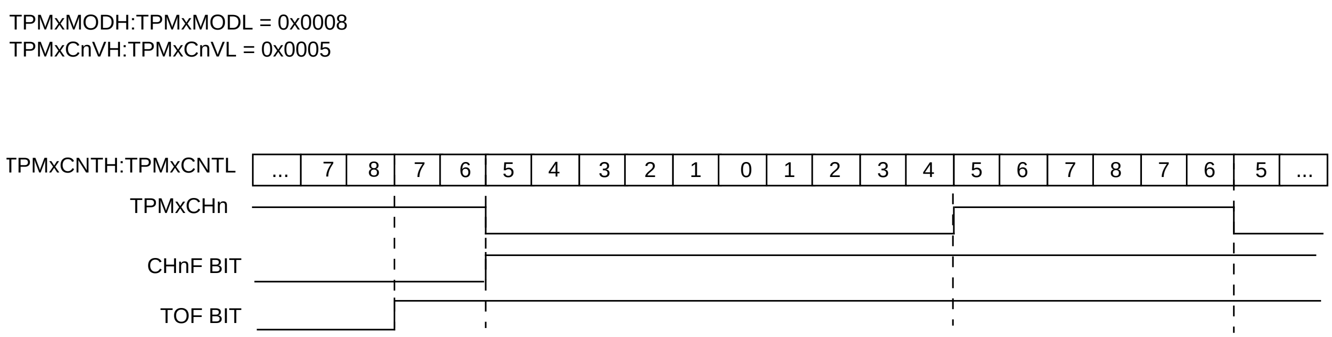


Figure 15-6. Low-True Pulse of a Center-Aligned PWM

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	1	Bit 0
W	Any write to TPMxCNTL clears the 16-bit counter							
Reset	0	0	0	0	0	0	0	0

Figure 15-9. TPM Counter Register Low (TPMxCNTL)

When BDM is active, the timer counter is frozen (this is the value that will be read by user); the coherency mechanism is frozen such that the buffer latches remain in the state they were in when the BDM became active, even if one or both counter halves are read while BDM is active. This assures that if the user was in the middle of reading a 16-bit register when BDM became active, it will read the appropriate value from the other half of the 16-bit value after returning to normal execution.

In BDM mode, writing any value to TPMxSC, TPMxCNTH or TPMxCNTL registers resets the read coherency mechanism of the TPMxCNTH:L registers, regardless of the data involved in the write.

15.3.3 TPM Counter Modulo Registers (TPMxMODH:TPMxMODL)

The read/write TPM modulo registers contain the modulo value for the TPM counter. After the TPM counter reaches the modulo value, the TPM counter resumes counting from 0x0000 at the next clock, and the overflow flag (TOF) becomes set. Writing to TPMxMODH or TPMxMODL inhibits the TOF bit and overflow interrupts until the other byte is written. Reset sets the TPM counter modulo registers to 0x0000 which results in a free running timer counter (modulo disabled).

Writing to either byte (TPMxMODH or TPMxMODL) latches the value into a buffer and the registers are updated with the value of their write buffer according to the value of CLKSB:CLKSA bits, so:

- If (CLKSB:CLKSA = 0:0), then the registers are updated when the second byte is written
- If (CLKSB:CLKSA not = 0:0), then the registers are updated after both bytes were written, and the TPM counter changes from (TPMxMODH:TPMxMODL - 1) to (TPMxMODH:TPMxMODL). If the TPM counter is a free-running counter, the update is made when the TPM counter changes from 0xFFFE to 0xFFFF

The latching mechanism may be manually reset by writing to the TPMxSC address (whether BDM is active or not).

When BDM is active, the coherency mechanism is frozen (unless reset by writing to TPMxSC register) such that the buffer latches remain in the state they were in when the BDM became active, even if one or both halves of the modulo register are written while BDM is active. Any write to the modulo registers bypasses the buffer latches and directly writes to the modulo register while BDM is active.

	7	6	5	4	3	2	1	0
R W	Bit 15	14	13	12	11	10	9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 15-10. TPM Counter Modulo Register High (TPMxMODH)

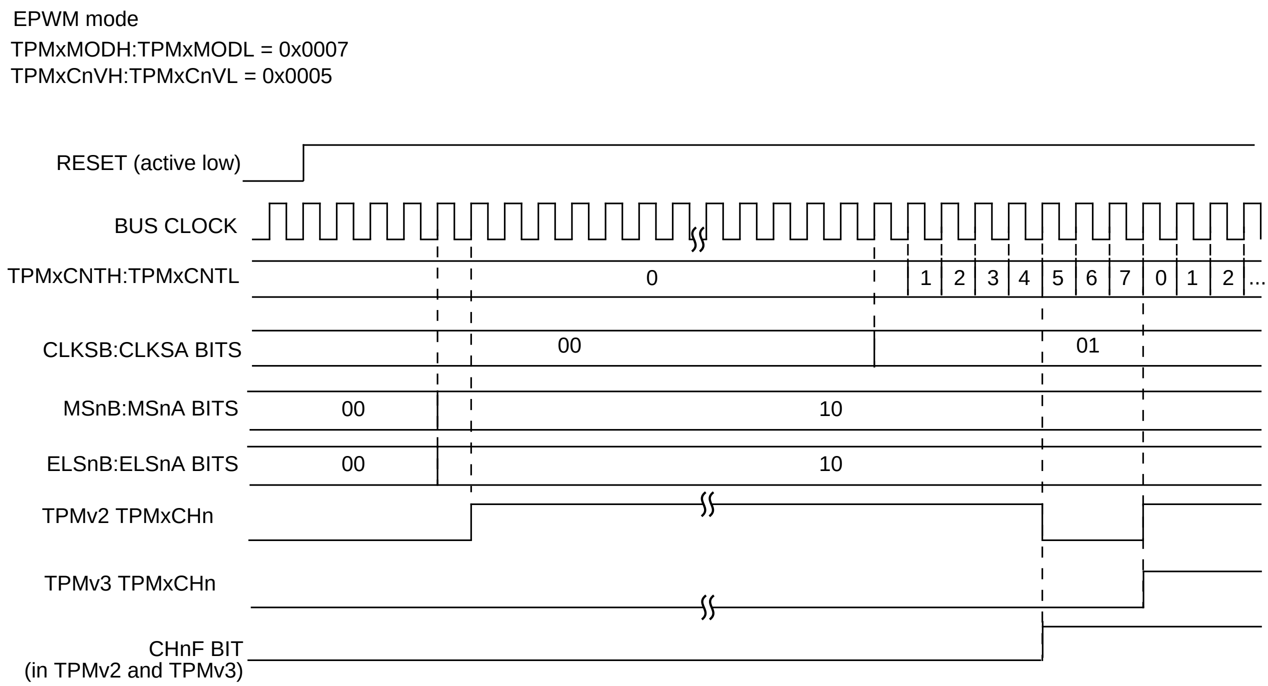


Figure 0-1. Generation of high-true EPWM signal by TPM v2 and v3 after the reset

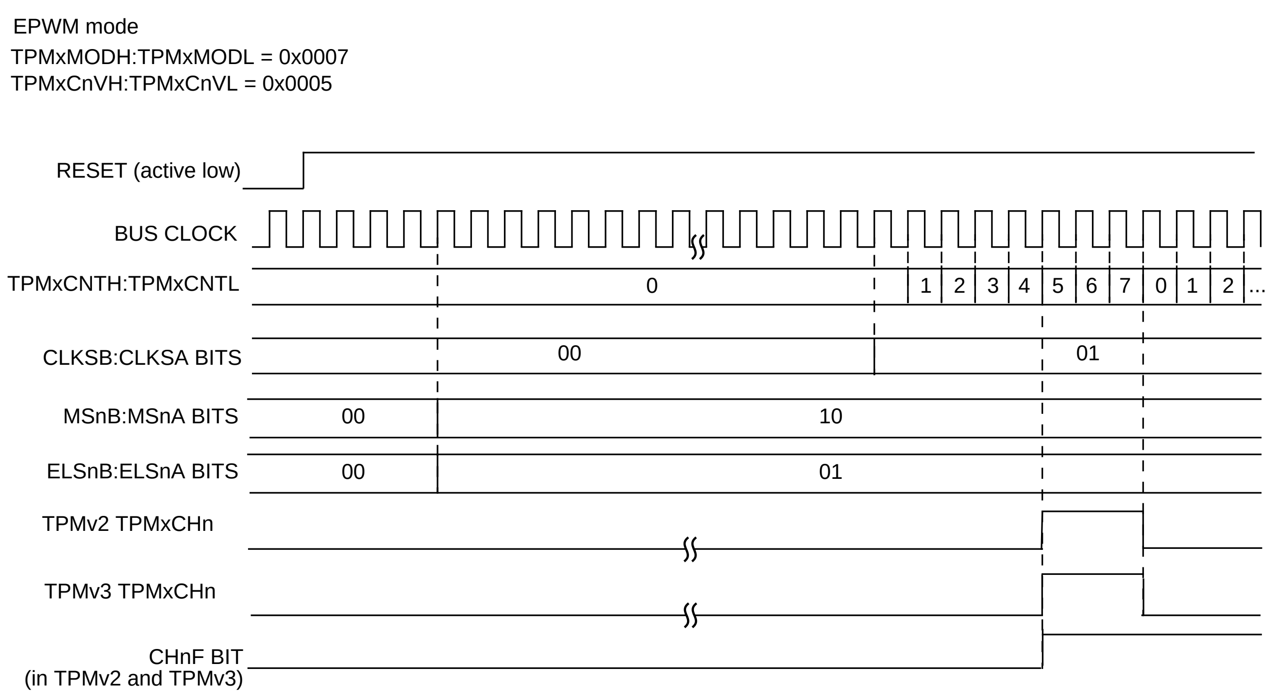


Figure 0-2. Generation of low-true EPWM signal by TPM v2 and v3 after the reset

The following procedure can be used in TPM v3 (when the channel pin is also a port pin) to emulate the high-true EPWM generated by TPM v2 after the reset.

16.1.2 Features

Features of the BDC module include:

- Single pin for mode selection and background communications
- BDC registers are not located in the memory map
- SYNC command to determine target communications rate
- Non-intrusive commands for memory access
- Active background mode commands for CPU register access
- GO and TRACE1 commands
- BACKGROUND command can wake CPU from stop or wait modes
- One hardware address breakpoint built into BDC
- Oscillator runs in stop mode, if BDC enabled
- COP watchdog disabled while in active background mode

Features of the ICE system include:

- Two trigger comparators: Two address + read/write (R/W) or one full address + data + R/W
- Flexible 8-word by 16-bit FIFO (first-in, first-out) buffer for capture information:
  — Change-of-flow addresses or
  — Event-only data
- Two types of breakpoints:
  — Tag breakpoints for instruction opcodes
  — Force breakpoints for any address access
- Nine trigger modes:
  — Basic: A-only, A OR B
  — Sequence: A then B
  — Full: A AND B data, A AND NOT B data
  — Event (store data): Event-only B, A then event-only B
  — Range: Inside range (A ≤ address ≤ B), outside range (address < A or address > B)

16.2 Background Debug Controller (BDC)

All MCUs in the HCS08 Family contain a single-wire background debug interface that supports in-circuit programming of on-chip nonvolatile memory and sophisticated non-intrusive debug capabilities. Unlike debug interfaces on earlier 8-bit MCUs, this system does not interfere with normal application resources. It does not use any user memory or locations in the memory map and does not share any on-chip peripherals.

BDC commands are divided into two groups:

- Active background mode commands require that the target MCU is in active background mode (the user program is not running). Active background mode commands allow the CPU registers to be read or written, and allow the user to trace one user instruction at a time, or GO to the user program from active background mode.

Figure 16-4 shows the host receiving a logic 0 from the target HCS08 MCU. Because the host is asynchronous to the target MCU, there is a 0-to-1 cycle delay from the host-generated falling edge on BKGD to the start of the bit time as perceived by the target MCU. The host initiates the bit time but the target HCS08 finishes it. Because the target wants the host to receive a logic 0, it drives the BKGD pin low for 13 BDC clock cycles, then briefly drives it high to speed up the rising edge. The host samples the bit level about 10 cycles after starting the bit time.

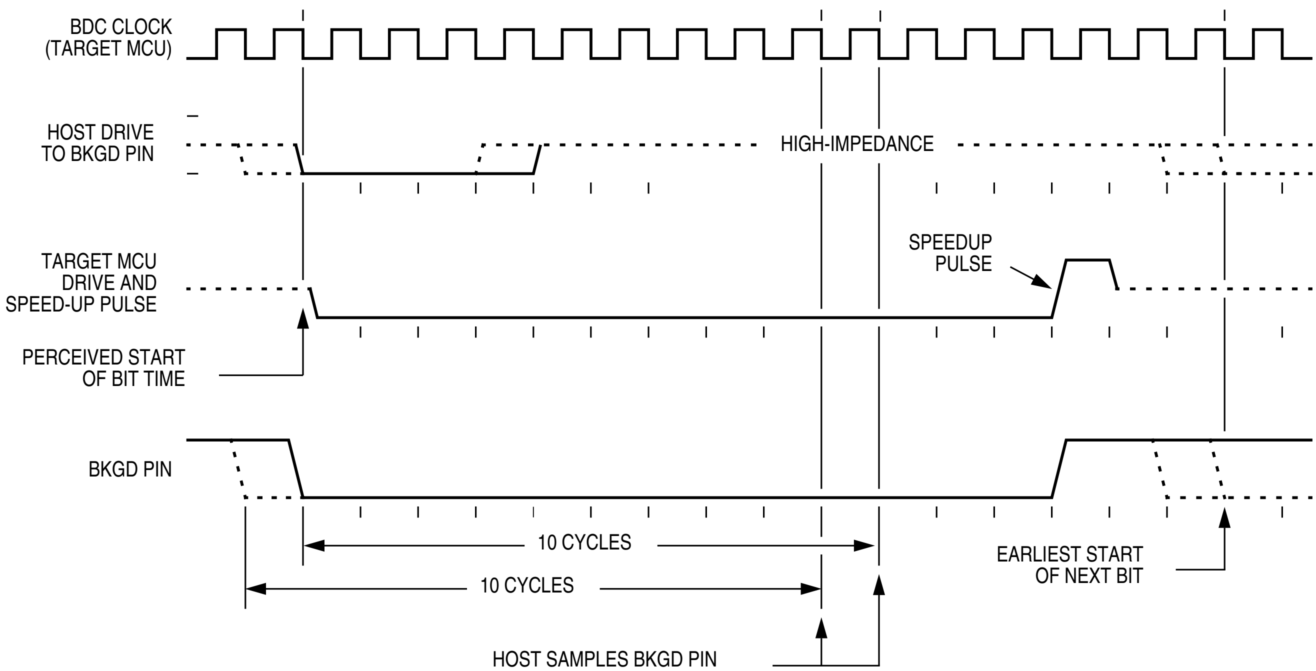
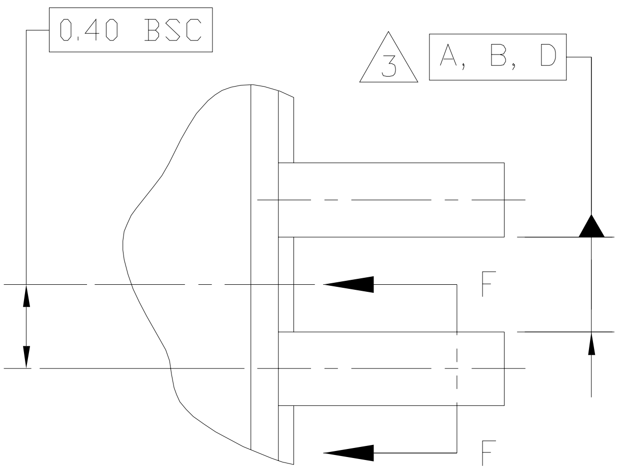
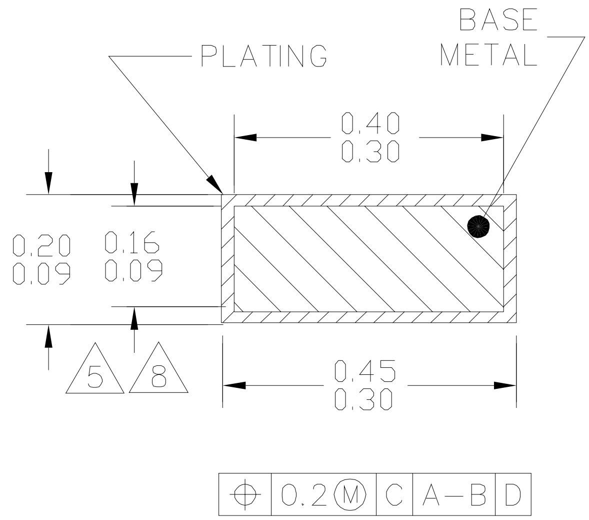


Figure 16-4. BDM Target-to-Host Serial Bit Timing (Logic 0)



DETAIL G



SECTION F–F

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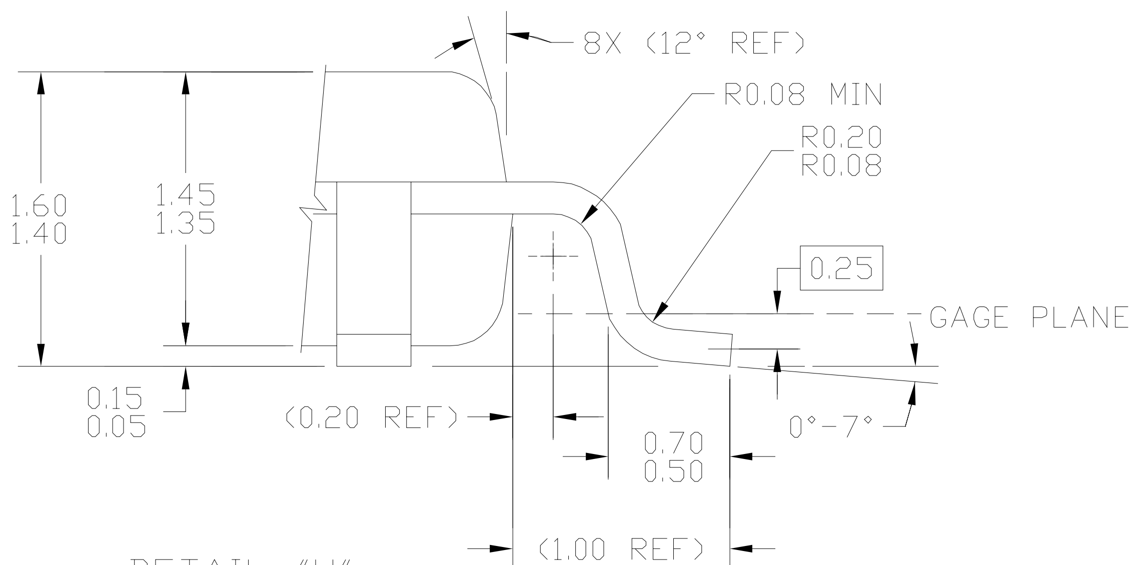

DETAIL "H"

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