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#### Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I <sup>2</sup> C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mc9s08dn16amlf">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mc9s08dn16amlf</a>

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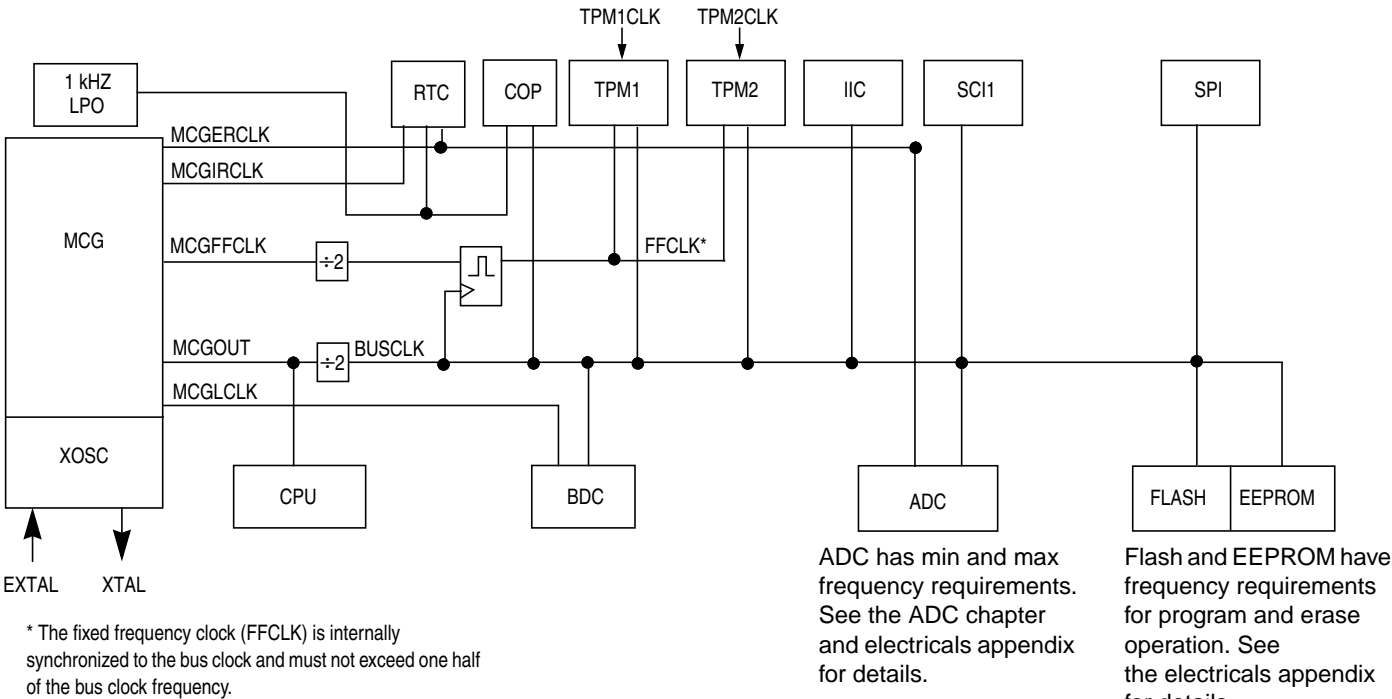


Figure 1-2. MC9S08DN60 System Clock Distribution Diagram

# Chapter 2

## Pins and Connections

This section describes signals that connect to package pins. It includes pinout diagrams, recommended system connections, and detailed discussions of signals.

### 2.1 Device Pin Assignment

This section shows the pin assignments for MC9S08DN60 Series MCUs in the available packages.

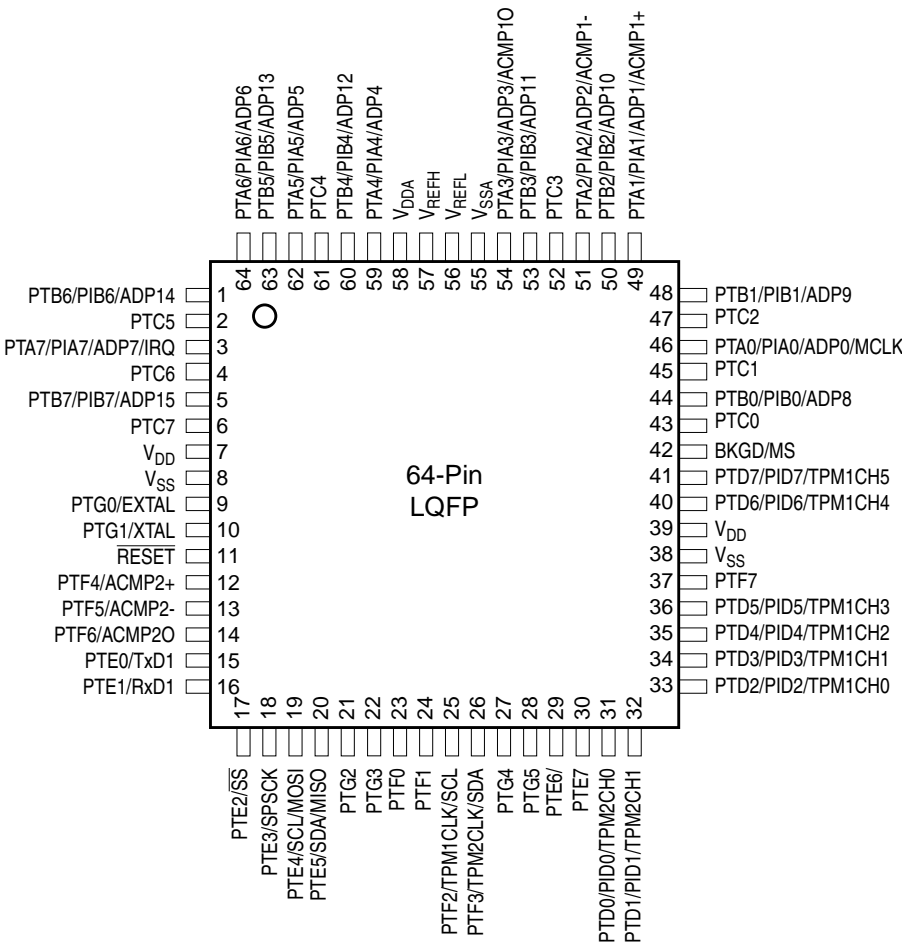


Figure 2-1. 64-Pin LQFP

## 5.8.1 Interrupt Pin Request Status and Control Register (IRQSC)

This direct page register includes status and control bits which are used to configure the IRQ function, report status, and acknowledge IRQ events.

	7	6	5	4	3	2	1	0
R	0	IRQPDD	IRQEDG	IRQPE	IRQF	0	IRQIE	IRQMOD
W						IRQACK		
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

**Figure 5-2. Interrupt Request Status and Control Register (IRQSC)**

**Table 5-2. IRQSC Register Field Descriptions**

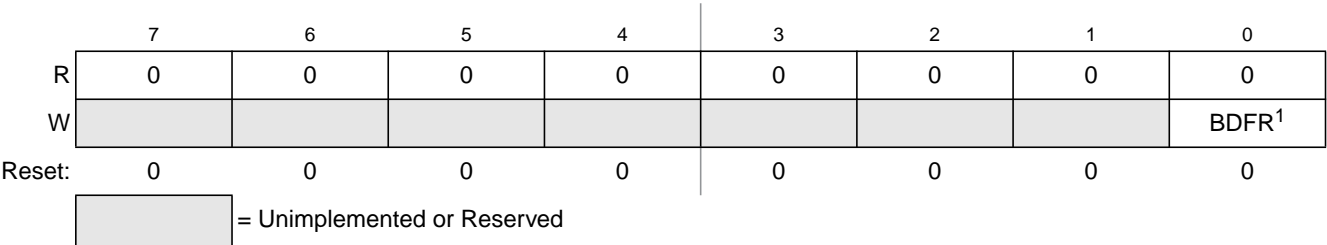
Field	Description
6 IRQPDD	<b>Interrupt Request (IRQ) Pull Device Disable</b> — This read/write control bit is used to disable the internal pull-up/pull-down device when the IRQ pin is enabled (IRQPE = 1) allowing for an external device to be used. 0 IRQ pull device enabled if IRQPE = 1. 1 IRQ pull device disabled if IRQPE = 1.
5 IRQEDG	<b>Interrupt Request (IRQ) Edge Select</b> — This read/write control bit is used to select the polarity of edges or levels on the IRQ pin that cause IRQF to be set. The IRQMOD control bit determines whether the IRQ pin is sensitive to both edges and levels or only edges. When the IRQ pin is enabled as the IRQ input and is configured to detect rising edges, it has a pull-down. When the IRQ pin is enabled as the IRQ input and is configured to detect falling edges, it has a pull-up. 0 IRQ is falling edge or falling edge/low-level sensitive. 1 IRQ is rising edge or rising edge/high-level sensitive.
4 IRQPE	<b>IRQ Pin Enable</b> — This read/write control bit enables the IRQ pin function. When this bit is set the IRQ pin can be used as an interrupt request. 0 IRQ pin function is disabled. 1 IRQ pin function is enabled.
3 IRQF	<b>IRQ Flag</b> — This read-only status bit indicates when an interrupt request event has occurred. 0 No IRQ request. 1 IRQ event detected.
2 IRQACK	<b>IRQ Acknowledge</b> — This write-only bit is used to acknowledge interrupt request events (write 1 to clear IRQF). Writing 0 has no meaning or effect. Reads always return 0. If edge-and-level detection is selected (IRQMOD = 1), IRQF cannot be cleared while the IRQ pin remains at its asserted level.
1 IRQIE	<b>IRQ Interrupt Enable</b> — This read/write control bit determines whether IRQ events generate an interrupt request. 0 Interrupt request when IRQF set is disabled (use polling). 1 Interrupt requested whenever IRQF = 1.
0 IRQMOD	<b>IRQ Detection Mode</b> — This read/write control bit selects either edge-only detection or edge-and-level detection. The IRQEDG control bit determines the polarity of edges and levels that are detected as interrupt request events. See <a href="#">Section 5.5.2.2, “Edge and Level Sensitivity”</a> for more details. 0 IRQ event on falling edges or rising edges only. 1 IRQ event on falling edges and low levels or on rising edges and high levels.

Table 5-3. SRS Register Field Descriptions

Field	Description
2 LOC	<b>Loss of Clock</b> — Reset was caused by a loss of external clock. 0 Reset not caused by loss of external clock 1 Reset caused by loss of external clock
1 LVD	<b>Low-Voltage Detect</b> — If the LVDRE bit is set and the supply drops below the LVD trip voltage, an LVD reset will occur. This bit is also set by POR. 0 Reset not caused by LVD trip or POR. 1 Reset caused by LVD trip or POR.

### 5.8.3 System Background Debug Force Reset Register (SBD FR)

This high page register contains a single write-only control bit. A serial background command such as WRITE\_BYTE must be used to write to SBD FR. Attempts to write this register from a user program are ignored. Reads always return 0x00.



<sup>1</sup> BDFR is writable only through serial background debug commands, not from user programs.

Figure 5-4. System Background Debug Force Reset Register (SBD FR)

Table 5-4. SBD FR Register Field Descriptions

Field	Description
0 BDFR	<b>Background Debug Force Reset</b> — A serial background command such as WRITE_BYTE can be used to allow an external debug host to force a target system reset. Writing 1 to this bit forces an MCU reset. This bit cannot be written from a user program.

### 6.5.2.7 Port B Interrupt Pin Select Register (PTBPS)

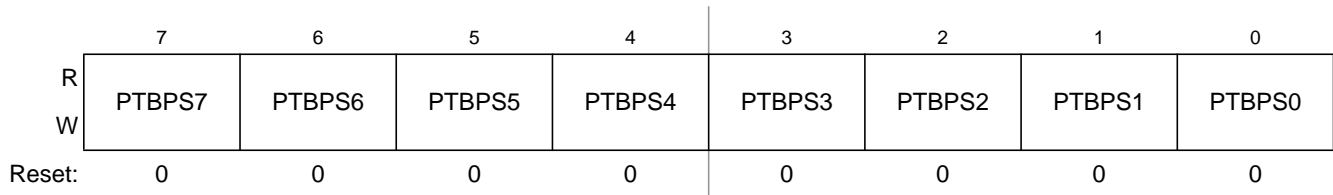


Figure 6-17. Port B Interrupt Pin Select Register (PTBPS)

Table 6-15. PTBPS Register Field Descriptions

Field	Description
7:0 PTBPS[7:0]	<b>Port B Interrupt Pin Selects</b> — Each of the PTBPSn bits enable the corresponding port B interrupt pin. 0 Pin not enabled as interrupt. 1 Pin enabled as interrupt.

### 6.5.2.8 Port B Interrupt Edge Select Register (PTBES)

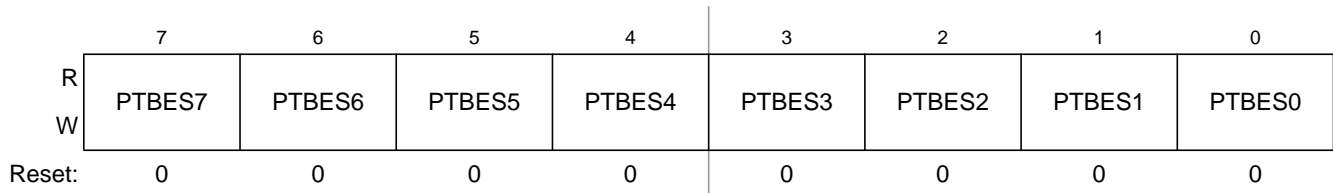


Figure 6-18. Port B Edge Select Register (PTBES)

Table 6-16. PTBES Register Field Descriptions

Field	Description
7:0 PTBES[7:0]	<b>Port B Edge Selects</b> — Each of the PTBESn bits serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled. 0 A pull-up device is connected to the associated pin and detects falling edge/low level for interrupt generation. 1 A pull-down device is connected to the associated pin and detects rising edge/high level for interrupt generation.



### 8.5.2.3 Example #3: Moving from BLPI to FEE Mode: External Crystal = 4 MHz, Bus Frequency = 16 MHz

In this example, the MCG will move through the proper operational modes from BLPI mode at a 16 kHz bus frequency running off of the internal reference clock (see previous example) to FEE mode using a 4 MHz crystal configured for a 16 MHz bus frequency. First, the code sequence will be described. Then a flowchart will be included which illustrates the sequence.

1. First, BLPI must transition to FBI mode.
  - a) MCGC2 = 0x00 (%00000000)
    - LP (bit 3) in MCGSC is 0
  - b) Optionally, loop until LOCK (bit 6) in the MCGSC is set, indicating that the FLL has acquired lock. Although the FLL is bypassed in FBI mode, it is still enabled and running.
2. Next, FBI will transition to FEE mode.
  - a) MCGC2 = 0x36 (%00110110)
    - RANGE (bit 5) set to 1 because the frequency of 4 MHz is within the high frequency range
    - HGO (bit 4) set to 1 to configure external oscillator for high gain operation
    - EREFS (bit 2) set to 1, because a crystal is being used
    - ERCLKEN (bit 1) set to 1 to ensure the external reference clock is active
  - b) Loop until OSCINIT (bit 1) in MCGSC is 1, indicating the crystal selected by the EREFS bit has been initialized.
  - c) MCGC1 = 0x38 (%00111000)
    - CLKS (bits 7 and 6) set to %00 in order to select the output of the FLL as system clock source
    - RDIV (bits 5-3) set to %111, or divide-by-128 because  $4 \text{ MHz} / 128 = 31.25 \text{ kHz}$  which is in the 31.25 kHz to 39.0625 kHz range required by the FLL
    - IREFS (bit 1) cleared to 0, selecting the external reference clock
  - d) Loop until IREFST (bit 4) in MCGSC is 0, indicating the external reference clock is the current source for the reference clock
  - e) Optionally, loop until LOCK (bit 6) in the MCGSC is set, indicating that the FLL has reacquired lock.
  - f) Loop until CLKST (bits 3 and 2) in MCGSC are %00, indicating that the output of the FLL is selected to feed MCGOUT

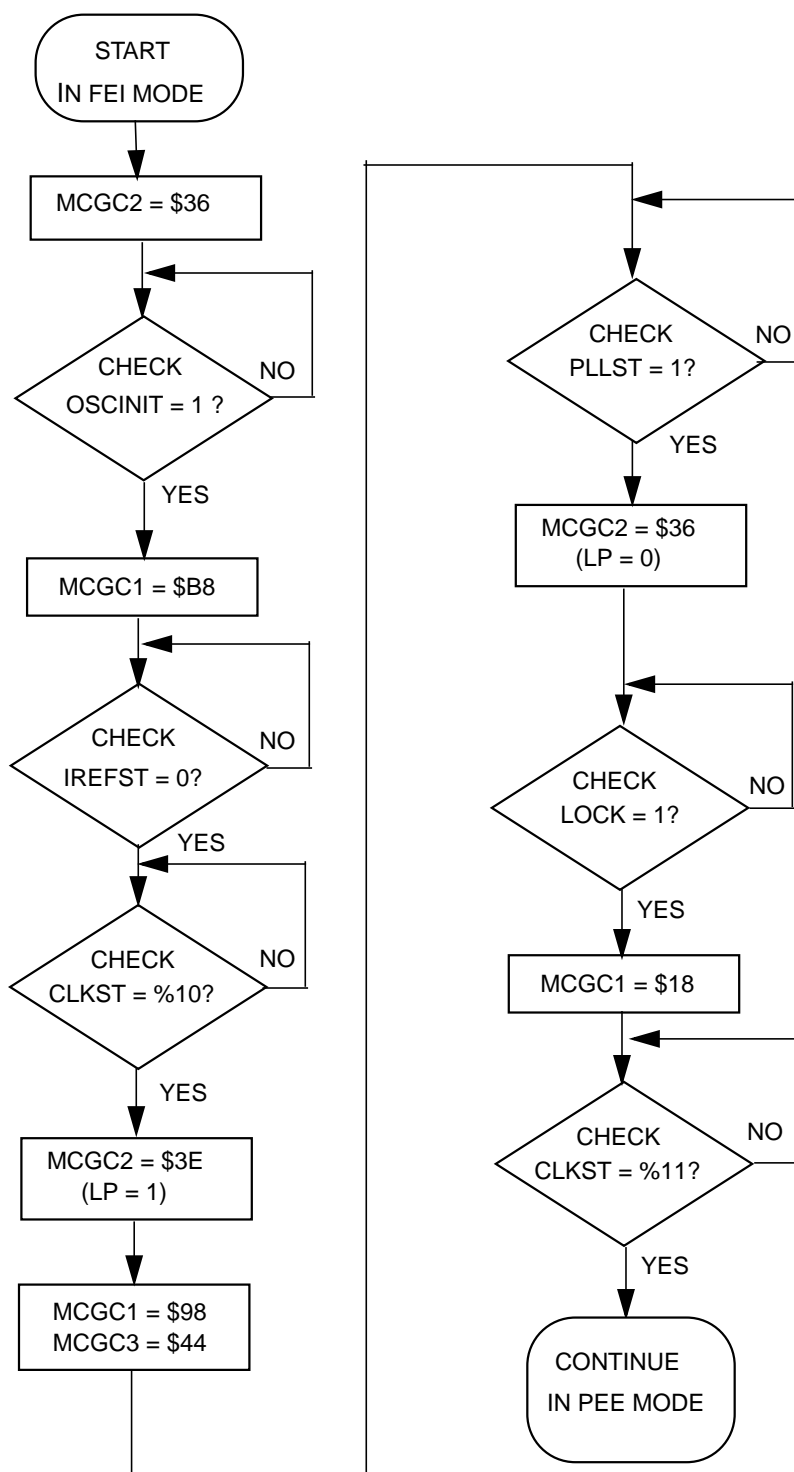


Figure 8-12. Flowchart of FEI to PEE Mode Transition using a 8 MHz crystal

## Chapter 10

# Analog-to-Digital Converter (S08ADC12V1)

### 10.1 Introduction

The 12-bit analog-to-digital converter (ADC) is a successive approximation ADC designed for operation within an integrated microcontroller system-on-chip.

#### NOTE

MC9S08DN60 Series devices operate at a higher voltage range (2.7 V to 5.5 V) and do not include stop1 mode. Please ignore references to stop1.

#### 10.1.1 Analog Power and Ground Signal Names

References to  $V_{DDAD}$  and  $V_{SSAD}$  in this chapter correspond to signals  $V_{DDA}$  and  $V_{SSA}$ , respectively.

#### 10.1.2 Channel Assignments

#### NOTE

The ADC channel assignments for the MC9S08DN60 Series devices are shown in [Table 10-1](#). Reserved channels convert to an unknown value.

This chapter shows bits for all S08ADC12V1 channels. MC9S08DN60 Series MCUs do not use all of these channels. All bits corresponding to channels that are not available on a device are reserved.

## 10.1.6 Features

Features of the ADC module include:

- Linear successive approximation algorithm with 12-bit resolution
- Up to 28 analog inputs
- Output formatted in 12-, 10-, or 8-bit right-justified unsigned format
- Single or continuous conversion (automatic return to idle after single conversion)
- Configurable sample time and conversion speed/power
- Conversion complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in wait or stop3 modes for lower noise operation
- Asynchronous clock source for lower noise operation
- Selectable asynchronous hardware conversion trigger
- Automatic compare with interrupt for less-than, or greater-than or equal-to, programmable value
- Temperature sensor

## 10.1.7 ADC Module Block Diagram

Figure 10-2 provides a block diagram of the ADC module.

### ADCSC1 = 0x41 (%01000001)

Bit 7	COCO	0	Read-only flag which is set when a conversion completes
Bit 6	AIEN	1	Conversion complete interrupt enabled
Bit 5	ADCO	0	One conversion only (continuous conversions disabled)
Bit 4:0	ADCH	00001	Input channel 1 selected as ADC input channel

### ADCRH/L = 0xxx

Holds results of conversion. Read high byte (ADCRH) before low byte (ADCRL) so that conversion data cannot be overwritten with data from the next conversion.

### ADCCVH/L = 0xxx

Holds compare value when compare function enabled

### APCTL1=0x02

AD1 pin I/O control disabled. All other AD pins remain general purpose I/O pins

### APCTL2=0x00

All other AD pins remain general purpose I/O pins

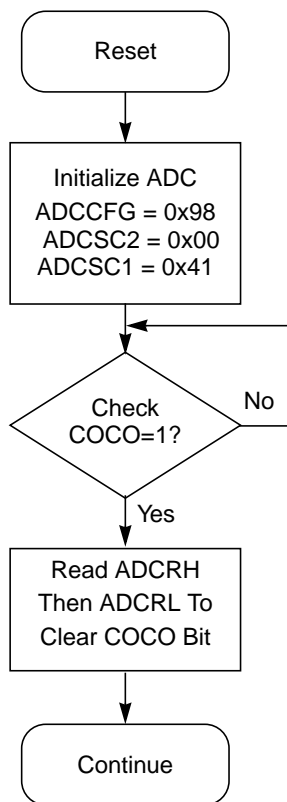


Figure 10-13. Initialization Flowchart for Example

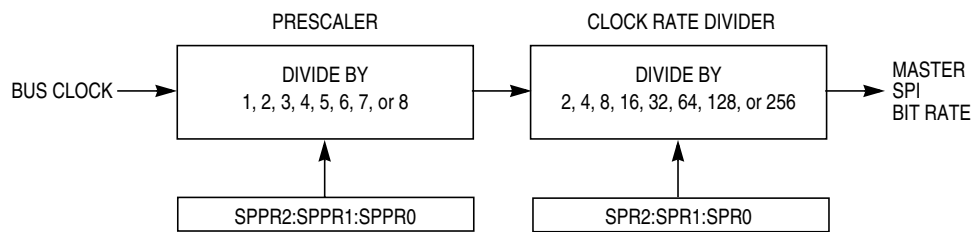


Figure 12-4. SPI Baud Rate Generation

## 12.2 External Signal Description

The SPI optionally shares four port pins. The function of these pins depends on the settings of SPI control bits. When the SPI is disabled ( $SPE = 0$ ), these four pins revert to being general-purpose port I/O pins that are not controlled by the SPI.

### 12.2.1 SPCK — SPI Serial Clock

When the SPI is enabled as a slave, this pin is the serial clock input. When the SPI is enabled as a master, this pin is the serial clock output.

### 12.2.2 MOSI — Master Data Out, Slave Data In

When the SPI is enabled as a master and SPI pin control zero ( $SPC0$ ) is 0 (not bidirectional mode), this pin is the serial data output. When the SPI is enabled as a slave and  $SPC0 = 0$ , this pin is the serial data input. If  $SPC0 = 1$  to select single-wire bidirectional mode, and master mode is selected, this pin becomes the bidirectional data I/O pin (MOMI). Also, the bidirectional mode output enable bit determines whether the pin acts as an input ( $BIDIROE = 0$ ) or an output ( $BIDIROE = 1$ ). If  $SPC0 = 1$  and slave mode is selected, this pin is not used by the SPI and reverts to being a general-purpose port I/O pin.

### 12.2.3 MISO — Master Data In, Slave Data Out

When the SPI is enabled as a master and SPI pin control zero ( $SPC0$ ) is 0 (not bidirectional mode), this pin is the serial data input. When the SPI is enabled as a slave and  $SPC0 = 0$ , this pin is the serial data output. If  $SPC0 = 1$  to select single-wire bidirectional mode, and slave mode is selected, this pin becomes the bidirectional data I/O pin (SISO) and the bidirectional mode output enable bit determines whether the pin acts as an input ( $BIDIROE = 0$ ) or an output ( $BIDIROE = 1$ ). If  $SPC0 = 1$  and master mode is selected, this pin is not used by the SPI and reverts to being a general-purpose port I/O pin.

### 12.2.4 $\overline{SS}$ — Slave Select

When the SPI is enabled as a slave, this pin is the low-true slave select input. When the SPI is enabled as a master and mode fault enable is off ( $MODFEN = 0$ ), this pin is not used by the SPI and reverts to being a general-purpose port I/O pin. When the SPI is enabled as a master and  $MODFEN = 1$ , the slave select output enable bit determines whether this pin acts as the mode fault input ( $SSOE = 0$ ) or as the slave select output ( $SSOE = 1$ ).

Table 13-5. SCI1S1 Field Descriptions (continued)

Field	Description
1 FE	<b>Framing Error Flag</b> — FE is set at the same time as RDRF when the receiver detects a logic 0 where the stop bit was expected. This suggests the receiver was not properly aligned to a character frame. To clear FE, read SCI1S1 with FE = 1 and then read the SCI data register (SCI1D). 0 No framing error detected. This does not guarantee the framing is correct. 1 Framing error.
0 PF	<b>Parity Error Flag</b> — PF is set at the same time as RDRF when parity is enabled (PE = 1) and the parity bit in the received character does not agree with the expected parity value. To clear PF, read SCI1S1 and then read the SCI data register (SCI1D). 0 No parity error. 1 Parity error.

### 13.2.5 SCI Status Register 2 (SCI1S2)

This register has one read-only status flag.

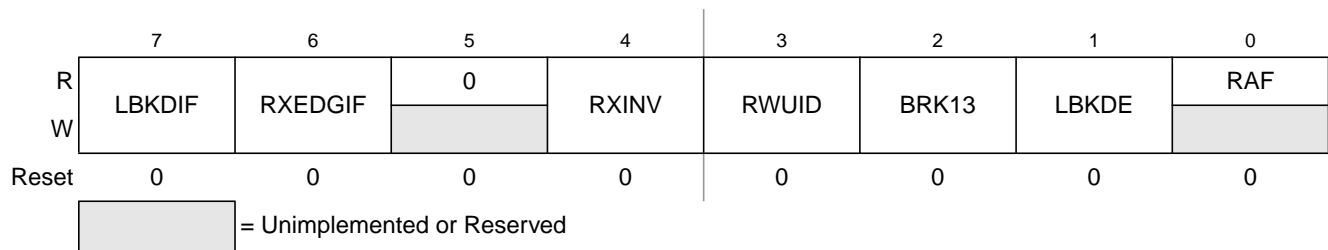


Figure 13-9. SCI Status Register 2 (SCI1S2)

Table 13-6. SCI1S2 Field Descriptions

Field	Description
7 LBKDIF	<b>LIN Break Detect Interrupt Flag</b> — LBKDIF is set when the LIN break detect circuitry is enabled and a LIN break character is detected. LBKDIF is cleared by writing a “1” to it. 0 No LIN break character has been detected. 1 LIN break character has been detected.
6 RXEDGIF	<b>RxD Pin Active Edge Interrupt Flag</b> — RXEDGIF is set when an active edge (falling if RXINV = 0, rising if RXINV=1) on the RxD pin occurs. RXEDGIF is cleared by writing a “1” to it. 0 No active edge on the receive pin has occurred. 1 An active edge on the receive pin has occurred.
4 RXINV <sup>1</sup>	<b>Receive Data Inversion</b> — Setting this bit reverses the polarity of the received data input. 0 Receive data not inverted 1 Receive data inverted
3 RWUID	<b>Receive Wake Up Idle Detect</b> — RWUID controls whether the idle character that wakes up the receiver sets the IDLE bit. 0 During receive standby state (RWU = 1), the IDLE bit does not get set upon detection of an idle character. 1 During receive standby state (RWU = 1), the IDLE bit gets set upon detection of an idle character.
2 BRK13	<b>Break Character Generation Length</b> — BRK13 is used to select a longer transmitted break character length. Detection of a framing error is not affected by the state of this bit. 0 Break character is transmitted with length of 10 bit times (11 if M = 1) 1 Break character is transmitted with length of 13 bit times (14 if M = 1)

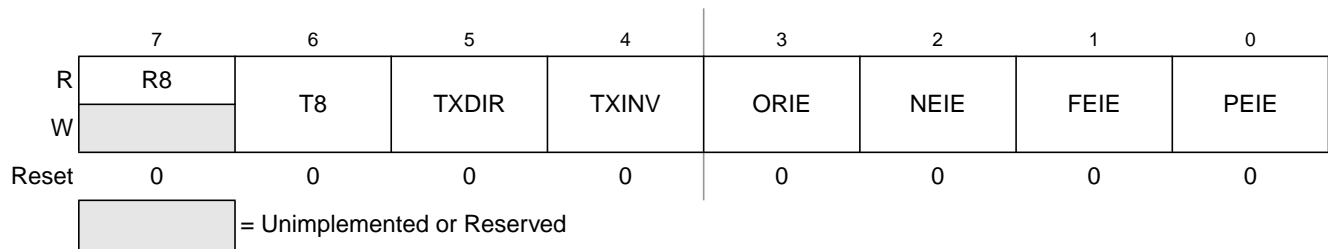
**Table 13-6. SCI1S2 Field Descriptions (continued)**

Field	Description
1 LBKDE	<b>LIN Break Detection Enable</b> — LBKDE is used to select a longer break character detection length. While LBKDE is set, framing error (FE) and receive data register full (RDRF) flags are prevented from setting. 0 Break character is detected at length of 10 bit times (11 if M = 1). 1 Break character is detected at length of 11 bit times (12 if M = 1).
0 RAF	<b>Receiver Active Flag</b> — RAF is set when the SCI receiver detects the beginning of a valid start bit, and RAF is cleared automatically when the receiver detects an idle line. This status flag can be used to check whether an SCI character is being received before instructing the MCU to go to stop mode. 0 SCI receiver idle waiting for a start bit. 1 SCI receiver active (RxD input not idle).

<sup>1</sup> Setting RXINV inverts the RxD input for all cases: data bits, start and stop bits, break, and idle.

When using an internal oscillator in a LIN system, it is necessary to raise the break detection threshold by one bit time. Under the worst case timing conditions allowed in LIN, it is possible that a 0x00 data character can appear to be 10.26 bit times long at a slave which is running 14% faster than the master. This would trigger normal break detection circuitry which is designed to detect a 10 bit break symbol. When the LBKDE bit is set, framing errors are inhibited and the break detection threshold changes from 10 bits to 11 bits, preventing false detection of a 0x00 data character as a LIN break symbol.

### 13.2.6 SCI Control Register 3 (SCI1C3)



**Figure 13-10. SCI Control Register 3 (SCI1C3)**

**Table 13-7. SCI1C3 Field Descriptions**

Field	Description
7 R8	<b>Ninth Data Bit for Receiver</b> — When the SCI is configured for 9-bit data (M = 1), R8 can be thought of as a ninth receive data bit to the left of the MSB of the buffered data in the SCI1D register. When reading 9-bit data, read R8 before reading SCI1D because reading SCI1D completes automatic flag clearing sequences which could allow R8 and SCI1D to be overwritten with new data.
6 T8	<b>Ninth Data Bit for Transmitter</b> — When the SCI is configured for 9-bit data (M = 1), T8 may be thought of as a ninth transmit data bit to the left of the MSB of the data in the SCI1D register. When writing 9-bit data, the entire 9-bit value is transferred to the SCI shift register after SCI1D is written so T8 should be written (if it needs to change from its previous value) before SCI1D is written. If T8 does not need to change in the new value (such as when it is used to generate mark or space parity), it need not be written each time SCI1D is written.
5 TXDIR	<b>TxD Pin Direction in Single-Wire Mode</b> — When the SCI is configured for single-wire half-duplex operation (LOOPS = RSRC = 1), this bit determines the direction of data at the TxD pin. 0 TxD pin is an input in single-wire mode. 1 TxD pin is an output in single-wire mode.





Figure 16-4 shows the host receiving a logic 0 from the target HCS08 MCU. Because the host is asynchronous to the target MCU, there is a 0-to-1 cycle delay from the host-generated falling edge on BKGD to the start of the bit time as perceived by the target MCU. The host initiates the bit time but the target HCS08 finishes it. Because the target wants the host to receive a logic 0, it drives the BKGD pin low for 13 BDC clock cycles, then briefly drives it high to speed up the rising edge. The host samples the bit level about 10 cycles after starting the bit time.

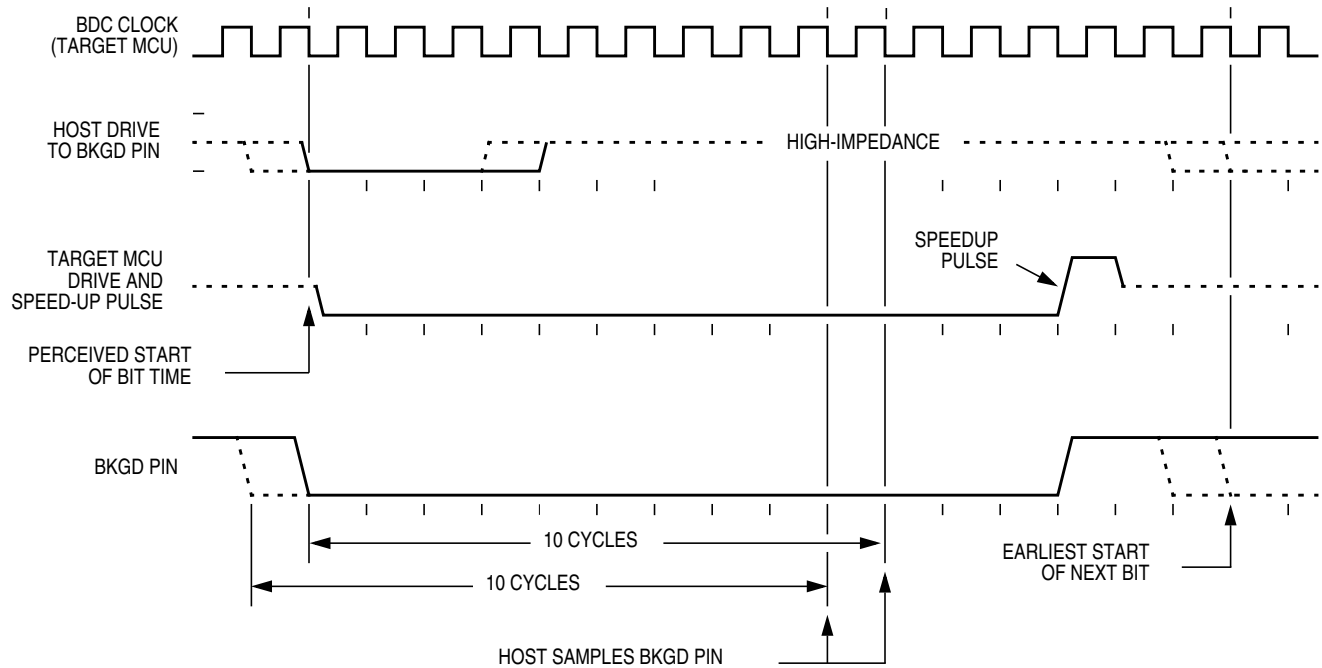


Figure 16-4. BDM Target-to-Host Serial Bit Timing (Logic 0)

where  $K$  is a constant pertaining to the particular part.  $K$  can be determined from equation 3 by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of  $K$ , the values of  $P_D$  and  $T_J$  can be obtained by solving equations 1 and 2 iteratively for any value of  $T_A$ .

## A.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM) and the Charge Device Model (CDM).

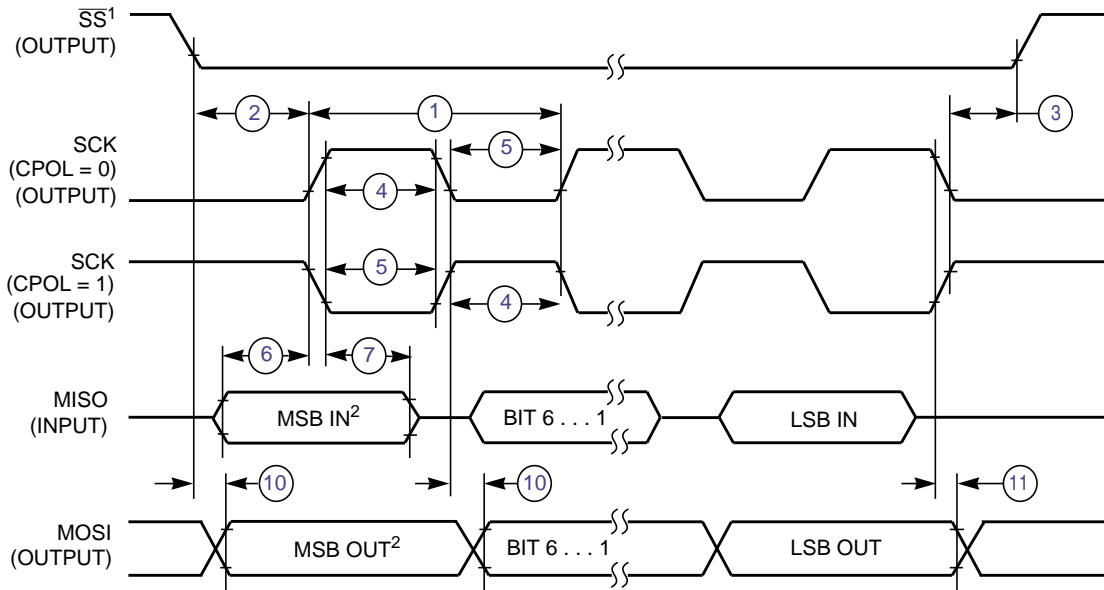
A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table A-4. ESD and Latch-up Test Conditions**

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	$\Omega$
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	–	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

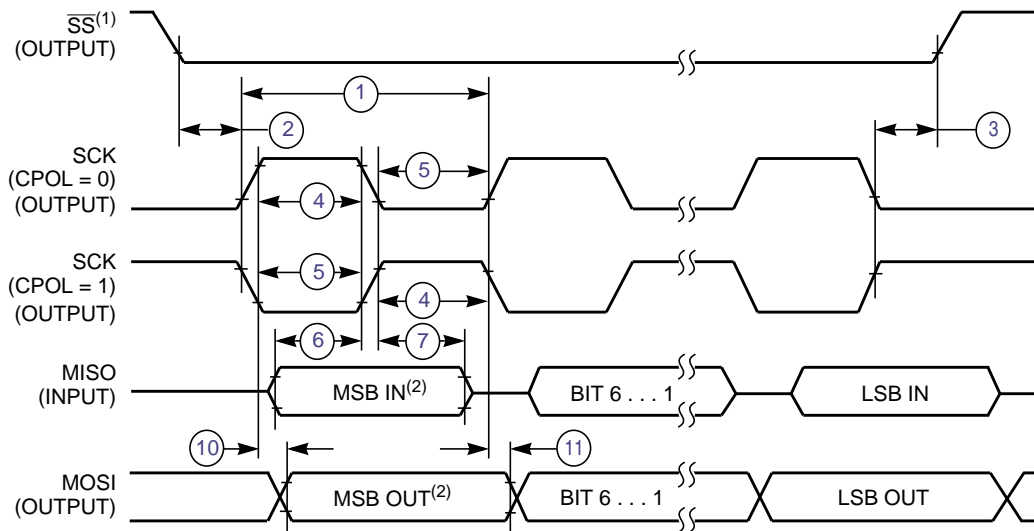
**Table A-5. ESD and Latch-Up Protection Characteristics**

Num	Rating	Symbol	Min	Max	Unit
1	Human Body Model (HBM)	$V_{HBM}$	+/- 2000	–	V
2	Charge Device Model (CDM)	$V_{CDM}$	+/- 500	–	V
3	Latch-up Current at $T_A = 125^\circ\text{C}$	$I_{LAT}$	+/- 100	–	mA



## NOTES:

1.  $\overline{SS}$  output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure A-7. SPI Master Timing (CPHA = 0)**


## NOTES:

1.  $\overline{SS}$  output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure A-8. SPI Master Timing (CPHA = 1)**

## A.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

### A.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

**Table A-17. Radiated Emissions for 3M05C Mask Set**

Parameter	Symbol	Conditions	Frequency	$f_{osc}/f_{CPU}$	Level <sup>1</sup> (Max)	Unit
Radiated emissions, electric field — Conditions -	$V_{RE\_TEM}$	$V_{DD} = 5$ $T_A = +25^{\circ}C$ 64 LQFP	0.15 – 50 MHz	16 MHz Crystal 20 MHz Bus	18	dB $\mu$ V
			50 – 150 MHz		18	
			150 – 500 MHz		13	
			500 – 1000 MHz		7	
			IEC Level		L	—
			SAE Level		2	—

<sup>1</sup> Data based on qualification test results.