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Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08dn32mlf

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1	6/2006	Advance Information version for alpha samples customers
2	9/2007	Product Launch. Removed the 64-pin QFN package. Changed from standard to extended mode for MSCAN registers in register summary. Corrected Block diagrams for SCI. Updated the latest Temp Sensor information. Made FTSTMOD reserved. Updated device to use the ADC 12-bit module. Revised the MCG module. Updated the TPM block module to version 3. Added the TPM block module version 2 as an appendix for devices using 3M05C (or earlier) mask sets. Heavily revised the Electricals appendix.
3	6/2008	Sustaining Update. Incorporated PS Issues # 2765, 3177, 3236, 3292, 3311, 3312, 3326, 3335, 3345, 3382, 2795, 3382 and 3386 PLL Jitter Spec update. Also, added internal reference clock trim adjustment statement to Features page. Updated the TPM module to the latest version. Adjusted values in Table A-13 Control Timing row 2 and in Table A-6 DC Characteristics row 24 so that it references 5.0 V instead of 3.0 V.

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2.2.1 Power

V_{DD} and V_{SS} are the primary power supply pins for the MCU. This voltage source supplies power to all I/O buffer circuitry and to an internal voltage regulator. The internal voltage regulator provides regulated lower-voltage source to the CPU and other internal circuitry of the MCU.

Typically, application systems have two separate capacitors across the power pins. In this case, there should be a bulk electrolytic capacitor, such as a 10- μ F tantalum capacitor, to provide bulk charge storage for the overall system and a 0.1- μ F ceramic bypass capacitor located as near to the MCU power pins as practical to suppress high-frequency noise. The MC9S08DN60 Series has two V_{DD} pins except on the 32-pin package. Each pin must have a bypass capacitor for best noise suppression.

V_{DDA} and V_{SSA} are the analog power supply pins for the MCU. This voltage source supplies power to the ADC module. A 0.1- μ F ceramic bypass capacitor should be located as near to the MCU power pins as practical to suppress high-frequency noise.

2.2.2 Oscillator

Immediately after reset, the MCU uses an internally generated clock provided by the multi-purpose clock generator (MCG) module. For more information on the MCG, see [Chapter 8, “Multi-Purpose Clock Generator \(S08MCGV1\).”](#)

The oscillator (XOSC) in this MCU is a Pierce oscillator that can accommodate a crystal or ceramic resonator. Rather than a crystal or ceramic resonator, an external oscillator can be connected to the EXTAL input pin.

Refer to [Figure 2-4](#) for the following discussion. R_S (when used) and R_F should be low-inductance resistors such as carbon composition resistors. Wire-wound resistors and some metal film resistors have too much inductance. C1 and C2 normally should be high-quality ceramic capacitors that are specifically designed for high-frequency applications.

R_F is used to provide a bias path to keep the EXTAL input in its linear range during crystal startup; its value is not generally critical. Typical systems use 1 M Ω to 10 M Ω . Higher values are sensitive to humidity, and lower values reduce gain and (in extreme cases) could prevent startup.

C1 and C2 are typically in the 5-pF to 25-pF range and are chosen to match the requirements of a specific crystal or resonator. Be sure to take into account printed circuit board (PCB) capacitance and MCU pin capacitance when selecting C1 and C2. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2 (which are usually the same size). As a first-order approximation, use 10 pF as an estimate of combined pin and PCB capacitance for each oscillator pin (EXTAL and XTAL).

2.2.3 $\overline{\text{RESET}}$

$\overline{\text{RESET}}$ is a dedicated pin with a pull-up device built in. It has input hysteresis, a high current output driver, and no output slew rate control. Internal power-on reset and low-voltage reset circuitry typically make external reset circuitry unnecessary. This pin is normally connected to the standard 6-pin background debug connector so a development system can directly reset the MCU system. If desired, a manual external reset can be added by supplying a simple switch to ground (pull reset pin low to force a reset).

Table 2-1. Pin Availability by Package Pin-Count

Pin Number			<-- Lowest Priority --> Highest				
64	48	32	Port Pin/Interrupt		Alt 1	Alt 2	
1	1	—	PTB6	PIB6	ADP14		
2	—	—	PTC5				
3	2	1	PTA7	PIA7	ADP7	IRQ	
4	—	—	PTC6				
5	3	—	PTB7	PIB7	ADP15		
6	—	—	PTC7				
7	4	2				V _{DD}	
8	5	3				V _{SS}	
9	6	4	PTG0		EXTAL		
10	7	5	PTG1		XTAL		
11	8	6				RESET	
12	9	—	PTF4			ACMP2+	
13	10	—	PTF5			ACMP2-	
14	—	—	PTF6			ACMP2O	
15	11	7	PTE0		TxD1		
16	12	8	PTE1 ²		RxD1 ²		
17	13	9	PTE2			SS	
18	14	10	PTE3			SPSCK	
19	15	11	PTE4		SCL ³	MOSI	
20	16	12	PTE5		SDA ³	MISO	
21	—	—	PTG2				
22	—	—	PTG3				
23	17	—	PTF0				
24	18	—	PTF1				
25	19	—	PTF2		TPM1CLK	SCL ³	
26	20	—	PTF3		TPM2CLK	SDA ³	
27	—	—	PTG4				
28	—	—	PTG5				
29	21	13	PTE6				
30	22	14	PTE7				
31	23	15	PTD0	PID0		TPM2CH0	
32	24	16	PTD1	PID1		TPM2CH1	

Pin Number			<-- Lowest Priority --> Highest				
64	48	32	Port Pin/Interrupt		Alt 1	Alt 2	
33	25	17	PTD2	PID2		TPM1CH0	
34	26	18	PTD3	PID3		TPM1CH1	
35	27	19	PTD4	PID4		TPM1CH2	
36	28	20	PTD5	PID5		TPM1CH3	
37	—	—	PTF7				
38	29	—				V _{SS}	
39	30	—				V _{DD}	
40	31	—	PTD6	PID6		TPM1CH4	
41	32	—	PTD7	PID7		TPM1CH5	
42	33	21			BKGD	MS	
43	—	—	PTC0				
44	34	22	PTB0	PIB0	ADP8		
45	—	—	PTC1				
46	35	23	PTA0	PIA0	ADP0	MCLK	
47	—	—	PTC2				
48	36	24	PTB1	PIB1	ADP9		
49	37	25	PTA1	PIA1	ADP1 ¹	ACMP1+ ¹	
50	38	—	PTB2	PIB2	ADP10		
51	39	26	PTA2	PIA2	ADP2 ¹	ACMP1- ¹	
52	—	—	PTC3				
53	40	—	PTB3	PIB3	ADP11		
54	41	27	PTA3	PIA3	ADP3	ACMP1O	
55	42	28				V _{SSA}	
56	—	—				V _{REFL}	
57	43	29				V _{REFH}	
58	—	—				V _{DDA}	
59	44	30	PTA4	PIA4	ADP4		
60	45	—	PTB4	PIB4	ADP12		
61	—	—	PTC4				
62	46	31	PTA5	PIA5	ADP5		
63	47	—	PTB5	PIB5	ADP13		
64	48	32	PTA6	PIA6	ADP6		

1. If both of these analog modules are enabled, they both will have access to the pin.
2. Pin does not contain a clamp diode to V_{DD} and should not be driven above V_{DD}. The voltage measured on this pin when internal pull-up is enabled may be as low as V_{DD} - 0.7 V. The internal gates connected to this pin are pulled to V_{DD}.
3. The IIC module pins can be repositioned using IICPS bit in the SOPT1 register. The default reset locations are on PTF2 and PTF3.

NOTE

The FCBEF flag will not set after launching the sector erase abort command. If an attempt is made to start a new command write sequence with a sector erase abort operation active, the FACCERR flag in the FSTAT register will be set. A new command write sequence may be started after clearing the ACCERR flag, if set.

NOTE

The sector erase abort command should be used sparingly since a sector erase operation that is aborted counts as a complete program/erase cycle.

4.5.6 Access Errors

An access error occurs whenever the command execution protocol is violated.

Any of the following specific actions will cause the access error flag (FACCERR) in FSTAT to be set. FACCERR must be cleared by writing a 1 to FACCERR in FSTAT before any command can be processed.

- Writing to a Flash address before the internal Flash and EEPROM clock frequency has been set by writing to the FCDIV register.
- Writing to a Flash address while FCBEF is not set. (A new command cannot be started until the command buffer is empty.)
- Writing a second time to a Flash address before launching the previous command. (There is only one write to Flash for every command.)
- Writing a second time to FCMD before launching the previous command. (There is only one write to FCMD for every command.)
- Writing to any Flash control register other than FCMD after writing to a Flash address.
- Writing any command code other than the six allowed codes (0x05, 0x20, 0x25, 0x40, 0x41, or 0x47) to FCMD.
- Writing any Flash control register other than to write to FSTAT (to clear FCBEF and launch the command) after writing the command to FCMD.
- The MCU enters stop mode while a program or erase command is in progress. (The command is aborted.)
- Writing the byte program, burst program, sector erase or sector erase abort command code (0x20, 0x25, 0x40, or 0x47) with a background debug command while the MCU is secured. (The background debug controller can do blank check and mass erase commands only when the MCU is secure.)
- Writing 0 to FCBEF to cancel a partial command.

4.5.10 EEPROM Mapping

Only half of the EEPROM is in the memory map. The EPGSEL bit in FCNFG register selects which half of the array can be accessed in foreground while the other half can not be accessed in background. There are two mapping mode options that can be selected to configure the 8-byte EEPROM sectors: 4-byte mode and 8-byte mode. Each mode is selected by the EPGMOD bit in the FOPT register.

In 4-byte sector mode (EPGMOD = 0), each 8-byte sector splits four bytes on foreground and four bytes on background but on the same addresses. The EPGSEL bit selects which four bytes can be accessed. During a sector erase, the entire 8-byte sector (four bytes in foreground and four bytes in background) is erased.

In 8-byte sector mode (EPGMOD = 1), each entire 8-byte sector is in a single page. The EPGSEL bit selects which sectors are on background. During a sector erase, the entire 8-byte sector in foreground is erased.

4.5.11 Flash and EEPROM Registers and Control Bits

The Flash and EEPROM modules have seven 8-bit registers in the high-page register space and three locations in the nonvolatile register space in Flash memory. Two of those locations are copied into two corresponding high-page control registers at reset. There is also an 8-byte comparison key in Flash memory. Refer to [Table 4-3](#) and [Table 4-4](#) for the absolute address assignments for all Flash and EEPROM registers. This section refers to registers and control bits only by their names. A Freescale Semiconductor-provided equate or header file normally is used to translate these names into the appropriate absolute addresses.

4.5.11.1 Flash and EEPROM Clock Divider Register (FCDIV)

Bit 7 of this register is a read-only flag. Bits 6:0 may be read at any time but can be written only one time. Before any erase or programming operations are possible, write to this register to set the frequency of the clock for the nonvolatile memory system within acceptable limits.

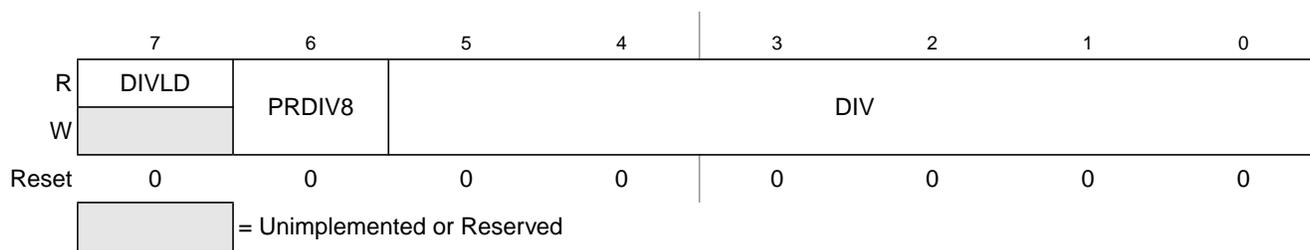


Figure 4-5. Flash and EEPROM Clock Divider Register (FCDIV)

Table 4-6. FCDIV Register Field Descriptions

Field	Description
7 DIVLD	Divisor Loaded Status Flag — When set, this read-only status flag indicates that the FCDIV register has been written since reset. Reset clears this bit and the first write to this register causes this bit to become set regardless of the data written. 0 FCDIV has not been written since reset; erase and program operations disabled for Flash and EEPROM. 1 FCDIV has been written since reset; erase and program operations enabled for Flash and EEPROM.
6 PRDIV8	Prescale (Divide) Flash and EEPROM Clock by 8 (This bit is write once.) 0 Clock input to the Flash and EEPROM clock divider is the bus rate clock. 1 Clock input to the Flash and EEPROM clock divider is the bus rate clock divided by 8.
5:0 DIV	Divisor for Flash and EEPROM Clock Divider — These bits are write once. The Flash and EEPROM clock divider divides the bus rate clock (or the bus rate clock divided by 8 if PRDIV8 = 1) by the value in the 6-bit DIV field plus one. The resulting frequency of the internal Flash and EEPROM clock must fall within the range of 200 kHz to 150 kHz for proper Flash and EEPROM operations. Program/Erase timing pulses are one cycle of this internal Flash and EEPROM clock which corresponds to a range of 5 μs to 6.7 μs. The automated programming logic uses an integer number of these pulses to complete an erase or program operation. See Equation 4-1 and Equation 4-2 .

$$\text{if PRDIV8} = 0 \text{ — } f_{\text{FCLK}} = f_{\text{Bus}} \div (\text{DIV} + 1) \quad \text{Eqn. 4-1}$$

$$\text{if PRDIV8} = 1 \text{ — } f_{\text{FCLK}} = f_{\text{Bus}} \div (8 \times (\text{DIV} + 1)) \quad \text{Eqn. 4-2}$$

Table 4-7 shows the appropriate values for PRDIV8 and DIV for selected bus frequencies.

Table 4-7. Flash and EEPROM Clock Divider Settings

f_{Bus}	PRDIV8 (Binary)	DIV (Decimal)	f_{FCLK}	Program/Erase Timing Pulse (5 μs Min, 6.7 μs Max)
20 MHz	1	12	192.3 kHz	5.2 μs
10 MHz	0	49	200 kHz	5 μs
8 MHz	0	39	200 kHz	5 μs
4 MHz	0	19	200 kHz	5 μs
2 MHz	0	9	200 kHz	5 μs
1 MHz	0	4	200 kHz	5 μs
200 kHz	0	0	200 kHz	5 μs
150 kHz	0	0	150 kHz	6.7 μs

4.5.11.2 Flash and EEPROM Options Register (FOPT and NVOPT)

During reset, the contents of the nonvolatile location NVOPT are copied from Flash into FOPT. To change the value in this register, erase and reprogram the NVOPT location in Flash memory as usual and then issue a new MCU reset.

5.8 Reset, Interrupt, and System Control Registers and Control Bits

One 8-bit register in the direct page register space and eight 8-bit registers in the high-page register space are related to reset and interrupt systems.

Refer to [Table 4-2](#) and [Table 4-3](#) in [Chapter 4, “Memory,”](#) of this data sheet for the absolute address assignments for all registers. This section refers to registers and control bits only by their names. A Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

Some control bits in the SOPT1 and SPMSC2 registers are related to modes of operation. Although brief descriptions of these bits are provided here, the related functions are discussed in greater detail in [Chapter 3, “Modes of Operation.”](#)

5.8.2 System Reset Status Register (SRS)

This high page register includes read-only status flags to indicate the source of the most recent reset. When a debug host forces reset by writing 1 to BDFR in the SBDFR register, none of the status bits in SRS will be set. Writing any value to this register address causes a COP reset when the COP is enabled except the values 0x55 and 0xAA. Writing a 0x55-0xAA sequence to this address clears the COP watchdog timer without affecting the contents of this register. The reset state of these bits depends on what caused the MCU to reset.

	7	6	5	4	3	2	1	0
R	POR	PIN	COP	ILOP	ILAD	LOC	LVD	0
W	Writing 0x55, 0xAA to SRS address clears COP watchdog timer.							
POR:	1	0	0	0	0	0	1	0
LVD:	u	0	0	0	0	0	1	0
Any other reset:	0	Note ⁽¹⁾	Note ⁽¹⁾	Note ⁽¹⁾	Note ⁽¹⁾	0	0	0

¹ Any of these reset sources that are active at the time of reset entry will cause the corresponding bit(s) to be set; bits corresponding to sources that are not active at the time of reset entry will be cleared.

Figure 5-3. System Reset Status (SRS)

Table 5-3. SRS Register Field Descriptions

Field	Description
7 POR	Power-On Reset — Reset was caused by the power-on detection logic. Because the internal supply voltage was ramping up at the time, the low-voltage reset (LVD) status bit is also set to indicate that the reset occurred while the internal supply was below the LVD threshold. 0 Reset not caused by POR. 1 POR caused reset.
6 PIN	External Reset Pin — Reset was caused by an active-low level on the external reset pin. 0 Reset not caused by external reset pin. 1 Reset came from external reset pin.
5 COP	Computer Operating Properly (COP) Watchdog — Reset was caused by the COP watchdog timer timing out. This reset source can be blocked by COPE = 0. 0 Reset not caused by COP timeout. 1 Reset caused by COP timeout.
4 ILOP	Illegal Opcode — Reset was caused by an attempt to execute an unimplemented or illegal opcode. The STOP instruction is considered illegal if stop is disabled by STOPE = 0 in the SOPT register. The BGND instruction is considered illegal if active background mode is disabled by ENBDM = 0 in the BDCSC register. 0 Reset not caused by an illegal opcode. 1 Reset caused by an illegal opcode.
3 ILAD	Illegal Address — Reset was caused by an attempt to access either data or an instruction at an unimplemented memory address. 0 Reset not caused by an illegal address. 1 Reset caused by an illegal address.

8.5.2.3 Example #3: Moving from BLPI to FEE Mode: External Crystal = 4 MHz, Bus Frequency = 16 MHz

In this example, the MCG will move through the proper operational modes from BLPI mode at a 16 kHz bus frequency running off of the internal reference clock (see previous example) to FEE mode using a 4 MHz crystal configured for a 16 MHz bus frequency. First, the code sequence will be described. Then a flowchart will be included which illustrates the sequence.

1. First, BLPI must transition to FBI mode.
 - a) MCGC2 = 0x00 (%00000000)
 - LP (bit 3) in MCGSC is 0
 - b) Optionally, loop until LOCK (bit 6) in the MCGSC is set, indicating that the FLL has acquired lock. Although the FLL is bypassed in FBI mode, it is still enabled and running.
2. Next, FBI will transition to FEE mode.
 - a) MCGC2 = 0x36 (%00110110)
 - RANGE (bit 5) set to 1 because the frequency of 4 MHz is within the high frequency range
 - HGO (bit 4) set to 1 to configure external oscillator for high gain operation
 - EREFS (bit 2) set to 1, because a crystal is being used
 - ERCLKEN (bit 1) set to 1 to ensure the external reference clock is active
 - b) Loop until OSCINIT (bit 1) in MCGSC is 1, indicating the crystal selected by the EREFS bit has been initialized.
 - c) MCGC1 = 0x38 (%00111000)
 - CLKS (bits 7 and 6) set to %00 in order to select the output of the FLL as system clock source
 - RDIV (bits 5-3) set to %111, or divide-by-128 because $4 \text{ MHz} / 128 = 31.25 \text{ kHz}$ which is in the 31.25 kHz to 39.0625 kHz range required by the FLL
 - IREFS (bit 1) cleared to 0, selecting the external reference clock
 - d) Loop until IREFST (bit 4) in MCGSC is 0, indicating the external reference clock is the current source for the reference clock
 - e) Optionally, loop until LOCK (bit 6) in the MCGSC is set, indicating that the FLL has reacquired lock.
 - f) Loop until CLKST (bits 3 and 2) in MCGSC are %00, indicating that the output of the FLL is selected to feed MCGOUT

external crystal and a maximum reference divider factor of 128, the resulting frequency of the reference clock for the FLL is 62.5 kHz (greater than the 39.0625 kHz maximum allowed).

Care must be taken in the software to minimize the amount of time spent in this state where the FLL is operating in this condition.

The following code sequence describes how to move from FEI mode to PEE mode until the 8 MHz crystal reference frequency is set to achieve a bus frequency of 8 MHz. Because the MCG is in FEI mode out of reset, this example also shows how to initialize the MCG for PEE mode out of reset. First, the code sequence will be described. Then a flowchart will be included which illustrates the sequence.

1. First, FEI must transition to FBE mode:
 - a) $MCGC2 = 0x36$ (%00110110)
 - BDIV (bits 7 and 6) set to %00, or divide-by-1
 - RANGE (bit 5) set to 1 because the frequency of 8 MHz is within the high frequency range
 - HGO (bit 4) set to 1 to configure external oscillator for high gain operation
 - EREFS (bit 2) set to 1, because a crystal is being used
 - ERCLKEN (bit 1) set to 1 to ensure the external reference clock is active
 - b) Loop until OSCINIT (bit 1) in MCGSC is 1, indicating the crystal selected by the EREFS bit has been initialized.
 - c) Block Interrupts (If applicable by setting the interrupt bit in the CCR).
 - d) $MCGC1 = 0xB8$ (%10111000)
 - CLKS (bits 7 and 6) set to %10 in order to select external reference clock as system clock source
 - RDIV (bits 5-3) set to %111, or divide-by-128.

NOTE

8 MHz / 128 = 62.5 kHz which is greater than the 31.25 kHz to 39.0625 kHz range required by the FLL. Therefore after the transition to FBE is complete, software must progress through to BLPE mode immediately by setting the LP bit in MCGC2.

- IREFS (bit 2) cleared to 0, selecting the external reference clock
 - e) Loop until IREFST (bit 4) in MCGSC is 0, indicating the external reference is the current source for the reference clock
 - f) Loop until CLKST (bits 3 and 2) in MCGSC are %10, indicating that the external reference clock is selected to feed MCGOUT
2. Then, FBE mode transitions into BLPE mode:
 - a) $MCGC2 = 0x3E$ (%00111110)
 - LP (bit 3) in MCGC2 to 1 (BLPE mode entered)

NOTE

There must be no extra steps (including interrupts) between steps 1d and 2a.

- b) Enable Interrupts (if applicable by clearing the interrupt bit in the CCR).

11.3.3 IIC Control Register (IICC1)

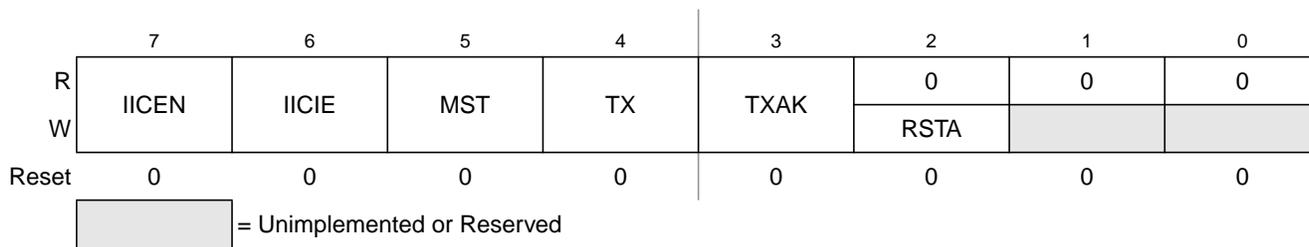


Figure 11-5. IIC Control Register (IICC1)

Table 11-5. IICC1 Field Descriptions

Field	Description
7 IICEN	IIC Enable. The IICEN bit determines whether the IIC module is enabled. 0 IIC is not enabled 1 IIC is enabled
6 IICIE	IIC Interrupt Enable. The IICIE bit determines whether an IIC interrupt is requested. 0 IIC interrupt request not enabled 1 IIC interrupt request enabled
5 MST	Master Mode Select. The MST bit changes from a 0 to a 1 when a start signal is generated on the bus and master mode is selected. When this bit changes from a 1 to a 0 a stop signal is generated and the mode of operation changes from master to slave. 0 Slave mode 1 Master mode
4 TX	Transmit Mode Select. The TX bit selects the direction of master and slave transfers. In master mode, this bit should be set according to the type of transfer required. Therefore, for address cycles, this bit is always high. When addressed as a slave, this bit should be set by software according to the SRW bit in the status register. 0 Receive 1 Transmit
3 TXAK	Transmit Acknowledge Enable. This bit specifies the value driven onto the SDA during data acknowledge cycles for master and slave receivers. 0 An acknowledge signal is sent out to the bus after receiving one data byte 1 No acknowledge signal response is sent
2 RSTA	Repeat start. Writing a 1 to this bit generates a repeated start condition provided it is the current master. This bit is always read as cleared. Attempting a repeat at the wrong time results in loss of arbitration.

Chapter 12

Serial Peripheral Interface (S08SPIV3)

12.1 Introduction

The serial peripheral interface (SPI) module provides for full-duplex, synchronous, serial communication between the MCU and peripheral devices. These peripheral devices can include other microcontrollers, analog-to-digital converters, shift registers, sensors, memories, etc.

The SPI runs at a baud rate up to the bus clock divided by two in master mode and bus clock divided by four in slave mode.

All devices in the MC9S08DN60 Series MCUs contain one SPI module, as shown in the following block diagram.

NOTE

Ensure that the SPI should not be disabled ($SPE=0$) at the same time as a bit change to the CPHA bit. These changes should be performed as separate operations or unexpected behavior may occur.

Instead of hardware interrupts, software polling may be used to monitor the TDRE and TC status flags if the corresponding TIE or TCIE local interrupt masks are 0s.

When a program detects that the receive data register is full ($RDRF = 1$), it gets the data from the receive data register by reading SCI1D. The RDRF flag is cleared by reading SCI1S1 while $RDRF = 1$ and then reading SCI1D.

When polling is used, this sequence is naturally satisfied in the normal course of the user program. If hardware interrupts are used, SCI1S1 must be read in the interrupt service routine (ISR). Normally, this is done in the ISR anyway to check for receive errors, so the sequence is automatically satisfied.

The IDLE status flag includes logic that prevents it from getting set repeatedly when the RxD line remains idle for an extended period of time. IDLE is cleared by reading SCI1S1 while $IDLE = 1$ and then reading SCI1D. After IDLE has been cleared, it cannot become set again until the receiver has received at least one new character and has set RDRF.

If the associated error was detected in the received character that caused RDRF to be set, the error flags — noise flag (NF), framing error (FE), and parity error flag (PF) — get set at the same time as RDRF. These flags are not set in overrun cases.

If RDRF was already set when a new character is ready to be transferred from the receive shifter to the receive data buffer, the overrun (OR) flag gets set instead the data along with any associated NF, FE, or PF condition is lost.

At any time, an active edge on the RxD serial data input pin causes the RXEDGIF flag to set. The RXEDGIF flag is cleared by writing a “1” to it. This function does depend on the receiver being enabled ($RE = 1$).

13.3.5 Additional SCI Functions

The following sections describe additional SCI functions.

13.3.5.1 8- and 9-Bit Data Modes

The SCI system (transmitter and receiver) can be configured to operate in 9-bit data mode by setting the M control bit in SCI1C1. In 9-bit mode, there is a ninth data bit to the left of the MSB of the SCI data register. For the transmit data buffer, this bit is stored in T8 in SCI1C3. For the receiver, the ninth bit is held in R8 in SCI1C3.

For coherent writes to the transmit data buffer, write to the T8 bit before writing to SCI1D.

If the bit value to be transmitted as the ninth bit of a new character is the same as for the previous character, it is not necessary to write to T8 again. When data is transferred from the transmit data buffer to the transmit shifter, the value in T8 is copied at the same time data is transferred from SCI1D to the shifter.

9-bit data mode typically is used in conjunction with parity to allow eight bits of data plus the parity in the ninth bit. Or it is used with address-mark wakeup so the ninth data bit can serve as the wakeup bit. In custom protocols, the ninth bit can also serve as a software-controlled marker.

- Non-intrusive commands can be executed at any time even while the user's program is running. Non-intrusive commands allow a user to read or write MCU memory locations or access status and control registers within the background debug controller.

Typically, a relatively simple interface pod is used to translate commands from a host computer into commands for the custom serial interface to the single-wire background debug system. Depending on the development tool vendor, this interface pod may use a standard RS-232 serial port, a parallel printer port, or some other type of communications such as a universal serial bus (USB) to communicate between the host PC and the pod. The pod typically connects to the target system with ground, the BKGD pin, $\overline{\text{RESET}}$, and sometimes V_{DD} . An open-drain connection to reset allows the host to force a target system reset, which is useful to regain control of a lost target system or to control startup of a target system before the on-chip nonvolatile memory has been programmed. Sometimes V_{DD} can be used to allow the pod to use power from the target system to avoid the need for a separate power supply. However, if the pod is powered separately, it can be connected to a running target system without forcing a target system reset or otherwise disturbing the running application program.

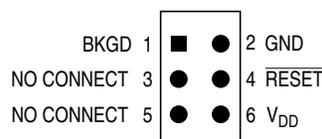


Figure 16-1. BDM Tool Connector

16.2.1 BKGD Pin Description

BKGD is the single-wire background debug interface pin. The primary function of this pin is for bidirectional serial communication of active background mode commands and data. During reset, this pin is used to select between starting in active background mode or starting the user's application program. This pin is also used to request a timed sync response pulse to allow a host development tool to determine the correct clock frequency for background debug serial communications.

BDC serial communications use a custom serial protocol first introduced on the M68HC12 Family of microcontrollers. This protocol assumes the host knows the communication clock rate that is determined by the target BDC clock rate. All communication is initiated and controlled by the host that drives a high-to-low edge to signal the beginning of each bit time. Commands and data are sent most significant bit first (MSB first). For a detailed description of the communications protocol, refer to [Section 16.2.2, "Communication Details."](#)

If a host is attempting to communicate with a target MCU that has an unknown BDC clock rate, a SYNC command may be sent to the target MCU to request a timed sync response signal from which the host can determine the correct communication speed.

BKGD is a pseudo-open-drain pin and there is an on-chip pullup so no external pullup resistor is required. Unlike typical open-drain pins, the external RC time constant on this pin, which is influenced by external capacitance, plays almost no role in signal rise time. The custom protocol provides for brief, actively driven speedup pulses to force rapid rise times on this pin without risking harmful drive level conflicts. Refer to [Section 16.2.2, "Communication Details,"](#) for more detail.

16.2.3 BDC Commands

BDC commands are sent serially from a host computer to the BKGD pin of the target HCS08 MCU. All commands and data are sent MSB-first using a custom BDC communications protocol. Active background mode commands require that the target MCU is currently in the active background mode while non-intrusive commands may be issued at any time whether the target MCU is in active background mode or running a user application program.

Table 16-1 shows all HCS08 BDC commands, a shorthand description of their coding structure, and the meaning of each command.

Coding Structure Nomenclature

This nomenclature is used in Table 16-1 to describe the coding structure of the BDC commands.

	Commands begin with an 8-bit hexadecimal command code in the host-to-target direction (most significant bit first)
/	= separates parts of the command
d	= delay 16 target BDC clock cycles
AAAA	= a 16-bit address in the host-to-target direction
RD	= 8 bits of read data in the target-to-host direction
WD	= 8 bits of write data in the host-to-target direction
RD16	= 16 bits of read data in the target-to-host direction
WD16	= 16 bits of write data in the host-to-target direction
SS	= the contents of BDCSCR in the target-to-host direction (STATUS)
CC	= 8 bits of write data for BDCSCR in the host-to-target direction (CONTROL)
RBKP	= 16 bits of read data in the target-to-host direction (from BDCBKPT breakpoint register)
WBKP	= 16 bits of write data in the host-to-target direction (for BDCBKPT breakpoint register)

A.12 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

A.12.1 Control Timing

Table A-13. Control Timing

Num	C	Rating	Symbol	Min	Typical ¹	Max	Unit
1	D/P	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	20	MHz
2	T	Internal low-power oscillator period	t_{LPO}	—	1500	—	μ s
3	D	External reset pulse width ²	t_{extrst}	$1.5 \times t_{cyc}$	—	—	ns
4	D	Reset low drive ³	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	Active background debug mode latch setup time	t_{MSSU}	25	—	—	ns
6	D	Active background debug mode latch hold time	t_{MSH}	25	—	—	ns
7	D	IRQ/PIAx/ PIBx/PIDx pulse width Asynchronous path ² Synchronous path ³	t_{LIH}, t_{IHIL}	100 $1.5 t_{cyc}$	—	—	ns
8	T	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF) ⁴ Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	40 75	—	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) ⁴ Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	11 35	—	ns

¹ Typical data was characterized at 5.0 V, 25°C unless otherwise stated.

² This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

³ When any reset is initiated, internal circuitry drives the \overline{RESET} pin low for about 34 cycles of t_{cyc} . After POR reset, the bus clock frequency changes to the untrimmed DCO frequency ($f_{reset} = (f_{dco_ut})/4$) because TRIM is reset to 0x80 and FTRIM is reset to 0; and there is an extra divide-by-two because BDIV is reset to 0:1. After other resets, trim stays at the pre-reset value.

⁴ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range -40°C to 125°C .

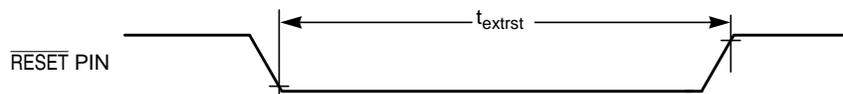
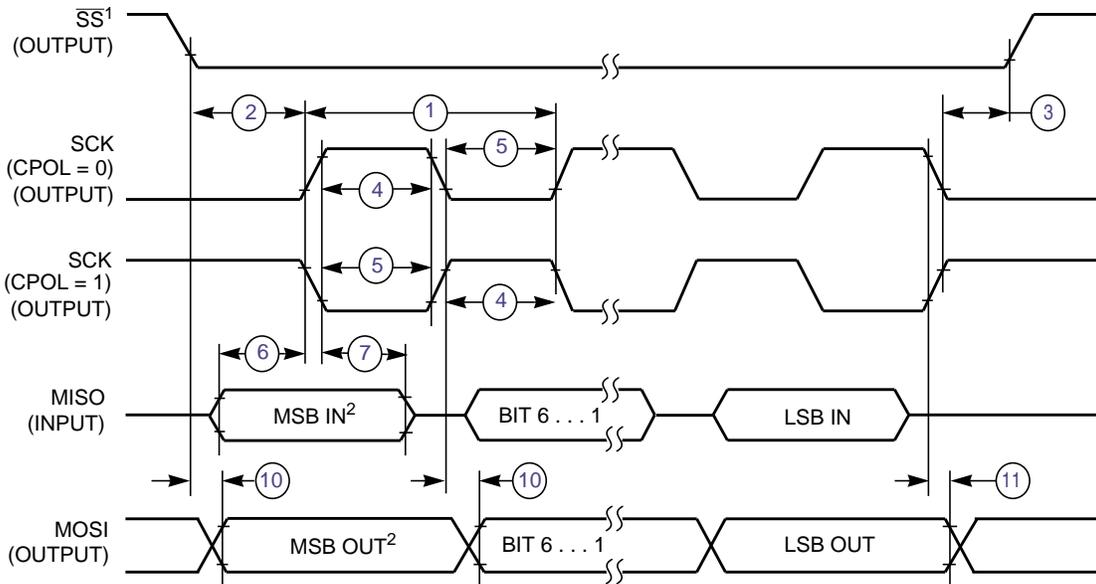
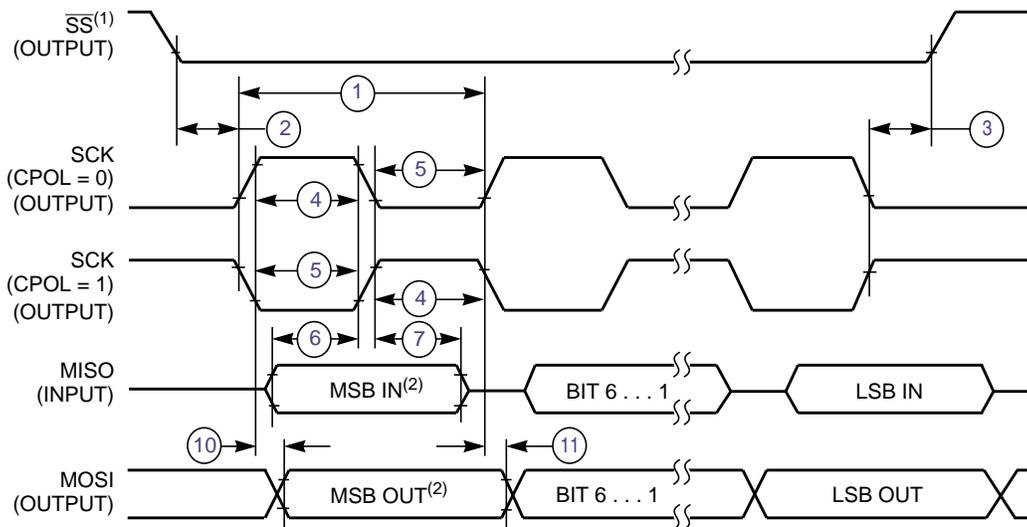


Figure A-2. Reset Timing



NOTES:

1. \overline{SS} output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-7. SPI Master Timing (CPHA = 0)


NOTES:

1. \overline{SS} output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-8. SPI Master Timing (CPHA = 1)

Freescale-provided equate or header file is used to translate these names into the appropriate absolute addresses.

B.2.1 Timer Status and Control Register (TPMxSC)

TPMxSC contains the overflow status flag and control bits that are used to configure the interrupt enable, TPM configuration, clock source, and prescale divisor. These controls relate to all channels within this timer module.

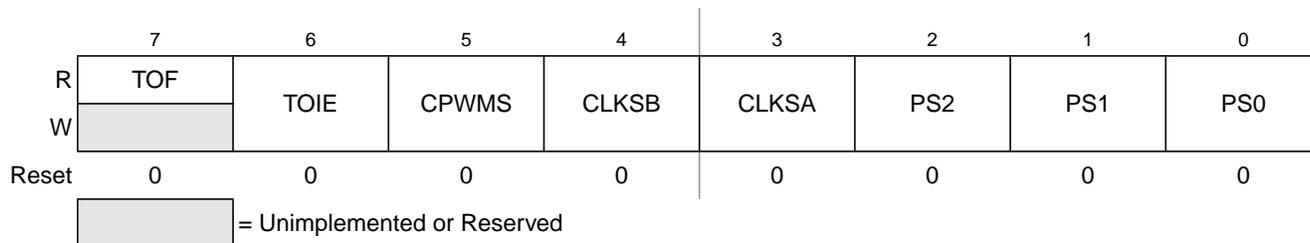


Figure B-2. Timer Status and Control Register (TPMxSC)

Table B-1. TPMxSC Register Field Descriptions

Field	Description
7 TOF	Timer Overflow Flag — This flag is set when the TPM counter changes to 0x0000 after reaching the modulo value programmed in the TPM counter modulo registers. When the TPM is configured for CPWM, TOF is set after the counter has reached the value in the modulo register, at the transition to the next lower count value. Clear TOF by reading the TPM status and control register when TOF is set and then writing a 0 to TOF. If another TPM overflow occurs before the clearing sequence is complete, the sequence is reset so TOF would remain set after the clear sequence was completed for the earlier TOF. Reset clears TOF. Writing a 1 to TOF has no effect. 0 TPM counter has not reached modulo value or overflow 1 TPM counter has overflowed
6 TOIE	Timer Overflow Interrupt Enable — This read/write bit enables TPM overflow interrupts. If TOIE is set, an interrupt is generated when TOF equals 1. Reset clears TOIE. 0 TOF interrupts inhibited (use software polling) 1 TOF interrupts enabled
5 CPWMS	Center-Aligned PWM Select — This read/write bit selects CPWM operating mode. Reset clears this bit so the TPM operates in up-counting mode for input capture, output compare, and edge-aligned PWM functions. Setting CPWMS reconfigures the TPM to operate in up-/down-counting mode for CPWM functions. Reset clears CPWMS. 0 All TPMx channels operate as input capture, output compare, or edge-aligned PWM mode as selected by the MSnB:MSnA control bits in each channel's status and control register 1 All TPMx channels operate in center-aligned PWM mode
4:3 CLKS[B:A]	Clock Source Select — As shown in Table B-2, this 2-bit field is used to disable the TPM system or select one of three clock sources to drive the counter prescaler. The external source and the XCLK are synchronized to the bus clock by an on-chip synchronization circuit.
2:0 PS[2:0]	Prescale Divisor Select — This 3-bit field selects one of eight divisors for the TPM clock input as shown in Table B-3. This prescaler is located after any clock source synchronization or clock source selection, so it affects whatever clock source is selected to drive the TPM system.

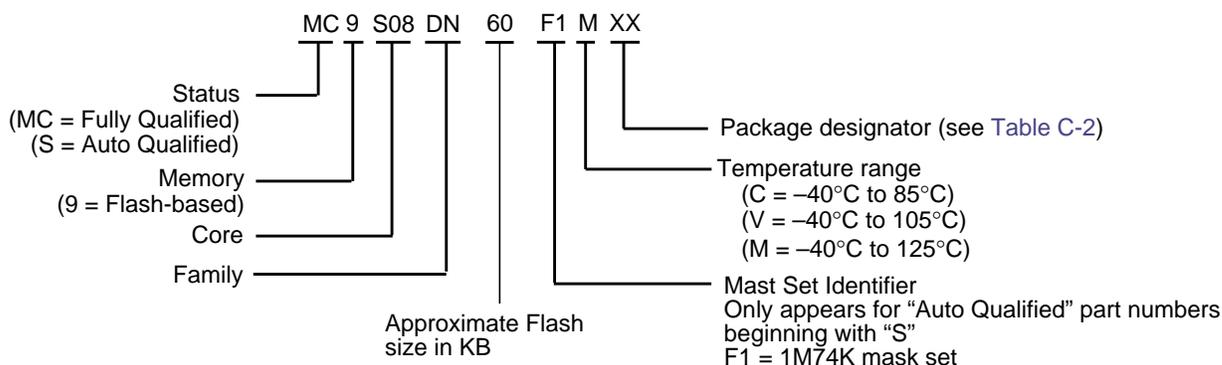
Appendix C

Ordering Information and Mechanical Drawings

C.1 Ordering Information

This section contains ordering information for MC9S08DN60 Series devices.

Example of the device numbering system:



C.1.1 MC9S08DN60 Series Devices

Table C-1. Devices in the MC9S08DN60 Series

Device Number	Memory			Available Packages ¹
	FLASH	RAM	EEPROM	
MC9S08DN60	62,080	2048	2048	64-LQFP, 48-LQFP, 32-LQFP
MC9S08DN48	49,152	2048	1536	
MC9S08DN32	33,792	1536	1024	
MC9S08DN16	16,896	1024	512	48-LQFP, 32-LQFP

¹ See Table C-2 for package information.

C.2 Mechanical Drawings

The following pages are mechanical drawings for the packages described in the following table: