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#### Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I <sup>2</sup> C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08dn60f2vlh">https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08dn60f2vlh</a>

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Table 4-11. FPROT Register Field Descriptions

Field	Description
7:6 EPS	<b>EEPROM Protect Select Bits</b> — This 2-bit field determines the protected EEPROM locations that cannot be erased or programmed. See <a href="#">Table 4-12</a> .
5:0 FPS	<b>Flash Protect Select Bits</b> — This 6-bit field determines the protected Flash locations that cannot be erased or programmed. See <a href="#">Table 4-13</a> .

Table 4-12. EEPROM Block Protection

EPS	Address Area Protected	Memory Size Protected (bytes)	Number of Sectors Protected
0x3	N/A	0	0
0x2	0x17F0 - 0x17FF	32	4
0x1	0x17E0 - 0x17FF	64	8
0x0	0x17C0–0x17FF	128	16

Table 4-13. Flash Block Protection

FPS	Address Area Protected	Memory Size Protected (bytes)	Number of Sectors Protected
0x3F	N/A	0	0
0x3E	0xFA00–0xFFFF	1.5K	2
0x3D	0xF400–0xFFFF	3K	4
0x3C	0xEE00–0xFFFF	4.5K	6
0x3B	0xE800–0xFFFF	6K	8
...	...	...	...
0x37	0xD000–0xFFFF	12K	16
0x36	0xCA00–0xFFFF	13.5K	18
0x35	0xC400–0xFFFF	15K	20
0x34	0xBE00–0xFFFF	16.5K	22
...	...	...	...
0x2C	0x8E00–0xFFFF	28.5K	38
0x2B	0x8800–0xFFFF	30K	40
0x2A	0x8200–0xFFFF	31.5K	42
0x29	0x7C00–0xFFFF	33K	44
...	...	...	...
0x22	0x5200–0xFFFF	43.5K	58
0x21	0x4C00–0xFFFF	45K	60
0x20	0x4600–0xFFFF	46.5K	62
0x1F	0x4000–0xFFFF	48K	64
...	...	...	...

## 5.5 Interrupts

Interrupts provide a way to save the current CPU status and registers, execute an interrupt service routine (ISR), and then restore the CPU status so processing resumes where it left off before the interrupt. Other than the software interrupt (SWI), which is a program instruction, interrupts are caused by hardware events such as an edge on the IRQ pin or a timer-overflow event. The debug module can also generate an SWI under certain circumstances.

If an event occurs in an enabled interrupt source, an associated read-only status flag will become set. The CPU will not respond unless the local interrupt enable is a 1 to enable the interrupt and the I bit in the CCR is 0 to allow interrupts. The global interrupt mask (I bit) in the CCR is initially set after reset which prevents all maskable interrupt sources. The user program initializes the stack pointer and performs other system setup before clearing the I bit to allow the CPU to respond to interrupts.

When the CPU receives a qualified interrupt request, it completes the current instruction before responding to the interrupt. The interrupt sequence obeys the same cycle-by-cycle sequence as the SWI instruction and consists of:

- Saving the CPU registers on the stack
- Setting the I bit in the CCR to mask further interrupts
- Fetching the interrupt vector for the highest-priority interrupt that is currently pending
- Filling the instruction queue with the first three bytes of program information starting from the address fetched from the interrupt vector locations

While the CPU is responding to the interrupt, the I bit is automatically set to avoid the possibility of another interrupt interrupting the ISR itself (this is called nesting of interrupts). Normally, the I bit is restored to 0 when the CCR is restored from the value stacked on entry to the ISR. In rare cases, the I bit can be cleared inside an ISR (after clearing the status flag that generated the interrupt) so that other interrupts can be serviced without waiting for the first service routine to finish. This practice is not recommended for anyone other than the most experienced programmers because it can lead to subtle program errors that are difficult to debug.

The interrupt service routine ends with a return-from-interrupt (RTI) instruction which restores the CCR, A, X, and PC registers to their pre-interrupt values by reading the previously saved information from the stack.

### NOTE

For compatibility with M68HC08 devices, the H register is not automatically saved and restored. It is good programming practice to push H onto the stack at the start of the interrupt service routine (ISR) and restore it immediately before the RTI that is used to return from the ISR.

If more than one interrupt is pending when the I bit is cleared, the highest priority source is serviced first (see [Table 5-1](#)).

### 6.5.3.3 Port C Pull Enable Register (PTCPE)

	7	6	5	4	3	2	1	0
R	PTCPE7	PTCPE6	PTCPE5	PTCPE4	PTCPE3	PTCPE2	PTCPE1	PTCPE0
W								
Reset:	0	0	0	0	0	0	0	0

Figure 6-21. Internal Pull Enable for Port C Register (PTCPE)

Table 6-19. PTCPE Register Field Descriptions

Field	Description
7:0 PTCPE[7:0]	<b>Internal Pull Enable for Port C Bits</b> — Each of these control bits determines if the internal pull-up device is enabled for the associated PTC pin. For port C pins that are configured as outputs, these bits have no effect and the internal pull devices are disabled. 0 Internal pull-up device disabled for port C bit n. 1 Internal pull-up device enabled for port C bit n.

#### NOTE

Pull-down devices only apply when using pin interrupt functions, when corresponding edge select and pin select functions are configured.

### 6.5.3.4 Port C Slew Rate Enable Register (PTCSE)

	7	6	5	4	3	2	1	0
R	PTCSE7	PTCSE6	PTCSE5	PTCSE4	PTCSE3	PTCSE2	PTCSE1	PTCSE0
W								
Reset:	0	0	0	0	0	0	0	0

Figure 6-22. Slew Rate Enable for Port C Register (PTCSE)

Table 6-20. PTCSE Register Field Descriptions

Field	Description
7:0 PTCSE[7:0]	<b>Output Slew Rate Enable for Port C Bits</b> — Each of these control bits determines if the output slew rate control is enabled for the associated PTC pin. For port C pins that are configured as inputs, these bits have no effect. 0 Output slew rate control disabled for port C bit n. 1 Output slew rate control enabled for port C bit n.

**Note:** Slew rate reset default values may differ between engineering samples and final production parts. Always initialize slew rate control to the desired value to ensure correct operation.

### 6.5.4.3 Port D Pull Enable Register (PTDPE)

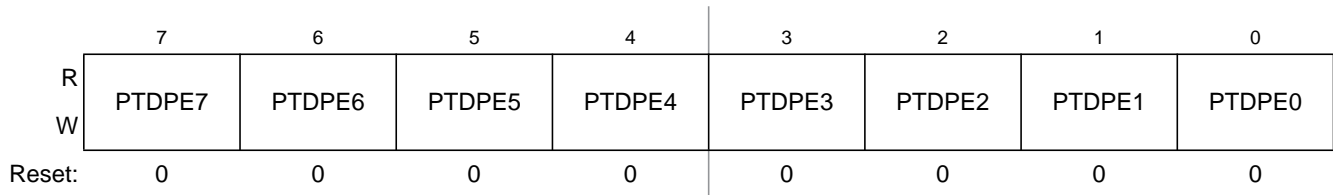


Figure 6-26. Internal Pull Enable for Port D Register (PTDPE)

Table 6-24. PTDPE Register Field Descriptions

Field	Description
7:0 PTDPE[7:0]	<b>Internal Pull Enable for Port D Bits</b> — Each of these control bits determines if the internal pull-up or pull-down device is enabled for the associated PTD pin. For port D pins that are configured as outputs, these bits have no effect and the internal pull devices are disabled. 0 Internal pull-up/pull-down device disabled for port D bit n. 1 Internal pull-up/pull-down device enabled for port D bit n.

#### NOTE

Pull-down devices only apply when using pin interrupt functions, when corresponding edge select and pin select functions are configured.

### 6.5.4.4 Port D Slew Rate Enable Register (PTDSE)

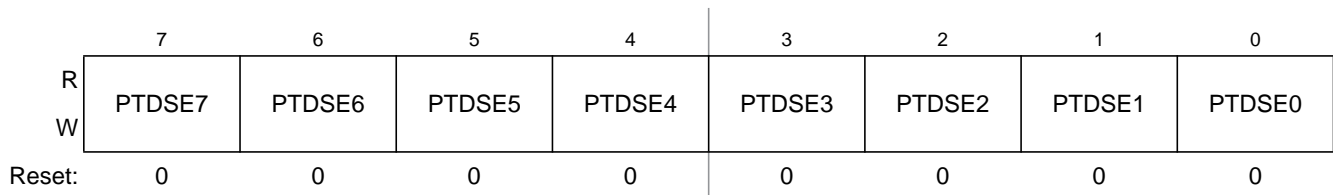


Figure 6-27. Slew Rate Enable for Port D Register (PTDSE)

Table 6-25. PTDSE Register Field Descriptions

Field	Description
7:0 PTDSE[7:0]	<b>Output Slew Rate Enable for Port D Bits</b> — Each of these control bits determines if the output slew rate control is enabled for the associated PTD pin. For port D pins that are configured as inputs, these bits have no effect. 0 Output slew rate control disabled for port D bit n. 1 Output slew rate control enabled for port D bit n.

**Note:** Slew rate reset default values may differ between engineering samples and final production parts. Always initialize slew rate control to the desired value to ensure correct operation.

## 6.5.6 Port F Registers

Port F is controlled by the registers listed below.

### 6.5.6.1 Port F Data Register (PTFD)

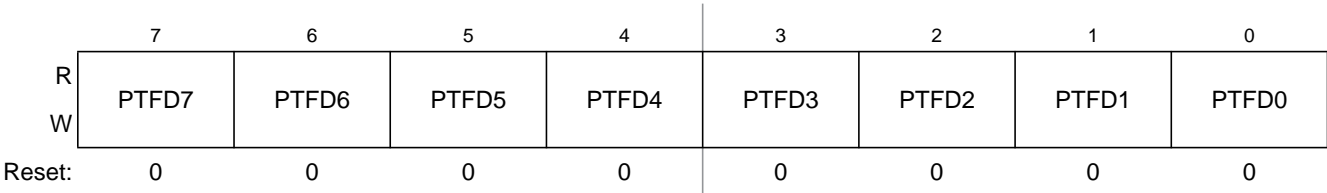


Figure 6-37. Port F Data Register (PTFD)

Table 6-35. PTFD Register Field Descriptions

Field	Description
7:0 PTFD[7:0]	<b>Port F Data Register Bits</b> — For port F pins that are inputs, reads return the logic level on the pin. For port F pins that are configured as outputs, reads return the last value written to this register. Writes are latched into all bits of this register. For port F pins that are configured as outputs, the logic level is driven out the corresponding MCU pin. Reset forces PTFD to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pull-ups disabled.

### 6.5.6.2 Port F Data Direction Register (PTFDD)

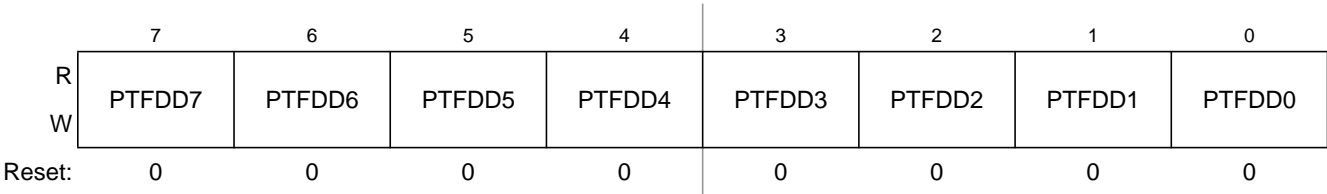


Figure 6-38. Port F Data Direction Register (PTFDD)

Table 6-36. PTFDD Register Field Descriptions

Field	Description
7:0 PTFDD[7:0]	<b>Data Direction for Port F Bits</b> — These read/write bits control the direction of port F pins and what is read for PTFD reads. 0 Input (output driver disabled) and reads return the pin value. 1 Output driver enabled for port F bit n and PTFD reads return the contents of PTFDn.

### 6.5.6.5 Port F Drive Strength Selection Register (PTFDS)

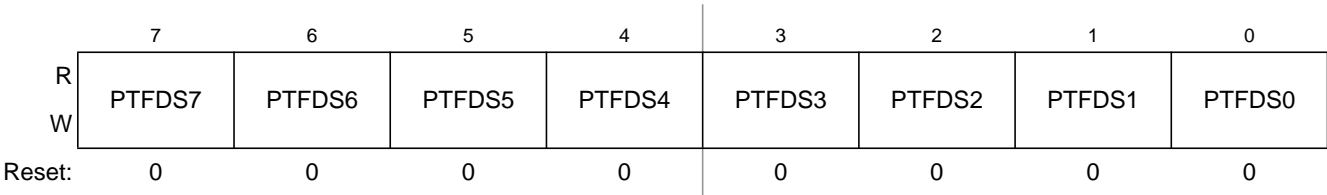


Figure 6-41. Drive Strength Selection for Port F Register (PTFDS)

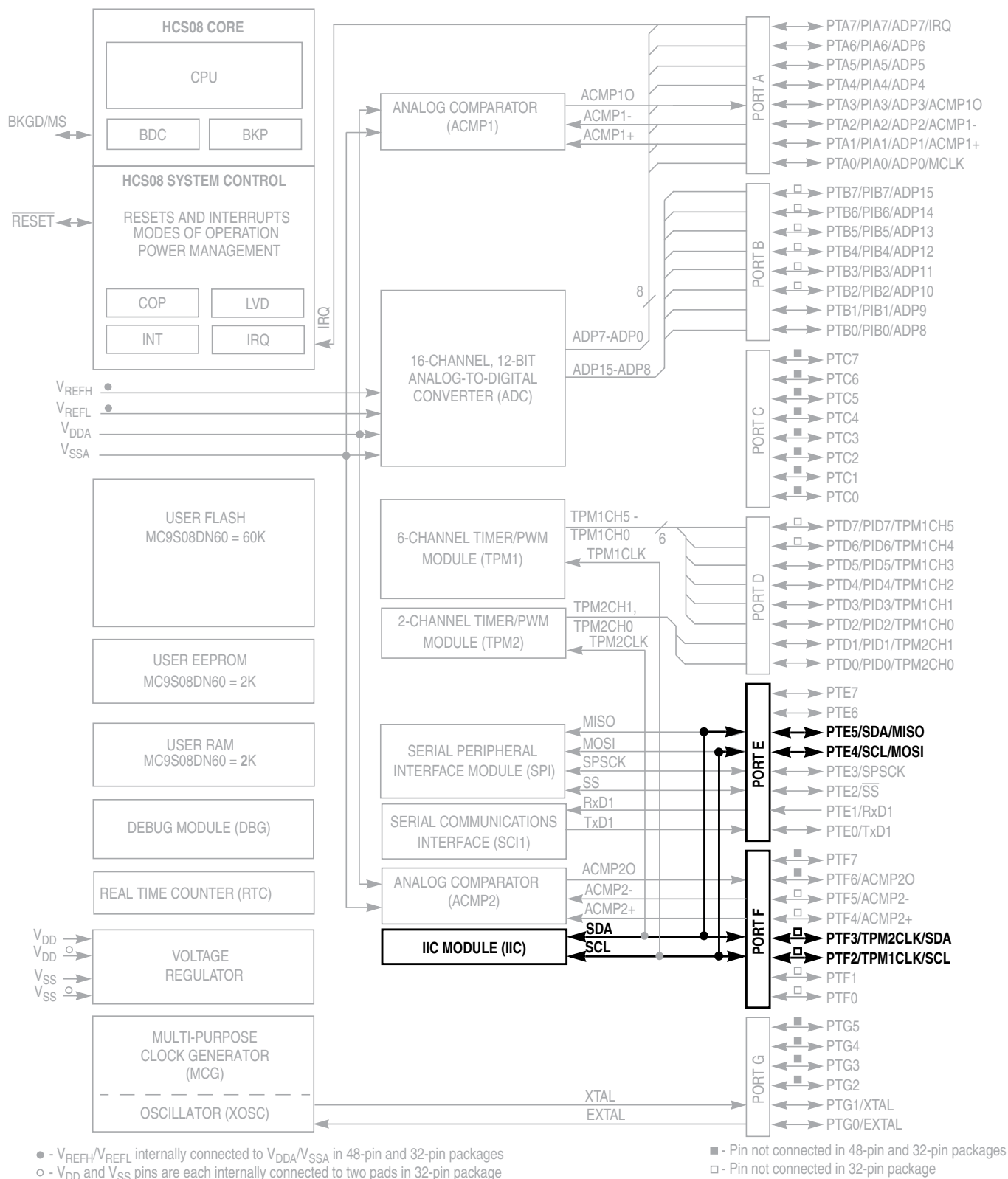
Table 6-39. PTFDS Register Field Descriptions

Field	Description
7:0 PTFDS[7:0]	<b>Output Drive Strength Selection for Port F Bits</b> — Each of these control bits selects between low and high output drive for the associated PTF pin. For port F pins that are configured as inputs, these bits have no effect. 0 Low output drive strength selected for port F bit n. 1 High output drive strength selected for port F bit n.



- c) MCGC1 = 0x98 (%10011000)
  - RDIV (bits 5-3) set to %011, or divide-by-8 because  $8 \text{ MHz} / 8 = 1 \text{ MHz}$  which is in the 1 MHz to 2 MHz range required by the PLL. In BLPE mode, the configuration of the RDIV does not matter because both the FLL and PLL are disabled. Changing them only sets up the the dividers for PLL usage in PBE mode
- d) MCGC3 = 0x44 (%01000100)
  - PLLS (bit 6) set to 1, selects the PLL. In BLPE mode, changing this bit only prepares the MCG for PLL usage in PBE mode
  - VDIV (bits 3-0) set to %0100, or multiply-by-16 because  $1 \text{ MHz reference} * 16 = 16 \text{ MHz}$ . In BLPE mode, the configuration of the VDIV bits does not matter because the PLL is disabled. Changing them only sets up the multiply value for PLL usage in PBE mode
- e) Loop until PLLST (bit 5) in MCGSC is set, indicating that the current source for the PLLS clock is the PLL
3. Then, BLPE mode transitions into PBE mode:
  - a) Clear LP (bit 3) in MCGC2 to 0 here to switch to PBE mode
  - b) Then loop until LOCK (bit 6) in MCGSC is set, indicating that the PLL has acquired lock
4. Last, PBE mode transitions into PEE mode:
  - a) MCGC1 = 0x18 (%00011000)
    - CLKS (bits 7 and 6) in MCGSC1 set to %00 in order to select the output of the PLL as the system clock source
  - b) Loop until CLKST (bits 3 and 2) in MCGSC are %11, indicating that the PLL output is selected to feed MCGOUT in the current clock mode
    - Now, With an RDIV of divide-by-8, a BDIV of divide-by-1, and a VDIV of multiply-by-16,  $\text{MCGOUT} = [(8 \text{ MHz} / 8) * 16] / 1 = 16 \text{ MHz}$ , and the bus frequency is  $\text{MCGOUT} / 2$ , or 8 MHz





**Figure 11-1. MC9S08DN60 Block**

### 11.3.4 IIC Status Register (IICS)

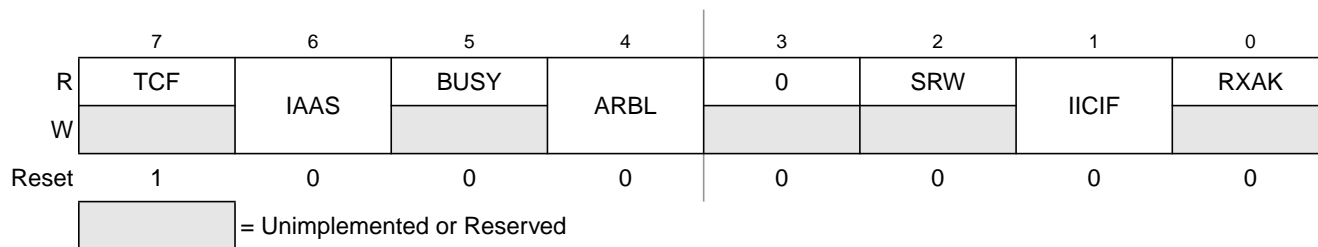


Figure 11-6. IIC Status Register (IICS)

Table 11-6. IICS Field Descriptions

Field	Description
7 TCF	<b>Transfer Complete Flag.</b> This bit is set on the completion of a byte transfer. This bit is only valid during or immediately following a transfer to the IIC module or from the IIC module. The TCF bit is cleared by reading the IICD register in receive mode or writing to the IICD in transmit mode. 0 Transfer in progress 1 Transfer complete
6 IAAS	<b>Addressed as a Slave.</b> The IAAS bit is set when the calling address matches the programmed slave address or when the GCAEN bit is set and a general call is received. Writing the IICC register clears this bit. 0 Not addressed 1 Addressed as a slave
5 BUSY	<b>Bus Busy.</b> The BUSY bit indicates the status of the bus regardless of slave or master mode. The BUSY bit is set when a start signal is detected and cleared when a stop signal is detected. 0 Bus is idle 1 Bus is busy
4 ARBL	<b>Arbitration Lost.</b> This bit is set by hardware when the arbitration procedure is lost. The ARBL bit must be cleared by software by writing a 1 to it. 0 Standard bus operation 1 Loss of arbitration
2 SRW	<b>Slave Read/Write.</b> When addressed as a slave, the SRW bit indicates the value of the R/W command bit of the calling address sent to the master. 0 Slave receive, master writing to slave 1 Slave transmit, master reading from slave
1 IICIF	<b>IIC Interrupt Flag.</b> The IICIF bit is set when an interrupt is pending. This bit must be cleared by software, by writing a 1 to it in the interrupt routine. One of the following events can set the IICIF bit: <ul style="list-style-type: none"> <li>One byte transfer completes</li> <li>Match of slave address to calling address</li> <li>Arbitration lost</li> </ul> 0 No interrupt pending 1 Interrupt pending
0 RXAK	<b>Receive Acknowledge.</b> When the RXAK bit is low, it indicates an acknowledge signal has been received after the completion of one byte of data transmission on the bus. If the RXAK bit is high it means that no acknowledge signal is detected. 0 Acknowledge received 1 No acknowledge received

### 11.4.1.3 Data Transfer

Before successful slave addressing is achieved, the data transfer can proceed byte-by-byte in a direction specified by the  $R/\overline{W}$  bit sent by the calling master.

All transfers that come after an address cycle are referred to as data transfers, even if they carry sub-address information for the slave device

Each data byte is 8 bits long. Data may be changed only while SCL is low and must be held stable while SCL is high as shown in [Figure 11-9](#). There is one clock pulse on SCL for each data bit, the msb being transferred first. Each data byte is followed by a 9th (acknowledge) bit, which is signalled from the receiving device. An acknowledge is signalled by pulling the SDA low at the ninth clock. In summary, one complete data transfer needs nine clock pulses.

If the slave receiver does not acknowledge the master in the ninth bit time, the SDA line must be left high by the slave. The master interprets the failed acknowledge as an unsuccessful data transfer.

If the master receiver does not acknowledge the slave transmitter after a data byte transmission, the slave interprets this as an end of data transfer and releases the SDA line.

In either case, the data transfer is aborted and the master does one of two things:

- Relinquishes the bus by generating a stop signal.
- Commences a new calling by generating a repeated start signal.

### 11.4.1.4 Stop Signal

The master can terminate the communication by generating a stop signal to free the bus. However, the master may generate a start signal followed by a calling command without generating a stop signal first. This is called repeated start. A stop signal is defined as a low-to-high transition of SDA while SCL at logical 1 (see [Figure 11-9](#)).

The master can generate a stop even if the slave has generated an acknowledge at which point the slave must release the bus.

### 11.4.1.5 Repeated Start Signal

As shown in [Figure 11-9](#), a repeated start signal is a start signal generated without first generating a stop signal to terminate the communication. This is used by the master to communicate with another slave or with the same slave in different mode (transmit/receive mode) without releasing the bus.

### 11.4.1.6 Arbitration Procedure

The IIC bus is a true multi-master bus that allows more than one master to be connected on it. If two or more masters try to control the bus at the same time, a clock synchronization procedure determines the bus clock, for which the low period is equal to the longest clock low period and the high is equal to the shortest one among the masters. The relative priority of the contending masters is determined by a data arbitration procedure, a bus master loses arbitration if it transmits logic 1 while another master transmits logic 0. The losing masters immediately switch over to slave receive mode and stop driving SDA output. In this case,

RTCP5 and the RTCLKS[0] bit select the desired divide-by value. If a different value is written to RTCP5, the prescaler and RTCCNT counters are reset to 0x00. Table 14-6 shows different prescaler period values.

**Table 14-6. Prescaler Period**

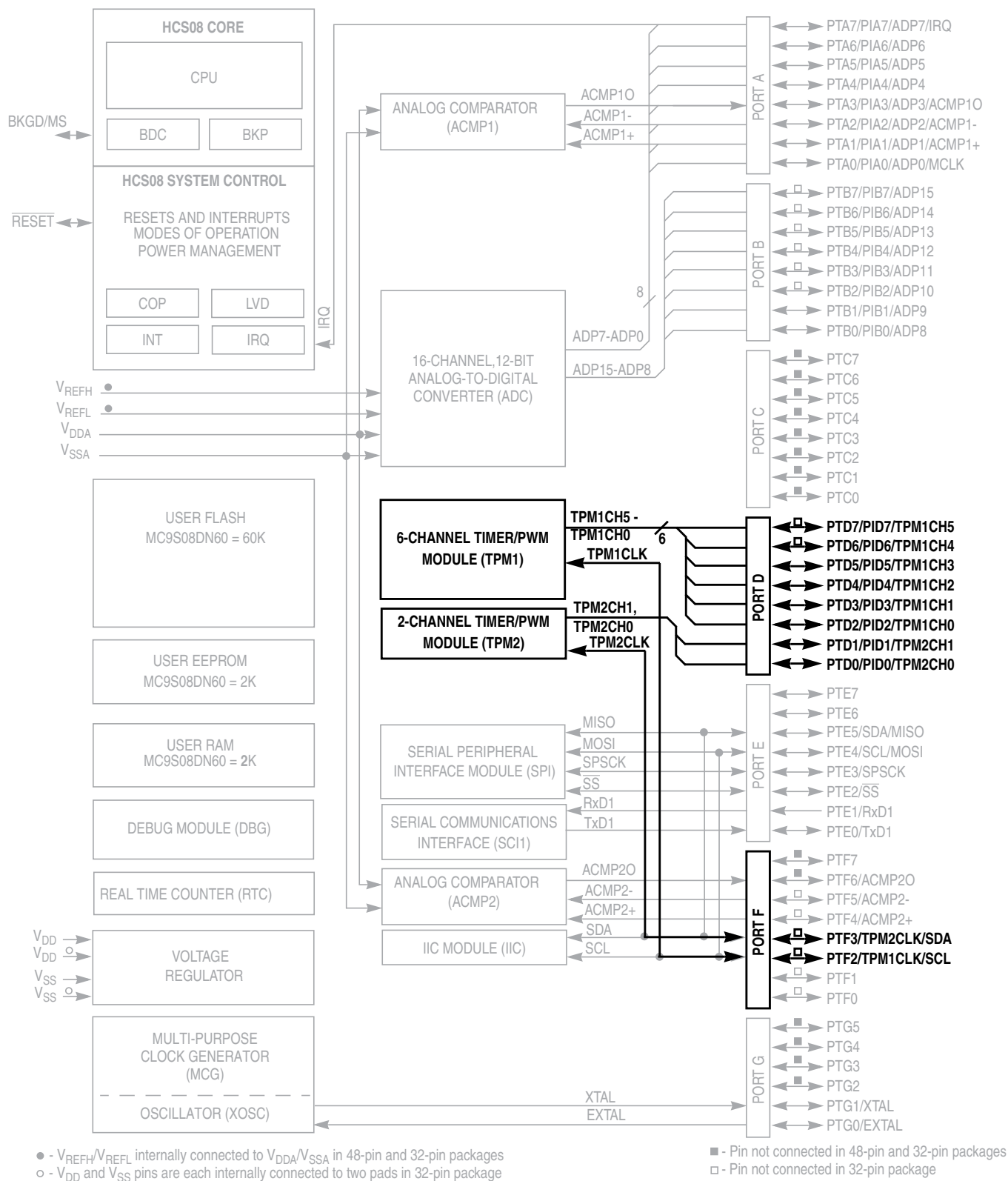
RTCP5	1-kHz Internal Clock (RTCLKS = 00)	1-MHz External Clock (RTCLKS = 01)	32-kHz Internal Clock (RTCLKS = 10)	32-kHz Internal Clock (RTCLKS = 11)
0000	Off	Off	Off	Off
0001	8 ms	1.024 ms	250 $\mu$ s	32 ms
0010	32 ms	2.048 ms	1 ms	64 ms
0011	64 ms	4.096 ms	2 ms	128 ms
0100	128 ms	8.192 ms	4 ms	256 ms
0101	256 ms	16.4 ms	8 ms	512 ms
0110	512 ms	32.8 ms	16 ms	1.024 s
0111	1.024 s	65.5 ms	32 ms	2.048 s
1000	1 ms	1 ms	31.25 $\mu$ s	31.25 ms
1001	2 ms	2 ms	62.5 $\mu$ s	62.5 ms
1010	4 ms	5 ms	125 $\mu$ s	156.25 ms
1011	10 ms	10 ms	312.5 $\mu$ s	312.5 ms
1100	16 ms	20 ms	0.5 ms	0.625 s
1101	0.1 s	50 ms	3.125 ms	1.5625 s
1110	0.5 s	0.1 s	15.625 ms	3.125 s
1111	1 s	0.2 s	31.25 ms	6.25 s

The RTC modulo register (RTCMOD) allows the compare value to be set to any value from 0x00 to 0xFF. When the counter is active, the counter increments at the selected rate until the count matches the modulo value. When these values match, the counter resets to 0x00 and continues counting. The real-time interrupt flag (RTIF) is set when a match occurs. The flag sets on the transition from the modulo value to 0x00. Writing to RTCMOD resets the prescaler and the RTCCNT counters to 0x00.

The RTC allows for an interrupt to be generated when RTIF is set. To enable the real-time interrupt, set the real-time interrupt enable bit (RTIE) in RTCSC. RTIF is cleared by writing a 1 to RTIF.

### 14.4.1 RTC Operation Example

This section shows an example of the RTC operation as the counter reaches a matching value from the modulo register.



**Figure 15-1. MC9S08DN60 Block Diagram**

The TPM channels are programmable independently as input capture, output compare, or edge-aligned PWM channels. Alternately, the TPM can be configured to produce CPWM outputs on all channels. When the TPM is configured for CPWMs, the counter operates as an up/down counter; input capture, output compare, and EPWM functions are not practical.

If a channel is configured as input capture, an internal pullup device may be enabled for that channel. The details of how a module interacts with pin controls depends upon the chip implementation because the I/O pins and associated general purpose I/O controls are not part of the module. Refer to the discussion of the I/O port logic in a full-chip specification.

Because center-aligned PWMs are usually used to drive 3-phase AC-induction motors and brushless DC motors, they are typically used in sets of three or six channels.

## 15.2 Signal Description

Table 15-1 shows the user-accessible signals for the TPM. The number of channels may be varied from one to eight. When an external clock is included, it can be shared with the same pin as any TPM channel; however, it could be connected to a separate input pin. Refer to the I/O pin descriptions in full-chip specification for the specific chip implementation.

**Table 15-1. Signal Properties**

Name	Function
EXTCLK <sup>1</sup>	External clock source which may be selected to drive the TPM counter.
TPMxCHn <sup>2</sup>	I/O pin associated with TPM channel n

<sup>1</sup> When preset, this signal can share any channel pin; however depending upon full-chip implementation, this signal could be connected to a separate external pin.

<sup>2</sup> n=channel number (1 to 8)

Refer to documentation for the full-chip for details about reset states, port connections, and whether there is any pullup device on these pins.

TPM channel pins can be associated with general purpose I/O pins and have passive pullup devices which can be enabled with a control bit when the TPM or general purpose I/O controls have configured the associated pin as an input. When no TPM function is enabled to use a corresponding pin, the pin reverts to being controlled by general purpose I/O controls, including the port-data and data-direction registers. Immediately after reset, no TPM functions are enabled, so all associated pins revert to general purpose I/O control.

### 15.2.1 Detailed Signal Descriptions

This section describes each user-accessible pin signal in detail. Although Table 15-1 grouped all channel pins together, any TPM pin can be shared with the external clock source signal. Since I/O pin logic is not part of the TPM, refer to full-chip documentation for a specific derivative for more details about the interaction of TPM pin functions and general purpose I/O controls including port data, data direction, and pullup controls.



### 15.6.2.1.2 Center-Aligned PWM Case

When CPWMS=1, TOF gets set when the timer counter changes direction from up-counting to down-counting at the end of the terminal count (the value in the modulo register). In this case the TOF corresponds to the end of a PWM period.

### 15.6.2.2 Channel Event Interrupt Description

The meaning of channel interrupts depends on the channel's current mode (input-capture, output-compare, edge-aligned PWM, or center-aligned PWM).

#### 15.6.2.2.1 Input Capture Events

When a channel is configured as an input capture channel, the ELSnB:ELSnA control bits select no edge (off), rising edges, falling edges or any edge as the edge which triggers an input capture event. When the selected edge is detected, the interrupt flag is set. The flag is cleared by the two-step sequence described in [Section 15.6.2, "Description of Interrupt Operation."](#)

#### 15.6.2.2.2 Output Compare Events

When a channel is configured as an output compare channel, the interrupt flag is set each time the main timer counter matches the 16-bit value in the channel value register. The flag is cleared by the two-step sequence described [Section 15.6.2, "Description of Interrupt Operation."](#)

#### 15.6.2.2.3 PWM End-of-Duty-Cycle Events

For channels configured for PWM operation there are two possibilities. When the channel is configured for edge-aligned PWM, the channel flag gets set when the timer counter matches the channel value register which marks the end of the active duty cycle period. When the channel is configured for center-aligned PWM, the timer count matches the channel value register twice during each PWM cycle. In this CPWM case, the channel flag is set at the start and at the end of the active duty cycle period which are the times when the timer counter matches the channel value register. The flag is cleared by the two-step sequence described [Section 15.6.2, "Description of Interrupt Operation."](#)

## 15.7 The Differences from TPM v2 to TPM v3

1. Write to TPMxCNTH:L registers ([Section 15.3.2, "TPM-Counter Registers \(TPMxCNTH:TPMxCNTL\)"](#)) [SE110-TPM case 7]

Any write to TPMxCNTH or TPMxCNTL registers in TPM v3 clears the TPM counter (TPMxCNTH:L) and the prescaler counter. Instead, in the TPM v2 only the TPM counter is cleared in this case.

2. Read of TPMxCNTH:L registers ([Section 15.3.2, "TPM-Counter Registers \(TPMxCNTH:TPMxCNTL\)"](#))

— In TPM v3, any read of TPMxCNTH:L registers during BDM mode returns the value of the TPM counter that is frozen. In TPM v2, if only one byte of the TPMxCNTH:L registers was read before the BDM mode became active, then any read of TPMxCNTH:L registers during

## A.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

### A.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

**Table A-17. Radiated Emissions for 3M05C Mask Set**

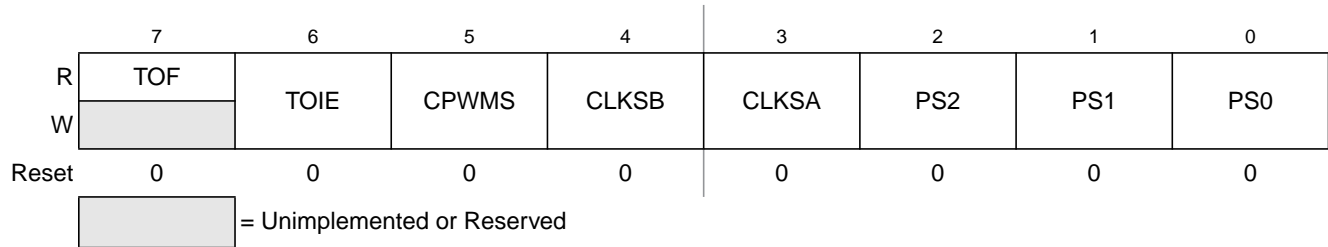
Parameter	Symbol	Conditions	Frequency	$f_{osc}/f_{CPU}$	Level <sup>1</sup> (Max)	Unit
Radiated emissions, electric field — Conditions -	$V_{RE\_TEM}$	$V_{DD} = 5$ $T_A = +25^{\circ}C$ 64 LQFP	0.15 – 50 MHz	16 MHz Crystal 20 MHz Bus	18	dBμV
			50 – 150 MHz		18	
			150 – 500 MHz		13	
			500 – 1000 MHz		7	
			IEC Level		L	—
			SAE Level		2	—

<sup>1</sup> Data based on qualification test results.

Freescall-provided equate or header file is used to translate these names into the appropriate absolute addresses.

## B.2.1 Timer Status and Control Register (TPMxSC)

TPMxSC contains the overflow status flag and control bits that are used to configure the interrupt enable, TPM configuration, clock source, and prescale divisor. These controls relate to all channels within this timer module.



**Figure B-2. Timer Status and Control Register (TPMxSC)**

**Table B-1. TPMxSC Register Field Descriptions**

Field	Description
7 TOF	<b>Timer Overflow Flag</b> — This flag is set when the TPM counter changes to 0x0000 after reaching the modulo value programmed in the TPM counter modulo registers. When the TPM is configured for CPWM, TOF is set after the counter has reached the value in the modulo register, at the transition to the next lower count value. Clear TOF by reading the TPM status and control register when TOF is set and then writing a 0 to TOF. If another TPM overflow occurs before the clearing sequence is complete, the sequence is reset so TOF would remain set after the clear sequence was completed for the earlier TOF. Reset clears TOF. Writing a 1 to TOF has no effect. 0 TPM counter has not reached modulo value or overflow 1 TPM counter has overflowed
6 TOIE	<b>Timer Overflow Interrupt Enable</b> — This read/write bit enables TPM overflow interrupts. If TOIE is set, an interrupt is generated when TOF equals 1. Reset clears TOIE. 0 TOF interrupts inhibited (use software polling) 1 TOF interrupts enabled
5 CPWMS	<b>Center-Aligned PWM Select</b> — This read/write bit selects CPWM operating mode. Reset clears this bit so the TPM operates in up-counting mode for input capture, output compare, and edge-aligned PWM functions. Setting CPWMS reconfigures the TPM to operate in up-/down-counting mode for CPWM functions. Reset clears CPWMS. 0 All TPMx channels operate as input capture, output compare, or edge-aligned PWM mode as selected by the MSnB:MSnA control bits in each channel's status and control register 1 All TPMx channels operate in center-aligned PWM mode
4:3 CLKS[B:A]	<b>Clock Source Select</b> — As shown in <a href="#">Table B-2</a> , this 2-bit field is used to disable the TPM system or select one of three clock sources to drive the counter prescaler. The external source and the XCLK are synchronized to the bus clock by an on-chip synchronization circuit.
2:0 PS[2:0]	<b>Prescale Divisor Select</b> — This 3-bit field selects one of eight divisors for the TPM clock input as shown in <a href="#">Table B-3</a> . This prescaler is located after any clock source synchronization or clock source selection, so it affects whatever clock source is selected to drive the TPM system.

Table C-2. Package Descriptions

Pin Count	Type	Abbreviation	Designator	Document No.
64	Low Quad Flat Package	LQFP	LH	98ASS23234W
48	Low Quad Flat Package	LQFP	LF	98ASH00962A
32	Low Quad Flat Package	LQFP	LC	98ASH70029A



NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.
- 3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
- 4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.
- 5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.
- 6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
- 7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
- 8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

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TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A		REV: D
	CASE NUMBER: 873A-03		19 MAY 2005
	STANDARD: JEDEC MS-026 BBA		