Analog Devices Inc./Maxim Integrated - 73S1209F-44IM/F/P Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80515
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SmartCard, UART/USART
Peripherals	LED, POR, WDT
Number of I/O	9
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/73s1209f-44im-f-p

FEATURES

80515 Core:

- 1 clock cycle per instruction (most instructions)
- CPU clocked up to 24MHz
- 32kB Flash memory with security
- 2kB XRAM (User Data Memory)
- 256 byte IRAM
- Hardware watchdog timer

Oscillators:

- Single low-cost 6MHz to 12MHz crystal
- An Internal PLL provides all the necessary clocks to each block of the system

Interrupts:

- Standard 80C515 4-priority level structure
- 9 different sources of interrupt to the core

Power Down Modes:

- 2 standard 80C515 Power Down and IDLE modes
- Extensive device power down mode

Timers:

- (2) Standard 80C52 timers T0 and T1
- (1) 16-bit timer

Built-in ISO-7816 Card Interface:

- Linear regulator produces VCC for the card (1.8V, 3V or 5V)
- Full compliance with EMV 4.1
- Activation/Deactivation sequencers
- Auxiliary I/O lines (C4 and C8 signals)
- 7kV ESD protection on all interface pins

Communication with Smart Cards:

- ISO-7816 UART for protocols T=0, T=1
- (2) 2-Byte FIFOs for transmit and receive
- Configured to drive multiple external Teridian 73S8010x interfaces (for multi-SAM architectures)

Communication Interfaces:

- Full-duplex serial interface (1200bps to 115kbps UART)
- I^2C Master Interface (400kbps)

Man-Machine Interface and I/Os:

- 5x6 Keyboard (hardware scanning, debouncing and scrambling)
- (9) User I/Os
- Up to 2 programmable current outputs (LED)

Voltage Detection:

- Analog Input (detection range: 1.0V to 2.5V)
- Operating Voltage:
- 2.7V to 3.6V Digital power supply
- 4.75 to 5.5V Analog, smart card power supply

Operating Temperature:

- -40°C to 85°C

Package:

- 68-pin QFN, 44-pin QFN

Software:

- Turnkey firmware:
  - Compliant with PC/SC, CCID, ISO7816 and EMV4.1 specifications
  - Features a Power Down mode accessible form the host
  - Supports Plug & Play over serial interface
  - Windows® XP driver available (*)
  - Windows CE / Mobile driver available (*)
  - Linux and other OS: Upon request
- Or for custom developments:
  - A complete set of ISO-7816, EMV4.1 and low-level libraries are available for T=0 / T=1
  - Two-level Application Programming Interface (ANSI C-language libraries)

(*) Contact Teridian Semiconductor for conditions and availability

Tables

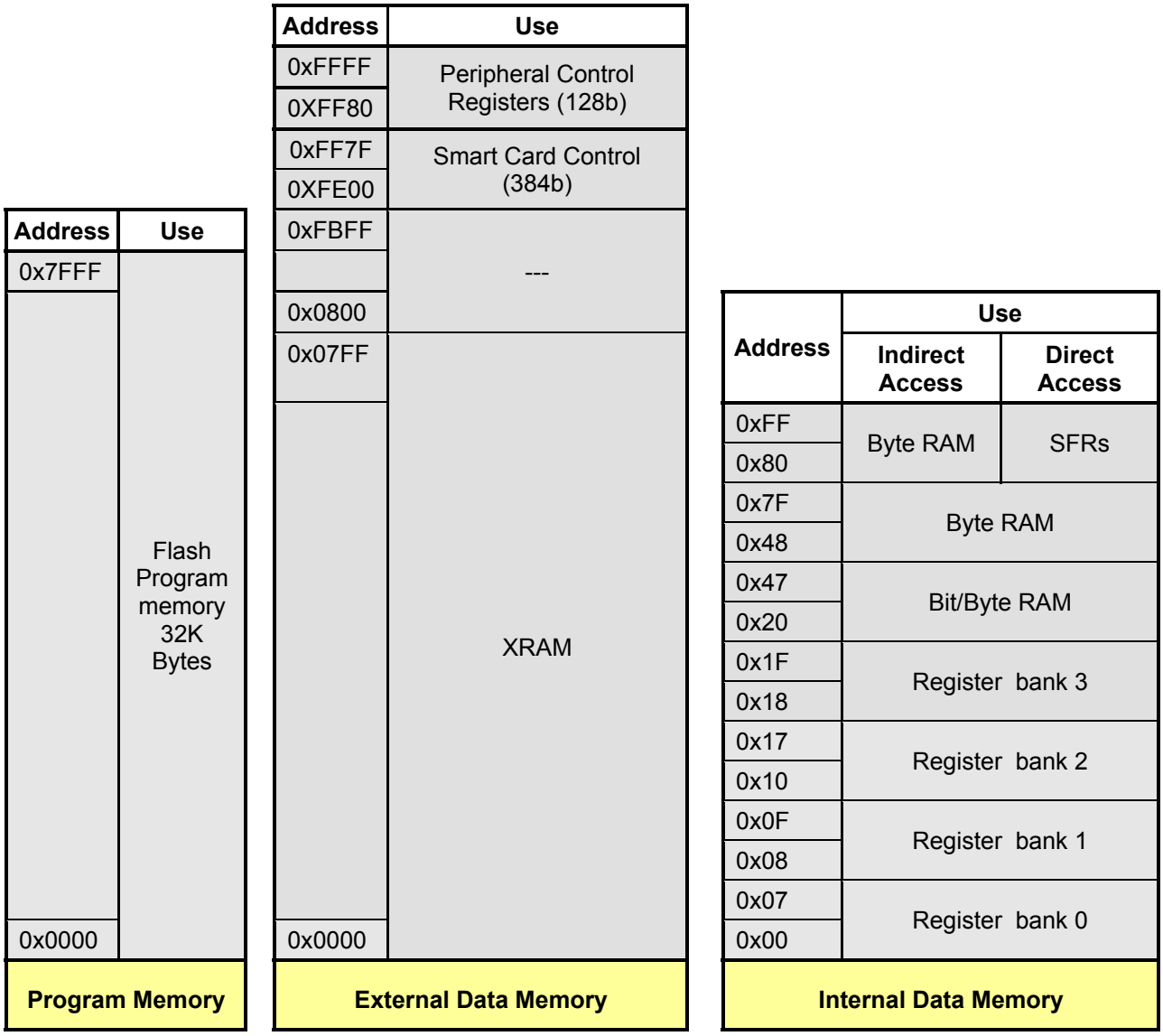


Figure 2: Memory Map

Dual Data Pointer: The Dual Data Pointer accelerates the block moves of data. The standard DPTR is a 16-bit register that is used to address external memory. In the 80515 core, the standard data pointer is called DPTR, the second data pointer is called DPTR1. The data pointer select bit chooses the active pointer. The data pointer select bit is located at the LSB of the DPS IRAM special function register (DPS.0). DPTR is selected when DPS.0 = 0 and DPTR1 is selected when DPS.0 = 1.

The user switches between pointers by toggling the LSB of the DPS register. All DPTR-related instructions use the currently selected DPTR for any activity.

Note: The second data pointer may not be supported by certain compilers.

1.5 Special Function Registers (SFRs)

The 73S1209F utilizes numerous SFRs to communicate with the 73S1209F s many peripherals. This results in the need for more SFR locations outside the direct address IRAM space (0x80 to 0xFF). While some peripherals are mapped to unused IRAM SFR locations, additional SFRs for the smart card and other peripheral functions are mapped to the top of the XRAM data space (0xFC00 to 0xFFFF).

1.5.1 Internal Data Special Function Registers (SFRs)

A map of the Special Function Registers is shown in Table 6.

Table 6: IRAM Special Function Registers Locations

Hex\ Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/ Hex
F8									FF
F0	B								F7
E8									EF
E0	A								E7
D8	BRCON								DF
D0	PSW	**KCOL**	**KROW**	**KSCAN**	**KSTAT**	**KSIZE**	**KORDERL**	**KORDERH**	D7
C8	T2CON								CF
C0	IRCON								C7
B8	IEN1	IP1	S0RELH	S1RELH					BF
B0			**FLSHCTL**					**PGADDR**	B7
A8	IEN0	IP0	S0RELL						AF
A0	**USR8**	**UDIR8**							A7
98	S0CON	S0BUF	IEN2	S1CON	S1BUF	S1RELL			9F
90	**USR70**	**UDIR70**	DPS		**ERASE**				97
88	TCON	TMOD	TL0	TL1	TH0	TH1		**MCLKCtl**	8F
80		SP	DPL	DPH	DPL1	DPH1	WDTREL	PCON	87

Only a few addresses are used, the others are not implemented. SFRs specific to the 73S1209F are shown in **bold** print (gray background). Any read access to unimplemented addresses will return undefined data, while most write access will have no effect. However, a few locations are reserved and not user configurable in the 73S1209F. **Writes to the unused SFR locations can affect the operation of the core and therefore must not be written to. This applies to all the SFR areas in both the IRAM and XRAM spaces. In addition, all unused bit locations within valid SFR registers must be left in their default (power on default) states.**

MPU Clock Control Register (MPUCKCtl): 0xFFA1 ← 0x0C

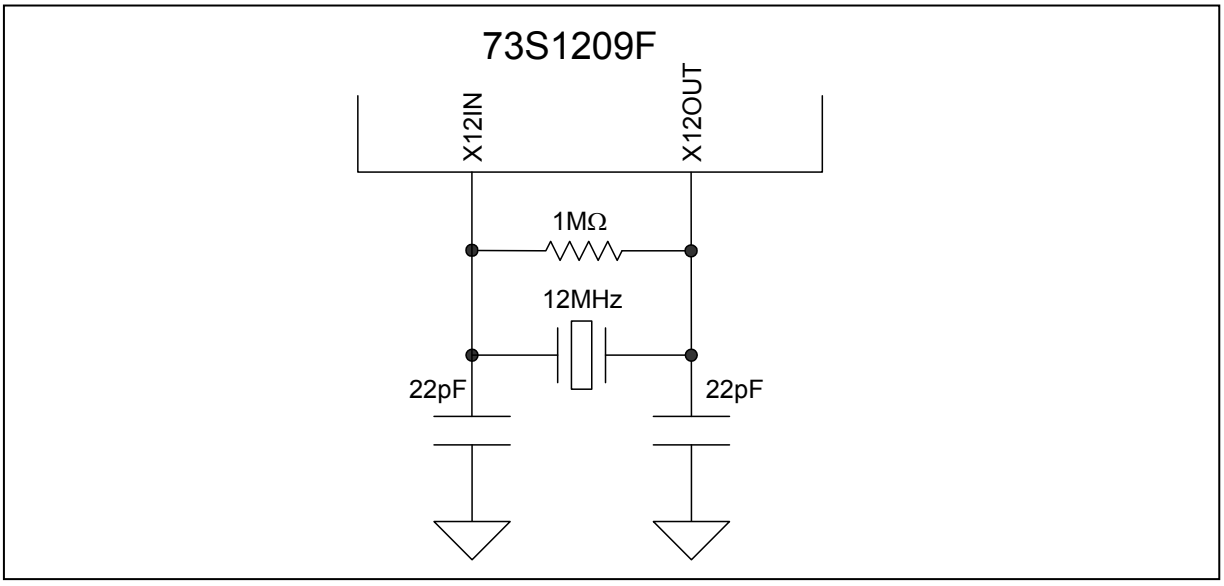
Table 13: The MPUCKCtl Register

MSB							LSB
–	–	MDIV.5	MDIV.4	MDIV.3	MDIV.2	MDIV.1	MDIV.0

Bit	Symbol	Function
MPUCKCtl.7	–	
MPUCKCtl.6	–	
MPUCKCtl.5	MDIV.5	This value determines the ratio of the MPU master clock frequency to the VCO frequency (MCLK) such that MPUClk = MCLK/(2 * (MPUCKDiv(5:0) + 1)). Do not use values of 0 or 1 for MPUCKDiv(n). Default is 0Ch to set CPCLK = 3.6923MHz.
MPUCKCtl.4	MDIV.4	
MPUCKCtl.3	MDIV.3	
MPUCKCtl.2	MDIV.2	
MPUCKCtl.1	MDIV.1	
MPUCKCtl.0	MDIV.0	

The oscillator circuits are designed to connect directly to standard parallel resonant crystal in a Pierce oscillator configuration. Each side of the crystal should include a 22pF capacitor to ground for both oscillator circuits and a 1MΩ resistor is required across the 12MHz crystal.

The CPU clock is available as an output on pin CPUCLK (68-pin version only).



Note: The crystal should be placed as close as possible to the IC, and vias should be avoided.

Figure 4: Oscillator Circuit

External Interrupt Control Register (INT5Ctl): 0xFF94 ← 0x00

Table 14: The INT5Ctl Register

MSB							LSB
PDMUX	–	–	–	–	–	KPIEN	KPINT

Bit	Symbol	Function
INT5Ctl.7	PDMUX	When set=1, enables interrupts from Keypad (normally going to int5), Smart Card interrupts (normally going to int4), or USR(7:0) pins (int0) to cause interrupt on int0. The assertion of the interrupt to int0 is delayed by 512 MPU clocks to allow the analog circuits, including the clock system, to stabilize. This bit must be set prior to asserting the PWRDN bit in order to properly configure the interrupts that will wake up the circuit. This bit is reset=0 when this register is read.
INT5Ctl.6	–	
INT5Ctl.5	–	
INT5Ctl.4	–	
INT5Ctl.3	–	
INT5Ctl.2	–	
INT5Ctl.1	KPIEN	Keypad interrupt enable.
INT5Ctl.0	KPINT	Keypad interrupt flag.

Miscellaneous Control Register 0 (MISCtl0): 0xFFF1 ← 0x00

Table 15: The MISCtl0 Register

MSB							LSB
PWRDN	–	–	–	–	–	SLPBK	SSEL

Bit	Symbol	Function
MISCtl0.7	PWRDN	This bit sets the circuit into a low-power condition. All analog (high speed oscillator and VCO/PLL) functions are disabled 32 MPU clock cycles after this bit is set=1. This allows time for the next instruction to set the STOP bit in the PCON register to stop the CPU core. The MPU is not operative in this mode. When set, this bit overrides the individual control bits that otherwise control power consumption.
MISCtl0.6	–	
MISCtl0.5	–	
MISCtl0.4	–	
MISCtl0.3	–	
MISCtl0.2	–	
MISCtl0.1	SLPBK	UART loop back testing mode.
MISCtl0.0	SSEL	Serial port pins select.

Interrupt Enable 0 Register (IEN0): 0xA8 ← 0x00

Table 44: The IEN0 Register

MSB							LSB
EAL	WDT	ET2	ES0	ET1	EX1	ET0	EX0

Bit	Symbol	Function
IEN0.7	EAL	EAL = 0 – disable all interrupts.
IEN0.6	WDT	Watchdog timer refresh flag. Set to initiate a refresh of the watchdog timer. Must be set directly before SWDT is set to prevent an unintentional refresh of the watchdog timer. WDT is reset by hardware 12 clock cycles after it has been set.
IEN0.5	–	
IEN0.4	ES0	ES0 = 0 – disable serial channel 0 interrupt.
IEN0.3	ET1	ET1 = 0 – disable timer 1 overflow interrupt.
IEN0.2	EX1	EX1 = 0 – disable external interrupt 1.
IEN0.1	ET0	ET0 = 0 – disable timer 0 overflow interrupt.
IEN0.0	EX0	EX0 = 0 – disable external interrupt 0.

Interrupt Enable 1 Register (IEN1): 0xB8 ← 0x00

Table 45: The IEN1 Register

MSB							LSB
–	SWDT	EX6	EX5	EX4	EX3	EX2	

Bit	Symbol	Function
IEN1.7	–	
IEN1.6	SWDT	Watchdog timer start/refresh flag. Set to activate/refresh the watchdog timer. When directly set after setting WDT, a watchdog timer refresh is performed. Bit SWDT is reset by the hardware 12 clock cycles after it has been set.
IEN1.5	EX6	EX6 = 0 – disable external interrupt 6.
IEN1.4	EX5	EX5 = 0 – disable external interrupt 5.
IEN1.3	EX4	EX4 = 0 – disable external interrupt 4.
IEN1.2	EX3	EX3 = 0 – disable external interrupt 3.
IEN1.1	EX2	EX2 = 0 – disable external interrupt 2.
IEN1.0	–	

External Interrupt Control Register (USRIntCtl1) : 0xFF90 ← 0x00

Table 51: The USRIntCtl1 Register

MSB							LSB
–	U1IS.6	U1IS.5	U1IS.4	–	U0IS.2	U0IS.1	U0IS.0

External Interrupt Control Register (USRIntCtl2) : 0xFF91 ← 0x00

Table 52: The USRIntCtl2 Register

MSB							LSB
–	U3IS.6	U3IS.5	U3IS.4	–	U2IS.2	U2IS.1	U2IS.0

External Interrupt Control Register (USRIntCtl3) : 0xFF92 ← 0x00

Table 53: The USRIntCtl3 Register

MSB							LSB
–	U5IS.6	U5IS.5	U5IS.4	–	U4IS.2	U4IS.1	U4IS.0

External Interrupt Control Register (USRIntCtl4) : 0xFF93 ← 0x00

Table 54: The USRIntCtl4 Register

MSB							LSB
–	U7IS.6	U7IS.5	U7IS.4	–	U6IS.2	U6IS.1	U6IS.0

1.7.9 LED Drivers

The 73S1209F provides two dedicated output pins for driving LEDs. The LED driver pins can be configured as current sources that will pull to ground to drive LEDs that are connected to VDD without the need for external current limiting resistors. These pins may be used as general purpose outputs with the programmed pull-down current and a strong (CMOS) pull-up, if enabled. The analog block must be enabled when these outputs are being used to drive the selected output current.

The pins may be used as inputs with consideration of the programmed output current and level. The register bit when read, indicates the state of the pin.

LED Control Register (LEDCtl): 0xFFF3 ← 0xFF

Table 57: The LEDCtl Register

MSB LSB

–	LPUEN	ISET.1	ISET.0	–	–	LEDD 1	LEDD0

Bit	Symbol	Function
LEDCtl.7	–	
LEDCtl.6	LPUEN	0 = Pull-ups are enabled for all of the LED pins.
LEDCtl.5	ISET.1	These two bits control the drive current (to ground) for all of the LED driver pins. Current levels are: 00 = 0ma(off) 01 = 2ma 10 = 4ma 11 = 10ma
LEDCtl.4	ISET.0	
LEDCtl.3	–	
LEDCtl.2	–	
LEDCtl.1	LEDD1	Write data controls output level of pin LED1. Read will report level of pin LED1.
LEDCtl.0	LEDD0	Write data controls output level of pin LED0. Read will report level of pin LED0.

1.7.10 I²C Master Interface

The 73S1209F includes a dedicated fast mode, 400kHz I²C Master interface. The I²C interface can read or write 1 or 2 bytes of data per data transfer frame. The MPU communicates with the interface through six dedicated SFR registers:

- Device Address (DAR)
- Write Data (WDR)
- Secondary Write Data (SWDR)
- Read Data (RDR)
- Secondary Read Data (SRDR)
- Control and Status (CSR)

The DAR register is used to set up the slave address and specify if the transaction is a read or write operation. The CSR register sets up, starts the transaction and reports any errors that may occur. When the I²C transaction is complete, the I²C interrupt is reported via external interrupt 6. The I²C interrupt is automatically de-asserted when a subsequent I²C transaction is started. The I²C interface uses a 400kHz clock from the time-base circuits.

1.7.10.1 I²C Write Sequence

To write data on the I²C Master Bus, the 80515 has to program the following registers according to the following sequence:

1. Write slave device address to Device Address register (DAR). The data contains 7 bits for the slave device address and 1 bit of op-code. The op-code bit should be written with a 0 to indicate a write operation.
2. Write data to Write Data register (WDR). This data will be transferred to the slave device.
3. If writing 2 bytes, set bit 0 of the Control and Status register (CSR) and load the second data byte to Secondary Write Data register (SWDR).
4. Set bit 1 of the CSR register to start I²C Master Bus.
5. Wait for I²C interrupt to be asserted. It indicates that the write on I²C Master Bus is done. Refer to information about the INT6Ctl, IEN1 and IRCON register for masking and flag operation.

Device Address Register (DAR): 0xFF80 ← 0x00

Table 58: The DAR Register

MSB							LSB
DVADR.6	DVADR.5	DVADR.4	DVADR.3	DVADR.2	DVADR.1	DVADR.0	I2CRW

Bit	Symbol	Function
DAR.7	DVADR [0:6]	Slave device address.
DAR.6		
DAR.5		
DAR.4		
DAR.3		
DAR.2		
DAR.1		
DAR.0	I2CRW	If set = 0, the transaction is a write operation. If set = 1, read.

I2C Write Data Register (WDR): 0XFF81 ← 0x00

Table 59: The WDR Register

MSB							LSB
WDR.7	WDR.6	WDR.5	WDR.4	WDR.3	WDR.2	WDR.1	WDR.0

Bit	Function
WDR.7	Data to be written to the I^2C slave device.
WDR.6	
WDR.5	
WDR.4	
WDR.3	
WDR.2	
WDR.1	
WDR.0	

1.7.11 Keypad Interface

The 73S1209F supports a 30-button (6 row x 5 column) keypad (SPST Mechanical Contact Switches) interface using 11 dedicated I/O pins. Figure 11 shows a simplified block diagram of the keypad interface.

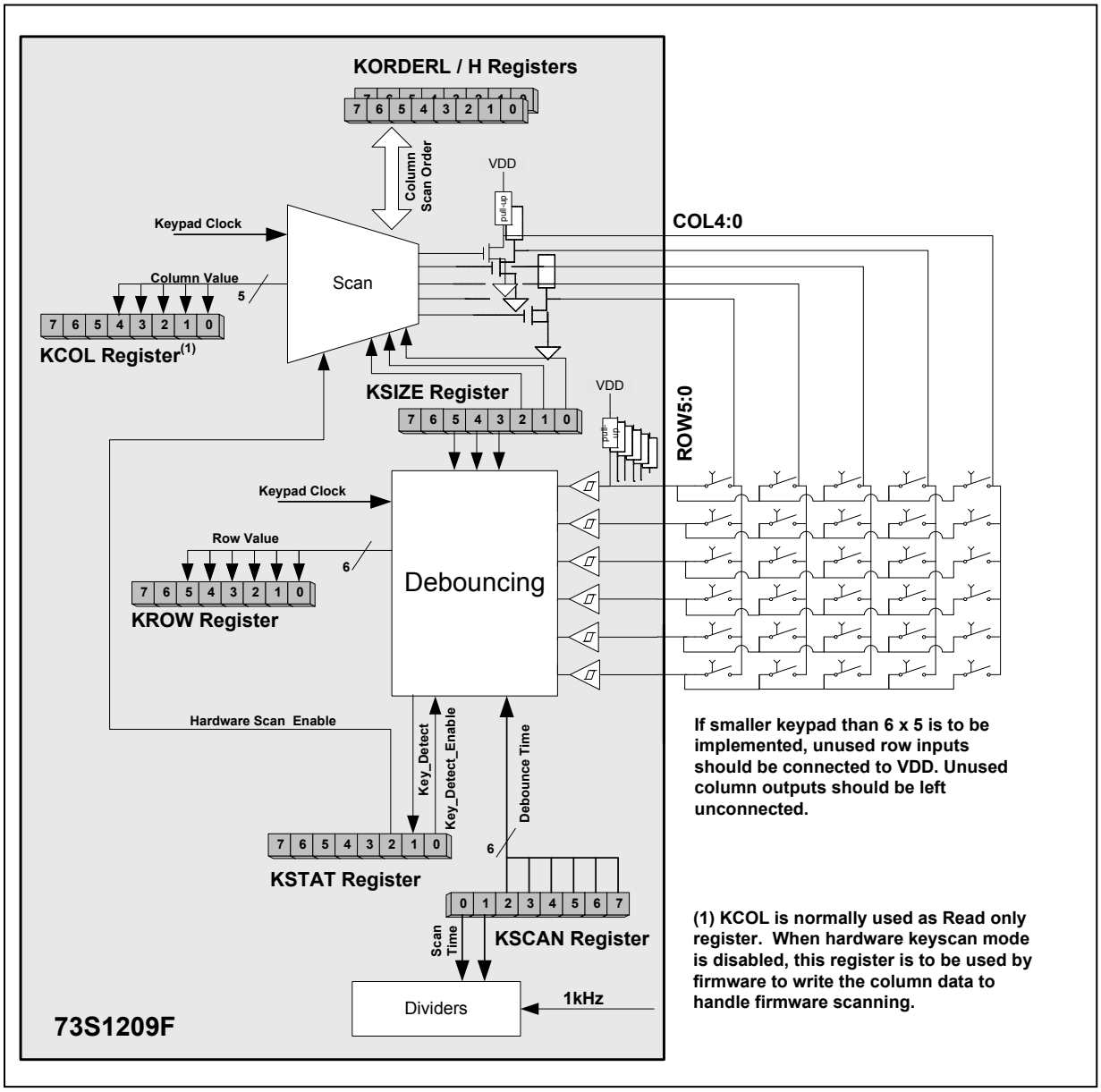


Figure 11: Simplified Keypad Block Diagram

There are 5 drive lines (outputs) corresponding to columns and 6 sense lines (inputs) corresponding to rows. Hysteresis and pull-ups are provided on all inputs (rows), which eliminate the need for external resistors in the keypad. Key scanning happens by asserting one of the 5 column lines low and looking for a low on a sense line indicating that a key is pressed (switch closed) at the intersection of the drive/sense (col/row) line in the keypad. Key detection is performed by hardware with an incorporated debounce timer. Debouncing time is adjustable through the KSCAN Register. Internal hardware circuitry performs column scanning at an adjustable scanning rate and column scanning order through registers KSCAN and KORDERL / KORDERH. Key scanning is disabled at reset and must be enabled by firmware. When a valid key is detected, an interrupt is generated and the valid value of the pressed key is automatically

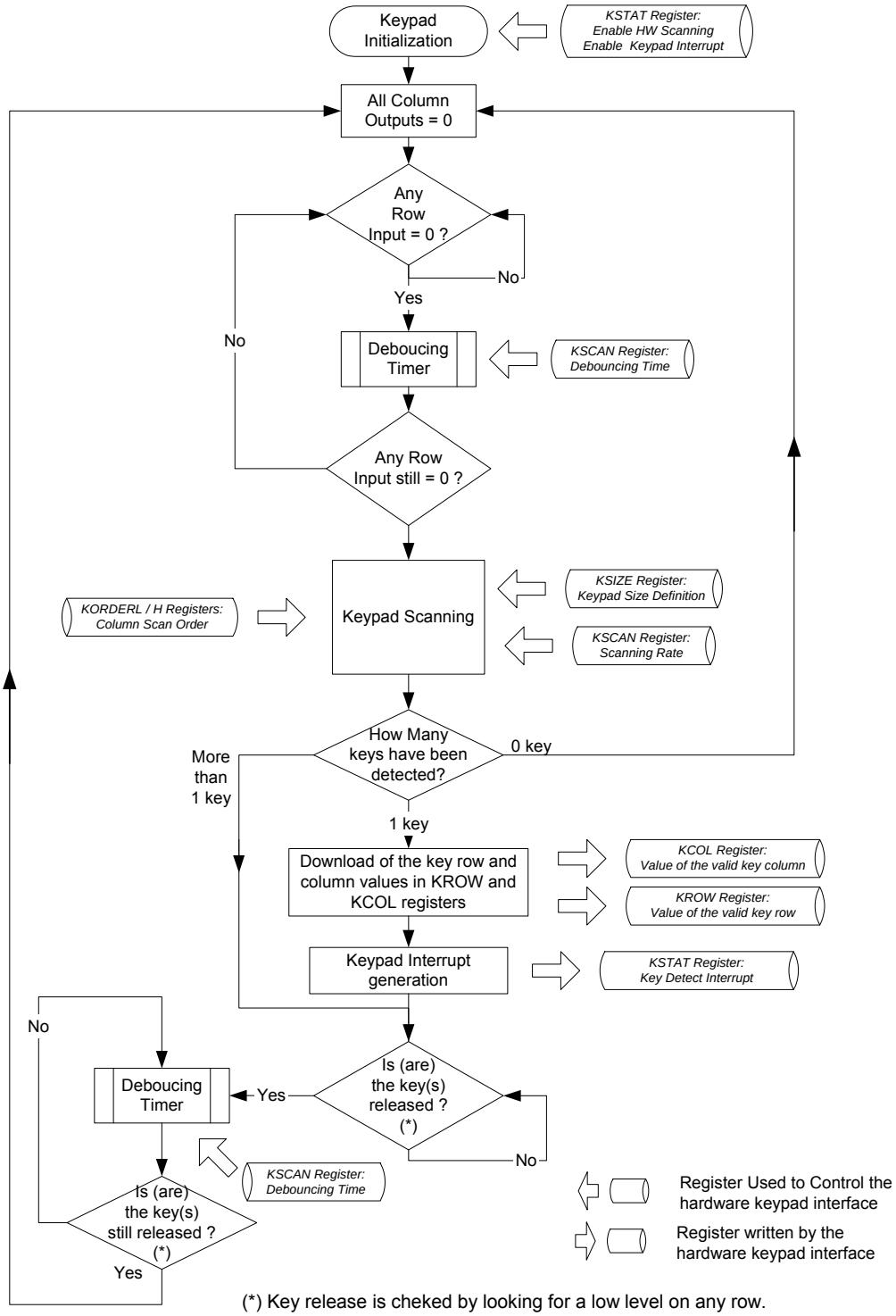


Figure 12: Keypad Interface Flow Chart

SRX Data Register (SRXData): 0xFE09 ← 0x00

Table 82: The SRXData Register

MSB LSB

SRXDAT.7	SRXDAT.6	SRXDAT.5	SRXDAT.4	SRXDAT.3	SRXDAT.2	SRXDAT.1	SRXDAT.0

Bit	Function
SRXData.7	(Read only) Data received from the smart card. Data received from the smart card gets stored in a FIFO that is read by the firmware.
SRXData.6	
SRXData.5	
SRXData.4	
SRXData.3	
SRXData.2	
SRXData.1	
SRXData.0	

Shaded locations indicate functions that are not provided in sync mode.

Table 108: Smart Card SFR Table

Name	Address	b7	b6	b5	b4	b3	b2	b1	b0
SCSel	FE00					SelSC(1:0)		BYPASS	
SCInt	FE01	WAITTO/ RLIEN	CRDEVT	VCCTMR	RXDAVI	TXEVNT	TXSENT	TXERR	RXERR
SCIE	FE02	WTOI/ RLIEN	CDEVNT	VTMREN	RXDAEN	TXEVEN	TXSNTEN	TXERR	RXERR
VccCtl	FE03	VCCSEL.1	VCCSEL.0	VDDFLT	RDYST	VCCOK			SCPWRDN
VccTmr	FE04	OFFTMR(3:0)				VCCTMR(3:0)			
CRDCtl	FE05	DEBOUN	CDETEN			DETPOL	PUENB	PDEN	CARDIN
STXCtl	FE06	SYCKST		TXFULL	TXEMTY	TXUNDR	LASTTX	TX/RXB	BREAKD
STXData	FE07	TXDATA(7:0)							
SRXCtl	FE08	BIT9DAT		LASTRX	CRCERR	RXFULL	RXEMTY	RXOVRR	PARITYE
SRXData	FE09	RXDATA(7:0)							
SCCtl	FE0A	RSTCRD		IO	IOD	C8	C4	CLKLVL	CLKOFF
SCECtl	FE0B			SIO	SIOD			SCLKLVL	SCLKOFF
SCDIR	FE0C					C8D	C4D		
SPrtcol	FE0D	I2CMODE	MOD9/8B	SCESYN	0	TMODE	CRCEN	CRCMS	RCVATR
SCCLK	FE0F			ICLKFS(5:0)					
SCECLK	FE10			ECLKFS(5:0)					
SParCtl	FE11		DISPAR	BRKGEN	BRKDET	RTRAN	DISCRX	INSPE	FORCPE
SByteCtl	FE12		DETTS	DIRTS	BRKDUR (1:0)				
FDReg	FE13	FVAL(3:0)				DVAL (3:0)			
CRCMsB	FE14	CRC(15:8)							
CRCLsB	FE15	CRC(7:0)							
BGT	FE16	EGT8				BGT(4:0)			
EGT	FE17	EGT(7:0)							
BWTB3	FE18					BWT(27:24)			
BWTB2	FE19	BWT(23:16)							
BWTB1	FE1A	BWT(15:8)							
BWTB0	FE1B	BWT(7:0)							
CWTB1	FE1C	CWT(15:8)							
CWTB0	FE1D	CWT(7:0)							
ATRMsB	FE1F	ATRTO(15:8)							
ATRLsB	FE20	ATRTO(7:0)							
STSTO	FE21	TSTO(7:0)							
RLength	FE22	RLen(7:0)							

1.7.14 VDD Fault Detect Function

The 73S1209F contains a circuit to detect a low-voltage condition on the supply voltage V_{DD}. If enabled, it will deactivate the active internal smart card interface when V_{DD} falls below the V_{DD} Fault threshold. The register configures the V_{DD} Fault threshold for the nominal default of 2.3V* or a user selectable threshold. The user's code may load a different value using the FOVRVDDF bit =1 after the power-up cycle has completed

VDDFault Control Register (VDDFCtl): 0xFFD4 ← 0x00

Table 109: The VDDFCtl Register

MSB LSB

–	FOVRVDDF	VDDFLTEN	–	STXDAT.3	VDDFTH.2	VDDFTH.1	VDDFTH.0

Bit	Symbol	Function
VDDFCtl.7	–	
VDDFCtl.6	FOVRVDDF	Setting this bit high will allow the VDDFLT(2:0) bits set in this register to control the VDDFault threshold. When this bit is set low, the VDDFault threshold will be set to the factory default setting of 2.3V*.
VDDFCtl.5	VDDFLTEN	Set = 1 will disable VDD Fault operation.
VDDFCtl.4	–	
VDDFCtl.3	–	
VDDFCtl.2	VDDFTH.2	VDD Fault Threshold. Bit value(2:0) VDDFault voltage 000 2.3 (nominal default) 001 2.4 010 2.5 011 2.6 100 2.7 101 2.8 110 2.9 111 3.0
VDDFCtl.1	VDDFTH.1	
VDDFCtl.0	VDDFTH.0	

* Note: The V_{DD} Fault factory default can be set to any threshold as defined by bits VDDFTH(2:0). The 73S1209F has the capability to burn fuses at the factory to set the factory default to any of these voltages. Contact Teridian for further details.

4.1 Package Pin Designation (68-pin QFN)

CAUTION: Use handling procedures necessary for a static sensitive component

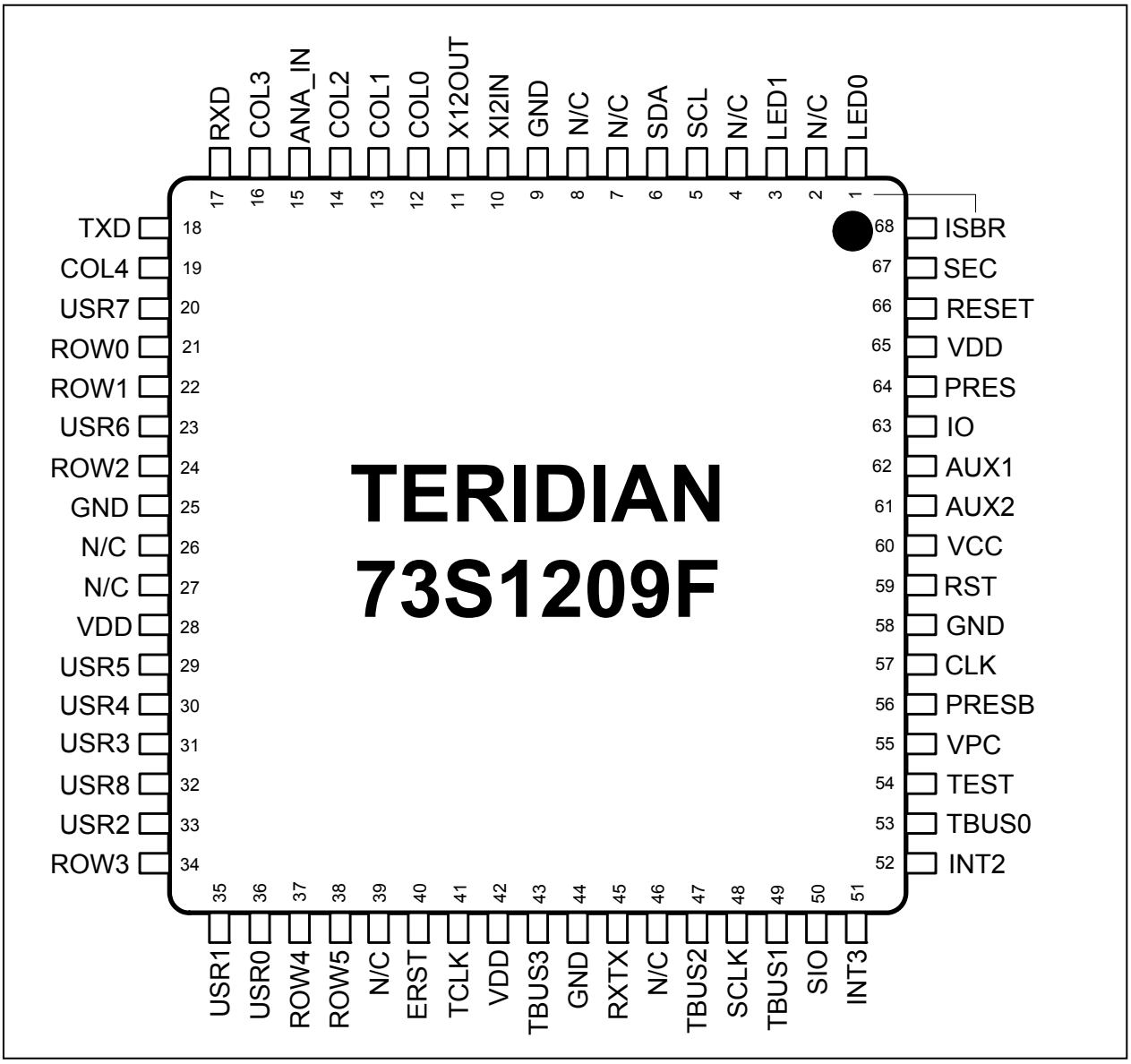


Figure 41: 73S1209F Pinout

5 Ordering Information

Table 110 lists the order numbers and packaging marks used to identify 73S1209F products.

Table 110: Order Numbers and Packaging Marks

Part Description	Order Number	Packaging Mark
73S1209F 68-Pin QFN Lead Free	73S1209F-68IM/F	73S1209F68IM
73S1209F 68-Pin QFN Lead Free, Tape and Reel	73S1209F-68IMR/F	73S1209F68IM
73S1209F 44-Pin QFN Lead Free	73S1209F-44IM/F	73S1209F44IM
73S1209F 44-Pin QFN Lead Free, Tape and Reel	73S1209F-44IMR/F	73S1209F44IM

6 Related Documentation

The following 73S1209F documents are available from Teridian Semiconductor Corporation:

73S1209F Data Sheet (this document)
73S1209F Development Board Quick Start Guide
73S1209F Software Development Kit Quick Start Guide
73S1209F Evaluation Board User's Guide
73S12xxF Software User's Guide
73S12xxF Synchronous Card Design Application Note

7 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73S1209F, contact us at:

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		In Section 1.7.13.5, deleted the Special Operating Mode for Sync and Async Operation table. In Figure 20, Figure 21 and Figure 22, replaced the timing diagrams. In Section 1.7.13.5, added "Synchronous card operation is broken down into three primary types. These are commonly referred to as 2-wire, 3-wire and I2C synchronous cards. Each card type requires different control and timing and therefore requires different algorithms to access. Teridian has created an application note to provide detailed algorithms for each card type. Refer to the application note titled *73S12xxF Synchronous Card Design Application Note*." In the VccCtl.0 bit description, deleted "When in power down mode, V_{DD} = 0V. V_{DD} can only be turned on by pressing the ON/OFF switch or by application of 5V to V_{BUS}. If V_{BUS} power is available and SCPWRDN bit is set, it has no effect until V_{BUS} is removed and V_{DD} will shut off." In Table 79 and Table 108, changed the SYCKST bit to I2CMODE. Changed the register address for ATRMsB from FE21 to FE1F. In Table 108 (SPrtcol register), changed the SCISYN bit to I2CMODE. In Figure 24 and Figure 25, replaced the schematics with new schematics. In Section 3.4, changed the Fxtal Min value from 4 to 6. Added Section 6, Related Documentation. Added Section 7, Contact Information. Formatted the document per new standard. Added section numbering.

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