Analog Devices Inc./Maxim Integrated - 73S1209F-44IMR/F Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80515
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SmartCard, UART/USART
Peripherals	LED, POR, WDT
Number of I/O	9
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/73s1209f-44imr-f

Pin Name	Pin (68 QFN)	Pin (44 QFN)	Type	Equivalent Circuit*	Description
VDD	28 42 65	18 27 44	I		General positive power supply pins. All digital IO is referred to this supply voltage. There is an on-chip regulator that uses VDD to provide power for internal circuits (VPD). A 0.1μF capacitor is recommended at each VDD pin.
N/C	2 4 7 8 26 27 39 46	16 17 29			No connect.
GND	9 25 44	7 15	GND		General ground supply pins for all IO and logic circuits.
RESET	66	1	I	Figure 31	Reset input, positive assertion. Resets logic and registers to default condition.

* See the figures in the Equivalent Circuits section.

1.2 Hardware Overview

The 73S1209F single smart card controller integrates all primary functional blocks required to implement a smart card reader. Included on chip are an 8051-compatible microprocessor (MPU) which executes up to one instruction per clock cycle (80515), a fully integrated IS0-7816 compliant smart card interface, expansion smart card interface, serial interface, I2C interface, 6 x 5 keypad interface, 2 LED drivers, RAM, FLASH memory, and a variety of I/O pins. A functional block diagram of the 73S1209F is shown in Figure 1.

1.3 80515 MPU Core

1.3.1 80515 Overview

The 73S1209F includes an 80515 MPU (8-bit, 8051-compatible) that performs most instructions in one clock cycle. The 80515 architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Normally a machine cycle is aligned with a memory fetch, therefore, most of the 1-byte instructions are performed in a single cycle. This leads to an 8x performance (average) improvement (in terms of MIPS) over the Intel 8051 device running at the same clock frequency.

Actual processor clocking speed can be adjusted to the total processing demand of the application (cryptographic calculations, key management, memory management, and I/O management) using the XRAM special function register MPUCKCtl.

Typical smart card, serial, keyboard and I2C management functions are available for the MPU as part of Teridian's standard library. A standard ANSI "C" 80515-application programming interface library is available to help reduce design cycle. Refer to the *73S12xxF Software User's Guide*.

1.3.2 Memory Organization

The 80515 MPU core incorporates the Harvard architecture with separate code and data spaces. Memory organization in the 80515 is similar to that of the industry standard 8051. There are three memory areas: Program memory (Flash), external data memory (XRAM), and internal data memory (IRAM). Data bus address space is allocated to on-chip memory as shown Table 2

Table 2: MPU Data Memory Map

Address (hex)	Memory Technology	Memory Type	Typical Usage	Memory Size (bytes)
0000-7FFF	Flash Memory	Non-volatile	Program and non-volatile data	32KB
0000-07FF	Static RAM	Volatile	MPU data XRAM	2KB
FC00-FFFF	External SFR	Volatile	Peripheral control	1KB

Note: The IRAM is part of the core and is addressed differently.

Program Memory: The 80515 can address up to 32KB of program memory space from 0x0000 to 0x7FFF. Program memory is read when the MPU fetches instructions or performs a MOVC operation. After reset, the MPU starts program execution from location 0x0000. The lower part of the program memory includes reset and interrupt vectors. The interrupt vectors are spaced at 8-byte intervals, starting from 0x0003. Reset is located at 0x0000.

Flash Memory: The program memory consists of flash memory. The flash memory is intended to primarily contain MPU program code. Flash erasure is initiated by writing a specific data pattern to specific SFR registers in the proper sequence. These special pattern/sequence requirements prevent inadvertent erasure of the flash memory.

1.4 Program Security

Two levels of program and data security are available. Each level requires a specific fuse to be blown in order to enable or set the specific security mode. Mode 0 security is enabled by setting the SECURE bit (bit 6 of SFR register FLSHCTL 0xB2) Mode 0 limits the ICE interface to only allow bulk erase of the flash program memory. All other ICE operations are blocked. This guarantees the security of the user's MPU program code. Security (Mode 0) is enabled by MPU code that sets the SECURE bit. The MPU code must execute the setting of the SECURE bit immediately after a reset to properly enable Mode 0. This should be the first instruction after the reset vector jump has been executed. If the "startup.a51" assembly file is used in an application, then it must be modified to set the SECURE bit after the reset vector jump. If not using "startup.a51", then this should be the first instruction in main(). Once security Mode 0 is enabled, the only way to disable it is to perform a global erase of the flash followed by a full circuit reset. Once the flash has been erased and the reset has been executed, security Mode 0 is disabled and the ICE has full control of the core. The flash can be reprogrammed after the bulk erase operation is completed. Global erase of the flash will also clear the data XRAM memory. The security enable bit (SECURE) is reset whenever the MPU is reset. Hardware associated with the bit only allows it to be set. As a result, the code may set the SECURE bit to enable the security Mode 0 feature but may not reset it. Once the SECURE bit is set, the code is protected and no external read of program code in flash or data (in XRAM) is possible. In order to invoke the security Mode 0, the SECSET0 (bit 1 of XRAM SFR register SECReg 0xFFD7) fuse must be blown beforehand or the security mode 0 will not be enabled. The SECSET0 and SECSET1 fuses once blown, cannot be overridden.

Specifically, when SECURE is set:

- The ICE is limited to bulk flash erase only.
- Page zero of flash memory may not be page-erased by either MPU or ICE. Page zero may only be erased with global flash erase. Note that global flash erase erases XRAM whether the SECURE bit is set or not.
- Writes to page zero, whether by MPU or ICE, are inhibited.

Security mode 1 is in effect when the SECSET1 fuse has been programmed (blown open). In security mode 1, the ICE is completely and permanently disabled. The Flash program memory and the MPU are not available for alteration, observation, or control. As soon as the fuse has been blown, the ICE is disabled. The testing of the SECSET1 fuse will occur during the reset and before the start of pre-boot and boot cycles. This mode is not reversible, nor recoverable. In order to blow the SECSET1 fuse, the SEC pin must be held high for the fuse burning sequence to be executed properly. The firmware can check to see if this pin is held high by reading the SECPIN bit (bit 5 of XRAM SFR register SECReg 0xFFD7). If this bit is set and the firmware desires, it can blow the SECSET1 fuse. The burning of the SECSET0 does not require the SEC pin to be held high.

In order to blow the fuse for SECSET1 and SECSET0, a particular set of register writes in a specific order need to be followed. There are two additional registers that need to have a specific value written to them in order for the desired fuse to be blown. These registers are FUSECtl (0xFFD2) and TRIMPCtl (0xFFD1). The sequence for blowing the fuse is as follows:

1. Write 0x54H to FUSECtl.
2. Write 0x81H for security mode 0 Note: only program one security mode at a time.
   Write 0x82H for security mode 1 Note: SEC pin must be high for security mode 1.
3. Write 0xA6 to TRIMPCtl.
4. Delay about 500 us
5. Write 0x00 to TRIMPCtl.

Table 5: Security Control Registers

Register	SFR Address	R/W	Description
FLSHCTL	0xB2	R/W	Bit 0 (FLSH_PWE): Program Write Enable: 0 – MOVX commands refer to XRAM Space, normal operation (default). 1 – MOVX @DPTR,A moves A to Program Space (Flash) @ DPTR. This bit is automatically reset after each byte written to flash. Writes to this bit are inhibited when interrupts are enabled.
		W	Bit 1 (FLSH_MEEN): Mass Erase Enable: 0 – Mass Erase disabled (default). 1 – Mass Erase enabled. Must be re-written for each new Mass Erase cycle.
		R/W	Bit 6 (SECURE): Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored.
TRIMPCtl	0xFFD1	W	0xA6 value will cause the selected fuse to be blown. All other values will stop the burning process.
FUSECtl	0xFFD2	W	0x54 value will set up for security fuse control. All other values are reserved and should not be used.
SECReg	0xFFD7	W	Bit 7 (PARAMSEC): 0 – Normal operation 1 – Enable permanent programming of the security fuses.
		R	Bit 5 (SECPIN): Indicates the state of the SEC pin. The SEC pin is held low by a pull-down resistor. The user can force this pin high during boot sequence time to indicate to the firmware that sec mode 1 is desired.
		R/W	Bit 1 (SECSET1): See Program Security section.
		R/W	Bit 0 (SECSET0): See Program Security section.

1.5.3 External Data Special Function Registers (SFRs)

A map of the XRAM Special Function Registers is shown in Table 6. . The smart card registers are listed separately in Table 108.

Table 8: XRAM Special Function Registers Reset Values

Name	Location	Reset Value	Description
DAR	0x FF80	0x00	Device Address Register (I^2C)
WDR	0x FF81	0x00	Write Data Register (I^2C)
SWDR	0x FF82	0x00	Secondary Write Data Register (I^2C)
RDR	0x FF83	0x00	Read Data Register (I^2C)
SRDR	0x FF84	0x00	Secondary Read Data Register (I^2C)
CSR	0x FF85	0x00	Control and Status Register (I^2C)
USRIntCtl1	0x FF90	0x00	External Interrupt Control 1
USRIntCtl2	0x FF91	0x00	External Interrupt Control 2
USRIntCtl3	0x FF92	0x00	External Interrupt Control 3
USRIntCtl4	0x FF93	0x00	External Interrupt Control 4
INT5Ctl	0x FF94	0x00	External Interrupt Control 5
INT6Ctl	0x FF95	0x00	External Interrupt Control 6
MPUCKCtl	0x FFA1	0x0C	MPU Clock Control
ACOMP	0x FFD0	0x00	Analog Compare Register
TRIMPCtl	0x FFD1	0x00	TRIM Pulse Control
FUSECtl	0x FFD2	0x00	FUSE Control
VDDFCtl	0x FFD4	0x00	VDDFault Control
SECReg	0x FFD7	0x00	Security Register
MISCtl0	0x FFF1	0x00	Miscellaneous Control Register 0
MISCtl1	0x FFF2	0x10	Miscellaneous Control Register 1
LEDCtl	0x FFF3	0xFF	LED Control Register

Accumulator (ACC, A): ACC is the accumulator register. Most instructions use the accumulator to hold the operand. The mnemonics for accumulator-specific instructions refer to accumulator as “A”, not ACC.

B Register: The B register is used during multiply and divide instructions. It can also be used as a scratch-pad register to hold temporary data.

Timer/Counter Control Register (TCON): 0x88 ← 0x00

Table 22: The TCON Register

MSB							LSB
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Bit	Symbol	Function
TCON.7	TF1	Timer 1 overflow flag.
TCON.6	TR1	Not used for interrupt control.
TCON.5	TF0	Timer 0 overflow flag.
TCON.4	TR0	Not used for interrupt control.
TCON.3	IE1	Interrupt 1 edge flag is set by hardware when the falling edge on external interrupt int1 is observed. Cleared when an interrupt is processed.
TCON.2	IT1	Interrupt 1 type control bit. 1 selects falling edge and 0 selects low level for input pin to cause an interrupt.
TCON.1	IE0	Interrupt 0 edge flag is set by hardware when the falling edge on external interrupt int0 is observed. Cleared when an interrupt is processed.
TCON.0	IT0	Interrupt 0 type control bit. 1 selects falling edge and 0 sets low level for input pin to cause interrupt.

Timer/Interrupt 2 Control Register (T2CON): 0xC8 ← 0x00

Table 23: The T2CON Register

MSB							LSB
–	I3FR	I2FR	–	–	–	–	–

Bit	Symbol	Function
T2CON.7	–	
T2CON.6	I3FR	External interrupt 3 failing/rising edge flag. I3FR = 0 external interrupt 3 negative transition active. I3FR = 1 external interrupt 3 positive transition active.
T2CON.5	I2FR	External interrupt 3 failing/rising edge flag. I2FR = 0 external interrupt 3 negative transition active. I2FR = 1 external interrupt 3 positive transition active.
T2CON.4	–	
T2CON.3	–	
T2CON.2	–	
T2CON.1	–	
T2CON.0	–	

Power Control Register 0 (PCON): 0x87 ← 0x00

The SMOD bit used for the baud rate generator is set up via this register.

Table 35: The PCON Register

MSB LSB

SMOD	–	–	–	GF1	GF0	STOP	IDLE

Bit	Symbol	Function
PCON.7	SMOD	If SM0D = 1, the baud rate is doubled.
PCON.6	–	
PCON.5	–	
PCON.4	–	
PCON.3	GF1	General purpose flag 1.
PCON.2	GF0	General purpose flag 1.
PCON.1	STOP	Sets CPU to Stop mode.
PCON.0	IDLE	Sets CPU to Idle mode.

Baud Rate Control Register 0 (BRCON): 0xD8 ← 0x00

The BSEL bit used to enable the baud rate generator is set up via this register.

Table 36: The BRCON Register

MSB LSB

BSEL	–	–	–	–	–	–	–

Bit	Symbol	Function
BRCON.7	BSEL	If BSEL = 0, the baud rate is derived using timer 1. If BSEL = 1 the baud rate generator circuit is used.
BRCON.6	–	
BRCON.5	–	.
BRCON.4	–	
BRCON.3	–	
BRCON.2	–	
BRCON.1	–	
BRCON.0	–	

1.7.5 Timers and Counters

The 80515 has two 16-bit timer/counter registers: Timer 0 and Timer 1. These registers can be configured for counter or timer operations.

In timer mode, the register is incremented every machine cycle, meaning that it counts up after every 12 periods of the MPU clock signal.

In counter mode, the register is incremented when the falling edge is observed at the corresponding input signal T0 or T1 (T0 and T1 are the timer gating inputs derived from USR[0:7] pins, see the User (USR) Ports section). Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle.

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function Registers (TMOD and TCON) are used to select the appropriate mode.

The Timer 0 load registers are designated as TL0 and TH0 and the Timer 1 load registers are designated as TL1 and TH1.

Timer/Counter Mode Control Register (TMOD): 0x89 ← 0x00

Table 40: The TMOD Register

MSB LSB

GATE	C/T	M1	M0	GATE	C/T	M1	M0
Timer 1				**Timer 0**			

Bits TR1 and TR0 in the TCON register start their associated timers when set.

Table 41: TMOD Register Bit Description

Bit	Symbol	Function
TMOD.7 TMOD.3	Gate	If set, enables external gate control (USR pin(s) connected to T0 or T1 for Counter 0 or 1, respectively). When T0 or T1 is high, and TRx bit is set (see the TCON register), a counter is incremented every falling edge on T0 or T1 input pin. If not set, the TRx bit controls the corresponding timer.
TMOD.6 TMOD.2	C/T	Selects Timer or Counter operation. When set to 1, the counter operation is performed based on the falling edge of T0 or T1. When cleared to 0, the corresponding register will function as a timer.
TMOD.5 TMOD.1	M1	Selects the mode for Timer/Counter 0 or Timer/Counter 1, as shown in the TMOD description.
TMOD.4 TMOD.0	M0	Selects the mode for Timer/Counter 0 or Timer/Counter 1, as shown in the TMOD description.

Timer/Counter Control Register (TCON): 0x88 ← 0x00

Table 43: The TCON Register

MSB LSB

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Bit	Symbol	Function
TCON.7	TF1	The Timer 1 overflow flag is set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when an interrupt is processed.
TCON.6	TR1	Timer 1 Run control bit. If cleared, Timer 1 stops.
TCON.5	TF0	Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when an interrupt is processed.
TCON.4	TR0	Timer 0 Run control bit. If cleared, Timer 0 stops.
TCON.3	IE1	External Interrupt 1 edge flag.
TCON.2	IT1	External interrupt 1 type control bit.
TCON.1	IE0	External Interrupt 0 edge flag.
TCON.0	IT0	External Interrupt 0 type control bit.

1.7.6 WD Timer (Software Watchdog Timer)

The software watchdog timer is a 16-bit counter that is incremented once every 24 or 384 clock cycles. After a reset, the watchdog timer is disabled and all registers are set to zero. The watchdog consists of a 16-bit counter (WDT), a reload register (WDTREL), prescalers (by 2 and by 16), and control logic. Once the watchdog starts, it cannot be stopped unless the internal reset signal becomes active.

WD Timer Start Procedure: The WDT is started by setting the SWDT flag. When the WDT register enters the state 0x7CFF, an asynchronous WDTS signal will become active. The signal WDTS sets bit 6 in the IP0 register and requests a reset state. WDTS is cleared either by the reset signal or by changing the state of the WDT timer.

Refreshing the WD Timer: The watchdog timer must be refreshed regularly to prevent the reset request signal from becoming active. This requirement imposes an obligation on the programmer to issue two instructions. The first instruction sets WDT and the second instruction sets SWDT. The maximum delay allowed between setting WDT and SWDT is 12 clock cycles. If this period has expired and SWDT has not been set, WDT is automatically reset, otherwise the watchdog timer is reloaded with the content of the WDTREL register and WDT is automatically reset.

1.7.7 User (USR) Ports

The 73S1209F includes 9 pins of general purpose digital I/O (GPIO). On reset or power-up, all USR pins are inputs until they are configured for the desired direction. The pins are configured and controlled by the USR and UDIR SFRs. Each pin declared as USR can be configured independently as an input or output with the bits of the UDIRn registers. Table 48 lists the direction registers and configurability associated with each group of USR pins. USR pins 0 to 7 are multiple use pins that can be used for general purpose I/O, external interrupts and timer control.

Table 49 shows the configuration for a USR pin through its associated bit in its UDIR register. Values read from and written into the GPIO ports use the data registers USR70 and USR8. Note: After reset, all USR pins are defaulted as inputs and pulled up to VDD until any write to the corresponding UDIR register is performed. This insures all USR pins are set to a known value until set by the firmware. Unused USR pins can be set for output if unused and unconnected to prevent them from floating. Alternatively, unused USR pins can be set for input and tied to ground or V_{DD}.

Table 48: Direction Registers and Internal Resources for DIO Pin Groups

USR Pin Group	Type	Direction Register Name	Direction Register (SFR) Location	Data Register Name	Data Register (SFR) Location
USR_0…USR_7	Multi-use	UDIR70	0x91 [7:0]	USR70	0x90 [7:0]
USR_8	GPIO only	UDIR8	0xA1 [0]	USR8	0xA0 [0]

Table 49: UDIR Control Bit

	UDIR Bit	
	0	1
USR Pin Function	output	input

Four XRAM SFR registers (USRIntCtl1, USRIntCtl2, USRIntCtl3, and USRIntCtl4) control the use of the USR [7:0] pins. Each of the USR [7:0] pins can be configured as GPIO or individually be assigned an internal resource such as an interrupt or a timer/counter control. Each of the four registers contains two 3-bit configuration words named UxIS (where x corresponds to the USR pin). The control resources selectable for the USR pins are listed in Table 74 through Table 78. If more than one input is connected to the same resource, the resources are combined using a logical OR.

Table 50: Selectable Controls Using the UxIS Bits

UxIS Value	Resource Selected for USRx Pin
0	None
1	None
2	T0 (counter0 gate/clock)
3	T1 (counter1 gate/clock)
4	Interrupt 0 rising edge/high level on USRx
5	Interrupt 1 rising edge/high level on USRx
6	Interrupt 0 falling edge/low level on USRx
7	Interrupt 1 falling edge/low level on USRx

Note: x denotes the corresponding USR pin. Interrupt edge or level control is assigned in the IT0 and IT1 bits in the TCON register.

1.7.8 Analog Voltage Comparator

The 73S1209F includes a programmable comparator that is connected to the ANA_IN pin. The comparator can be configured to trigger an interrupt if the input voltage rises above or falls below a selectable threshold voltage. The comparator control register should not be modified when the analog interrupt (ANAIEN bit in the INT6Ctl register) is enabled to guard against any false interrupt that might be generated when modifying the threshold. The comparator has a built-in hysteresis to prevent the comparator from repeatedly responding to low-amplitude noise. This hysteresis is approximately 20mV. Interrupt control is handled in the INT6Ctl register.

Analog Compare Control Register (ACOMP): 0xFFD0 ← 0x00

Table 55: The ACOMP Register

MSB LSB

ANALVL	–	ONCHG	CPOL	CMPEN	TSEL.2	TSEL.1	TSEL.0

Bit	Symbol	Function
ACOMP.7	ANALVL	When read, indicates whether the input level is above or below the threshold. This is a real time value and is not latched, so it may change from the time of the interrupt trigger until read.
ACOMP.6	-	
ACOMP.5	ONCHG	If set, the Ana_interrupt is invoked on any change above or below the threshold, bit 4 is ignored.
ACOMP.4	CPOL	If set = 1, Ana_interrupt is invoked when signal rises above selected threshold. If set = 0, Ana_interrupt is invoked when signal goes below selected threshold (default).
ACOMP.3	CMPEN	Enables power to the analog comparator. 1= Enabled. 0 = Disabled (default).
ACOMP.2	TSEL.2	Sets the voltage threshold for comparison to the voltage on pin ANA_IN. Thresholds are as follows: TSEL.2 TSEL.1 TSEL.0 Voltage Threshold 0 0 0 1.00V 0 0 1 1.24V 0 1 0 1.40V 0 1 1 1.50V 1 0 0 1.75V 1 0 1 2.00V 1 1 0 2.30V 1 1 1 2.50V
ACOMP.1	TSEL.1	
ACOMP.0	TSEL.0	

Device Address Register (DAR): 0xFF80 ← 0x00

Table 58: The DAR Register

MSB							LSB
DVADR.6	DVADR.5	DVADR.4	DVADR.3	DVADR.2	DVADR.1	DVADR.0	I2CRW

Bit	Symbol	Function
DAR.7	DVADR [0:6]	Slave device address.
DAR.6		
DAR.5		
DAR.4		
DAR.3		
DAR.2		
DAR.1		
DAR.0	I2CRW	If set = 0, the transaction is a write operation. If set = 1, read.

I2C Write Data Register (WDR): 0XFF81 ← 0x00

Table 59: The WDR Register

MSB							LSB
WDR.7	WDR.6	WDR.5	WDR.4	WDR.3	WDR.2	WDR.1	WDR.0

Bit	Function
WDR.7	Data to be written to the I^2C slave device.
WDR.6	
WDR.5	
WDR.4	
WDR.3	
WDR.2	
WDR.1	
WDR.0	

1.7.11 Keypad Interface

The 73S1209F supports a 30-button (6 row x 5 column) keypad (SPST Mechanical Contact Switches) interface using 11 dedicated I/O pins. Figure 11 shows a simplified block diagram of the keypad interface.

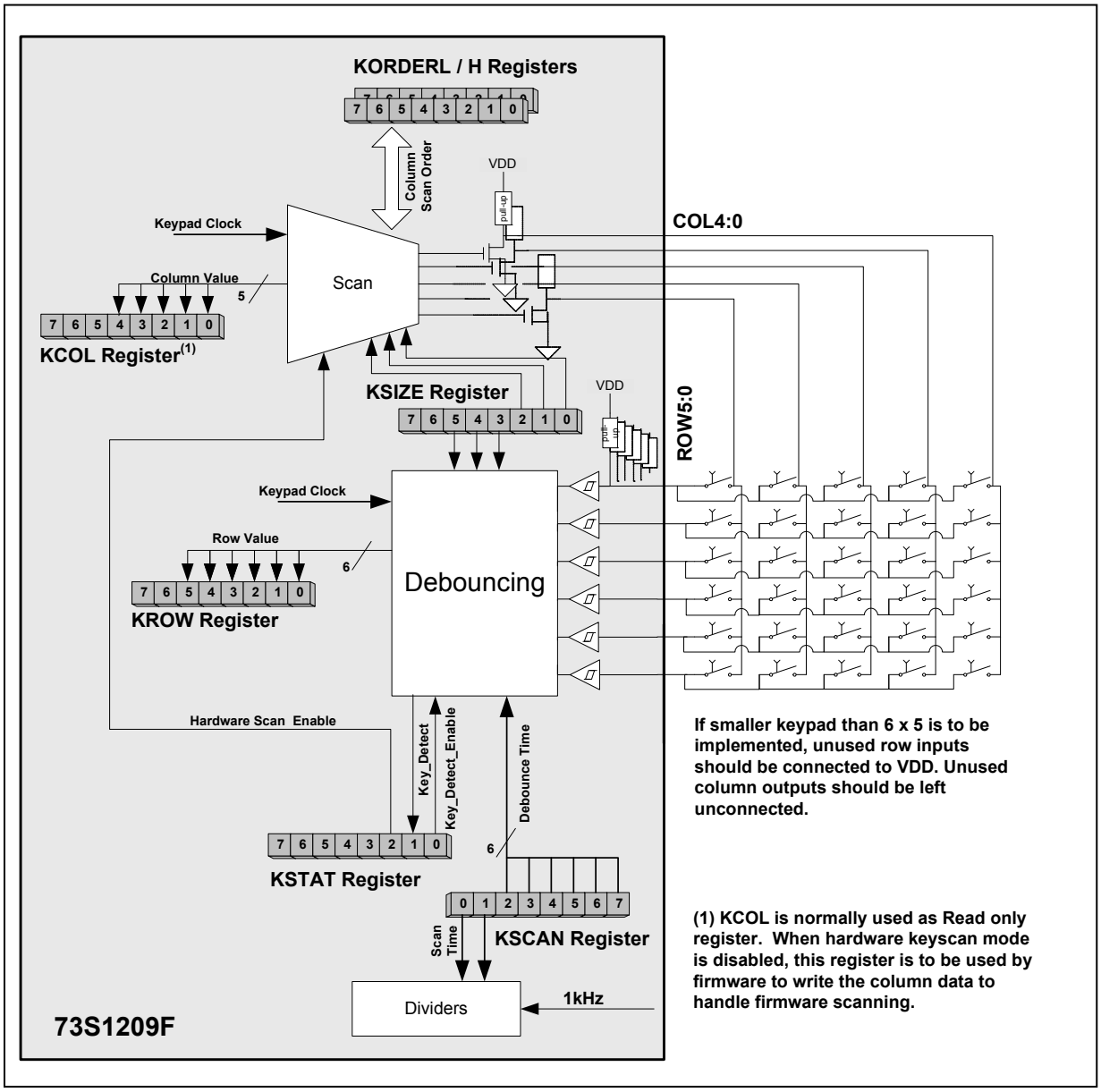

Figure 11: Simplified Keypad Block Diagram

There are 5 drive lines (outputs) corresponding to columns and 6 sense lines (inputs) corresponding to rows. Hysteresis and pull-ups are provided on all inputs (rows), which eliminate the need for external resistors in the keypad. Key scanning happens by asserting one of the 5 column lines low and looking for a low on a sense line indicating that a key is pressed (switch closed) at the intersection of the drive/sense (col/row) line in the keypad. Key detection is performed by hardware with an incorporated debounce timer. Debouncing time is adjustable through the KSCAN Register. Internal hardware circuitry performs column scanning at an adjustable scanning rate and column scanning order through registers KSCAN and KORDERL / KORDERH. Key scanning is disabled at reset and must be enabled by firmware. When a valid key is detected, an interrupt is generated and the valid value of the pressed key is automatically

written into KCOL and KROW registers. The keypad interface uses a 1kHz clock derived from the 12MHz crystal. The clock is enabled by setting bit 6 – KBEN – in the MCLKCtl register (see the Oscillator and Clock Generation section) to carry out scanning and debouncing. The keypad size can be adjusted within the KSIZE register.

Normal scanning is performed by hardware when the SCNEN bit is set to 1 in the KSTAT register. Figure 12 shows the flowchart of how the hardware scanning operates. In order to minimize power, scanning does not occur until a key-press is detected. Once hardware key scanning is enabled, the hardware drives all column outputs low and waits for a low to be detected on one of the inputs. When a low is detected on any row, and before key scanning starts, the hardware checks that the low level is still detected after a debounce time. The debounce time is defined by firmware in the KSCAN register (bits 7:0, DBTIME). Debounce times from 4ms to 256ms in 4ms increments are supported. If a key is not pressed after the debounce time, the hardware will go back to looking for any input to be low. If a key is confirmed to be pressed, key scanning begins.

Key scanning asserts one of the 5 drive lines (COL 4:0) low and looks for a low on a sense line indicating that a key is pressed at the intersection of the drive/sense line in the keypad. After all sense lines have been checked without a key-press being detected, the next column line is asserted. The time between checking each sense line is the scan time and is defined by firmware in the KSCAN register (bits 0:1 – SCTIME). Scan times from 1ms to 4ms are supported. Scanning order does not affect the scan time. This scanning continues until the entire keypad is scanned. If only one key is pressed, a valid key is detected. Simultaneous key presses are not considered as valid (If two keys are pressed, no key is reported to firmware).

Possible scrambling of the column scan order is provided by means of KORDERL and KORDERH registers that define the order of column scanning. Values in these registers must be updated every time a new keyboard scan order is desired. It is not possible to change the order of scanning the sense lines. The column and row intersection for the detected valid key are stored in the KCOL and KROW registers. When a valid key is detected, an interrupt is generated. Firmware can then read those registers to determine which key had been pressed. After reading the KCOL and KROW registers, the firmware can update the KORDERL / KORDERH registers if a new scan order is needed.

When the SCNEN bit is enabled in the KSTAT register, the KCOL and KROW registers are only updated after a valid key has been identified. The hardware does not wait for the firmware to service the interrupt in order to proceed with the key scanning process. Once the valid key (or invalid key – e.g. two keys pressed) is detected, the hardware waits for the key to be released. Once the key is released, the debounce timer is started. If the key is not still released after the debounce time, the debounce counter starts again. After a key release, all columns will be driven low as before and the process will repeat waiting for any key to be pressed.

When the SCNEN bit is disabled, all drive outputs are set to the value in the KCOL register. If firmware clears the SCNEN bit in the middle of a key scan, the KCOL register contains the last value stored in there which will then be reflected on the output pins.

A bypass mode is provided so that the firmware can do the key scanning manually (SCNEN bit must be cleared). In bypass mode, the firmware writes/reads the Column and Row registers to perform the key scanning.

Keypad Scan Time Register (KSCAN): 0xD3 ← 0x00

This register contains the values of scanning time and debouncing time.

Table 67: The KSCAN Register

MSB							LSB
DBTIME.5	DBTIME.4	DBTIME.3	DBTIME.2	DBTIME.1	DBTIME.0	SCTIME.1	SCTIME.0

Bit	Symbol	Function
KSCAN.7	DBTIME.5	De-bounce time in 4ms increments. 1 = 4ms de-bounce time, 0x3F = 252ms, 0x00 = 256ms. Key presses and key releases are de-bounced by this amount of time.
KSCAN.6	DBTIME.4	
KSCAN.5	DBTIME.3	
KSCAN.4	DBTIME.2	
KSCAN.3	DBTIME.1	
KSCAN.2	DBTIME.0	
KSCAN.1	SCTIME.1	Scan time in ms. 01 = 1ms, 02 = 2ms, 00 = 3ms, 00 = 4ms. Time between checking each key during keypad scanning.
KSCAN.0	SCTIME.0	

Keypad Control/Status Register (KSTAT): 0xD4 ← 0x00

This register is used to control the hardware keypad scanning and detection capabilities, as well as the keypad interrupt control and status.

Table 68: The KSTAT Register

MSB							LSB
–	–	–	–	KEYCLK	HWSCEN	KEYDET	KYDTEN

Bit	Symbol	Function
KSTAT.7	–	
KSTAT.6	–	
KSTAT.5	–	
KSTAT.4	–	
KSTAT.3	KEYCLK	The current state of the keyboard clock can be read from this bit.
KSTAT.2	HWSCEN	Hardware Scan Enable – When set, the hardware will perform automatic key scanning. When cleared, the firmware must perform the key scanning manually (bypass mode).
KSTAT.1	KEYDET	Key Detect – When HWSCEN = 1 this bit is set causing an interrupt that indicates a valid key press was detected and the key location can be read from the Keypad Column and Row registers. When HWSCEN = 0, this bit is an interrupt which indicates a falling edge on any Row input if all Row inputs had been high previously (note: multiple Key Detect interrupts may occur in this case due to the keypad switch bouncing). In all cases, this bit is cleared when read. When HWSCEN = 0 and the keypad interface 1kHz clock is disabled, a key press will still set this bit and cause an interrupt.
KSTAT.0	KYDTEN	Key Detect Enable – When set, the KEYDET bit can cause an interrupt and when cleared the KEYDET cannot cause an interrupt. KEYDET can still get set even if the interrupt is not enabled.

Keypad Column MS Scan Order Register (KORDERH): 0xD7 ← 0x00

Table 71: The KORDERH Register

MSB							LSB
–	5COL.2	5COL.1	5COL.0	4COL.2	4COL.1	4COL.0	3COL.2

Bit	Symbol	Function
KORDERH.7	–	
KORDERH.6	5COL.2	Column to scan 5th.
KORDERH.5	5COL.1	
KORDERH.4	5COL.0	
KORDERH.3	4COL.2	Column to scan 4th.
KORDERH.2	4COL.1	
KORDERH.1	4COL.0	
KORDERH.0	3COL.2	Column to scan 3rd (msb).

External Interrupt Control Register (INT5Ctl): 0xFF94 ← 0x00

Table 72: The INT5Ctl Register

MSB							LSB
PDMUX	–	RTCIEN	RTCINT	USBIEN	USBINT	KPIEN	KPINT

Bit	Symbol	Function
INT5Ctl.7	PDMUX	Power down multiplexer control.
INT5Ctl.6	–	
INT5Ctl.5	RTCIEN	When set =1, enables RTC interrupt.
INT5Ctl.4	RTCINT	When set =1, indicates interrupt from Real Time Clock function. Cleared on read of register.
INT5Ctl.3	USBIEN	USB interrupt enable.
INT5Ctl.2	USBINT	USB interrupt flag.
INT5Ctl.1	KPIEN	Enables Keypad interrupt when set = 1.
INT5Ctl.0	KPINT	This bit indicates the Keypad logic has set Key_Detect bit and a key location may be read. Cleared on read of register.

1.7.12 Emulator Port

The emulator port, consisting of the pins E_RST, E_TCLK and E_RXTX, provides control of the MPU through an external in-circuit emulator. The E_TBUS[3:0] pins, together with the E_ISYNC/BRKRQ, add trace capability to the emulator. The emulator port is compatible with the ADM51 emulators manufactured by Signum Systems.

If code trace capability is needed on this interface, 20pF capacitors (to ground) need to be added to allow the trace function capability to run properly. These capacitors should be attached to the TBUS0:3 and ISBR signals.

STX Data Register (STXData): 0xFE07 ← 0x00

Table 80: The STXData Register

MSB							LSB
STXDAT.7	STXDAT.6	STXDAT.5	STXDAT.4	STXDAT.3	STXDAT.2	STXDAT.1	STXDAT.0

Bit	Function
STXData.7	Data to be transmitted to smart card. Gets stored in the TX FIFO and then extracted by the hardware and sent to the selected smart card. When the MPU reads this register, the byte pointer is changed to effectively "read out" the data. Thus, two reads will always result in an "empty" FIFO condition. The contents of the FIFO registers are not cleared, but will be overwritten by writes.
STXData.6	
STXData.5	
STXData.4	
STXData.3	
STXData.2	
STXData.1	
STXData.0	

SRX Control/Status Register (SRXCtl): 0xFE08 ← 0x00

This register is used to monitor reception of data from the smart card.

Table 81: The SRXCtl Register

MSB							LSB
BIT9DAT	–	LASTRX	CRCERR	RXFULL	RXEMTY	RXOVRR	PARITYE

Bit	Symbol	Function
SRXCtl.7	BIT9DAT	Bit 9 Data – When in sync mode and with MODE9/8B set, this bit will contain the data on IO (or SIO) pin that was sampled on the ninth CLK (or SCLK) rising edge. This is used to read data in synchronous 9-bit formats.
SRXCtl.6	–	
SRXCtl.5	LASTRX	Last RX Byte – User sets this bit during the reception of the last byte. When byte is received and this bit is set, logic checks CRC to match 0x1D0F (T=1 mode) or LRC to match 00h (T=1 mode), otherwise a CRC or LRC error is asserted.
SRXCtl.4	CRCERR	(Read only) 1 = CRC (or LRC) error has been detected.
SRXCtl.3	RXFULL	(Read only) RX FIFO is full. Status bit to indicate RX FIFO is full.
SRXCtl.2	RXEMTY	(Read only) RX FIFO is empty. This is only a status bit and does not generate a RX interrupt.
SRXCtl.1	RXOVRR	RX Overrun – (Read Only) Asserted when a receive-over-run condition has occurred. An over-run is defined as a byte was received from the smart card when the RX FIFO was full. Invalid data may be in the receive FIFO. Firmware should take appropriate action. Cleared when read. Additional writes to the RX FIFO are discarded when a RXOVRR occurs until the overrun condition is cleared. Will generate RXERR interrupt.
SRXCtl.0	PARITYE	Parity Error – (Read only) 1 = The logic detected a parity error on incoming data from the smart card. Cleared when read. Will generate RXERR interrupt.

4.2 Package Pin Designation (44-pin QFN)

CAUTION: Use handling procedures necessary for a static sensitive component

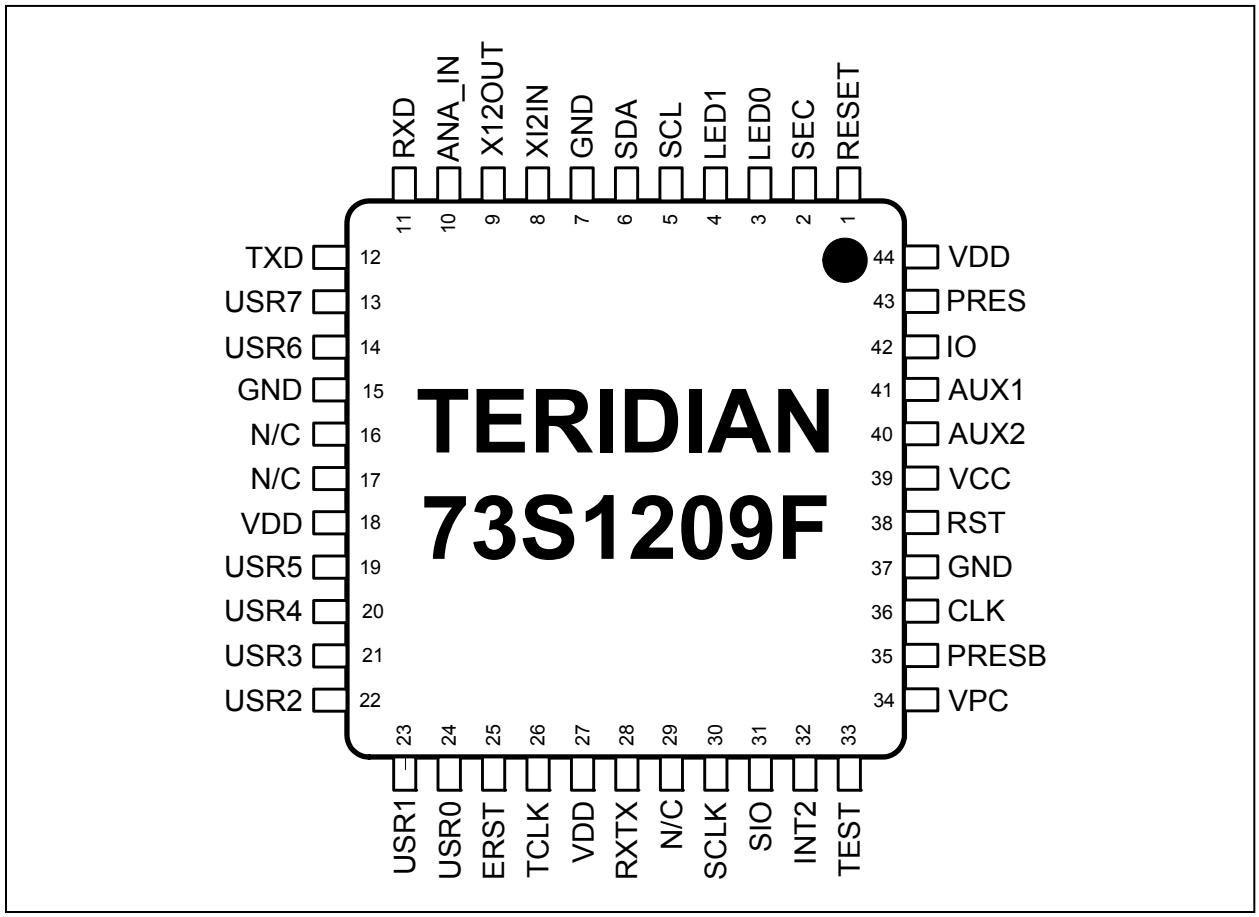

Figure 42: 73S1209F Pinout

5 Ordering Information

Table 110 lists the order numbers and packaging marks used to identify 73S1209F products.

Table 110: Order Numbers and Packaging Marks

Part Description	Order Number	Packaging Mark
73S1209F 68-Pin QFN Lead Free	73S1209F-68IM/F	73S1209F68IM
73S1209F 68-Pin QFN Lead Free, Tape and Reel	73S1209F-68IMR/F	73S1209F68IM
73S1209F 44-Pin QFN Lead Free	73S1209F-44IM/F	73S1209F44IM
73S1209F 44-Pin QFN Lead Free, Tape and Reel	73S1209F-44IMR/F	73S1209F44IM

6 Related Documentation

The following 73S1209F documents are available from Teridian Semiconductor Corporation:

73S1209F Data Sheet (this document)
73S1209F Development Board Quick Start Guide
73S1209F Software Development Kit Quick Start Guide
73S1209F Evaluation Board User's Guide
73S12xxF Software User's Guide
73S12xxF Synchronous Card Design Application Note

7 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73S1209F, contact us at:

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For a complete list of worldwide sales offices, go to http://www.teridian.com.