Analog Devices Inc./Maxim Integrated - 73S1209F-44MR/F/PD Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80515
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SmartCard, UART/USART
Peripherals	LED, POR, WDT
Number of I/O	9
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/73s1209f-44mr-f-pd

Pin Name	Pin (68 QFN)	Pin (44 QFN)	Type	Equivalent Circuit*	Description
INT2	52	32	I	Figure 31	General purpose interrupt input.
SIO	50	31	IO	Figure 27	IO data signal for use with external Smart Card interface circuit such as 73S8010.
SCLK	48	30	O	Figure 28	Clock signal for use with external Smart Card interface circuit.
PRES	64	43	I	Figure 39	Smart Card presence. Active high. Note: the pin has a very weak pull down resistor. In noisy environments, an external pull down may be desired to insure against a false card event.
PRESB	56	35	I	Figure 40	Smart Card presence. Active low. Note: the pin has a very weak pull up resistor. In noisy environments, an external pull up may be desired to insure against a false card event.
CLK	57	36	O	Figure 37	Smart card clock signal.
RST	59	38	O	Figure 37	Smart card Reset signal.
IO	63	42	IO	Figure 38	Smart card Data IO signal.
AUX1	62	41	IO	Figure 38	Auxiliary Smart Card IO signal (C4).
AUX2	61	40	IO	Figure 38	Auxiliary Smart Card IO signal (C8).
VCC	60	39	PSO		Smart Card VCC supply voltage output. A 0.47µF capacitor is required and should be located at the smart card connector. The capacitor should be a ceramic type with low ESR.
GND	58	37	GND		Smart Card Ground.
VPC	55	34	PSI		Smart Card LDO regulator power supply source. A 10µF and a 0.1µF capacitor are required at the VPC input. The 10µF capacitor should be a ceramic type with low ESR.
TBUS(3:0) 0 1 2 3	 53 49 47 43		IO		Trace bus signals for ICE.
RXTX	45	28	IO		ICE control.
ERST	40	25	IO		ICE control.
ISBR	68		IO		ICE control.
TCLK	41	26	I		ICE control.
ANA_IN	15	10	AI	Figure 36	Analog input pin. This signal goes to a programmable comparator and is used to sense the value of an external voltage.
SEC	67	2	I	Figure 35	Input pin for use in programming security fuse. It should be connected to ground when not in use.
TEST	54	33	DI	Figure 35	Test pin, should be connected to ground.

Table 3: Flash Special Function Registers

Register	SFR Address	R/W	Description
ERASE	0x94	W	This register is used to initiate either the Flash Mass Erase cycle or the Flash Page Erase cycle. Specific patterns are expected for ERASE in order to initiate the appropriate Erase cycle (default = 0x00). 0x55 – Initiate Flash Page Erase cycle. Must be proceeded by a write to PGADDR @ SFR 0xB7. 0xAA – Initiate Flash Mass Erase cycle. Must be proceeded by a write to FLSH_MEEN @ SFR 0xB2 and the debug port must be enabled. Any other pattern written to ERASE will have no effect.
PGADDR	0xB7	R/W	Flash Page Erase Address register containing the flash memory page address (page 0 through 127) that will be erased during the Page Erase cycle (default = 0x00). Note: the page address is shifted left by one bit (see detailed description above). Must be re-written for each new Page Erase cycle.
FLSHCTL	0xB2	R/W	Bit 0 (FLSH_PWE): Program Write Enable: 0 – MOVX commands refer to XRAM Space, normal operation (default). 1 – MOVX @DPTR,A moves A to Program Space (Flash) @ DPTR. This bit is automatically reset after each byte written to flash. Writes to this bit are inhibited when interrupts are enabled.
		W	Bit 1 (FLSH_MEEN): Mass Erase Enable: 0 – Mass Erase disabled (default). 1 – Mass Erase enabled. Must be re-written for each new Mass Erase cycle.
		R/W	Bit 6 (SECURE): Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored.

External Interrupt Control Register (INT5Ctl): 0xFF94 ← 0x00

Table 14: The INT5Ctl Register

MSB							LSB
PDMUX	–	–	–	–	–	KPIEN	KPINT

Bit	Symbol	Function
INT5Ctl.7	PDMUX	When set=1, enables interrupts from Keypad (normally going to int5), Smart Card interrupts (normally going to int4), or USR(7:0) pins (int0) to cause interrupt on int0. The assertion of the interrupt to int0 is delayed by 512 MPU clocks to allow the analog circuits, including the clock system, to stabilize. This bit must be set prior to asserting the PWRDN bit in order to properly configure the interrupts that will wake up the circuit. This bit is reset=0 when this register is read.
INT5Ctl.6	–	
INT5Ctl.5	–	
INT5Ctl.4	–	
INT5Ctl.3	–	
INT5Ctl.2	–	
INT5Ctl.1	KPIEN	Keypad interrupt enable.
INT5Ctl.0	KPINT	Keypad interrupt flag.

Miscellaneous Control Register 0 (MISCtl0): 0xFFF1 ← 0x00

Table 15: The MISCtl0 Register

MSB							LSB
PWRDN	–	–	–	–	–	SLPBK	SSEL

Bit	Symbol	Function
MISCtl0.7	PWRDN	This bit sets the circuit into a low-power condition. All analog (high speed oscillator and VCO/PLL) functions are disabled 32 MPU clock cycles after this bit is set=1. This allows time for the next instruction to set the STOP bit in the PCON register to stop the CPU core. The MPU is not operative in this mode. When set, this bit overrides the individual control bits that otherwise control power consumption.
MISCtl0.6	–	
MISCtl0.5	–	
MISCtl0.4	–	
MISCtl0.3	–	
MISCtl0.2	–	
MISCtl0.1	SLPBK	UART loop back testing mode.
MISCtl0.0	SSEL	Serial port pins select.

Miscellaneous Control Register 1 (MISCtl1): 0xFFF2 ← 0x10

Table 16: The MISCtl1 Register

MSB							LSB
–	–	FRPEN	FLSH66	–	–	–	–

Bit	Symbol	Function
MISCtl1.7	–	
MISCtl1.6	–	
MISCtl1.5	FRPEN	Flash Read Pulse enable (low). If FRPEN=1, the Flash Read signal is passed through with no change. When FRPEN=0, a one-shot circuit that shortens the Flash Read signal is enabled to save power. The Flash Read pulse will shorten to 40 or 66ns (approximate based on the setting of the FLSH66 bit) in duration, regardless of the MPU clock rate. For MPU clock frequencies greater than 10MHz, this bit should be set high.
MISCtl1.4	FLSH66	When high, creates a 66ns Flash read pulse, otherwise creates a 40ns read pulse when FRPEN is set.
MISCtl1.3	–	
MISCtl1.2	–	
MISCtl1.1	–	
MISCtl1.0	–	

Master Clock Control Register (MCLKCtl): 0x8F ← 0x0A

Table 17: The MCLKCtl Register

MSB							LSB
HSOEN	KBEN	SCEN	–	–	MCT.2	MCT.1	MCT.0

Bit	Symbol	Function
MCLKCtl.7	HSOEN*	High-speed oscillator enable. When set = 1, disables the high-speed crystal oscillator and VCO/PLL system. This bit is not changed when the PWRDN bit is set but the oscillator/VCO/PLL is disabled.
MCLKCtl.6	KBEN	1 = Disable the keypad logic clock. This bit is not changed in PWRDN mode but the function is disabled.
MCLKCtl.5	SCEN	1 = Disable the smart card logic clock. This bit is not changed in PWRDN mode but the function is disabled. Interrupt logic for card insertion/removal remains operable even with smart card clock disabled.
MCLKCtl.4	–	
MCLKCtl.3	–	
MCLKCtl.2	MCT.2	This value determines the ratio of the VCO frequency (MCLK) to the high-speed crystal oscillator frequency such that: MCLK=(MCount*2 + 4)*Fxtal. The default value is MCount= 2h such that MCLK = (2*2 + 4)*12.00MHz = 96MHz.
MCLKCtl.1	MCT.1	
MCLKCtl.0	MCT.0	

*Note: The HSOEN bit should never be set under normal circumstances. Power down control should only be initiated via use of the PWRDN bit in MISCtl0.

Power Control Register 0 (PCON): 0x87 ← 0x00

The SMOD bit used for the baud rate generator is setup via this register.

Table 18: The PCON Register

MSB LSB

SMOD	–	–	–	GF1	GF0	STOP	IDLE

Bit	Symbol	Function
PCON.7	SMOD	If SM0D = 1, the baud rate is doubled.
PCON.6	–	
PCON.5	–	
PCON.4	–	
PCON.3	GF1	General purpose flag 1.
PCON.2	GF0	General purpose flag 1.
PCON.1	STOP	Sets CPU to Stop mode.
PCON.0	IDLE	Sets CPU to Idle mode.

Interrupt Enable 1 Register (IEN1): 0xB8 ← 0x00

Table 20: The IEN1 Register

MSB							LSB
–	SWDT	EX6	EX5	EX4	EX3	EX2	–

Bit	Symbol	Function
IEN1.7	–	
IEN1.6	SWDT	Not used for interrupt control.
IEN1.5	EX6	EX6 = 0 – disable external interrupt 6.
IEN1.4	EX5	EX5 = 0 – disable external interrupt 5.
IEN1.3	EX4	EX4 = 0 – disable external interrupt 4.
IEN1.2	EX3	EX3 = 0 – disable external interrupt 3.
IEN1.1	EX2	EX2 = 0 – disable external interrupt 2.
IEN1.0	–	

Interrupt Enable 2 Register (IEN2): 0x9A ← 0x00

Table 21: The IEN2 Register

MSB							LSB
–	–	–	–	–	–	–	ES1

Bit	Symbol	Function
IEN2.0	ES1	ES1 = 0 – disable serial channel interrupt.

Miscellaneous Control Register 0 (MISCtl0): 0xFFF1 ← 0x00

Transmit and receive (TX and RX) pin selection and loop back test configuration are set up via this register.

Table 37: The MISCtl0 Register

MSB							LSB
PWRDN	–	–	–	–	–	SLPBK	SSEL

Bit	Symbol	Function
MISCtl0.7	PWRDN	This bit places the 73S1209F into a power down state.
MISCtl0.6	–	
MISCtl0.5	–	
MISCtl0.4	–	
MISCtl0.3	–	
MISCtl0.2	–	
MISCtl0.1	SLPBK	1 = UART loop back testing mode. The pins TXD and RXD are to be connected together externally (with SLPBK =1) and therefore: SLPBK SSEL Mode 0 0 normal using Serial_0 0 1 normal using Serial_1 1 0 Serial_0 TX feeds Serial_1 RX 1 1 Serial_1 TX feeds Serial_0 RX
MISCtl0.0	SSEL	Selects either Serial_1 if set =1 or Serial_0 if set = 0 to be connected to RXD and TXD pins.

1.7.4.1 Serial Interface 0

The Serial Interface 0 can operate in four modes:

- **Mode 0**

  Pin RX serves as $_{input}$ and output. TX outputs the shift clock. Eight bits are transmitted with the LSB first. The baud rate is fixed at 1/12 of the crystal frequency. Reception is initialized in Mode 0 by setting the flags in S0CON as follows: RI0 = 0 and REN0 = 1. In other modes, a start bit when REN0 = 1 starts receiving serial data.

- **Mode 1**

  Pin RX serves as input, and TX serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading S0BUF, and stop bit sets the flag RB80 in the Special Function Register S0CON. In mode 1 either internal baud rate generator or timer 1 can be use to specify baud rate.

- **Mode 2**

  This mode is similar to Mode 1, with two differences. The baud rate is fixed at 1/32 or 1/64 of oscillator frequency and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB80 in S0CON is output as the 9th bit, and at receive, the 9th bit affects RB80 in Special Function Register S0CON.

- **Mode 3**

  The only difference between Mode 2 and Mode 3 is that in Mode 3 either internal baud rate generator or timer 1 can be use to specify baud rate.

The S0BUF register is used to read/write data to/from the serial 0 interface.

1.7.5 Timers and Counters

The 80515 has two 16-bit timer/counter registers: Timer 0 and Timer 1. These registers can be configured for counter or timer operations.

In timer mode, the register is incremented every machine cycle, meaning that it counts up after every 12 periods of the MPU clock signal.

In counter mode, the register is incremented when the falling edge is observed at the corresponding input signal T0 or T1 (T0 and T1 are the timer gating inputs derived from USR[0:7] pins, see the User (USR) Ports section). Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle.

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function Registers (TMOD and TCON) are used to select the appropriate mode.

The Timer 0 load registers are designated as TL0 and TH0 and the Timer 1 load registers are designated as TL1 and TH1.

Timer/Counter Mode Control Register (TMOD): 0x89 ← 0x00

Table 40: The TMOD Register

MSB LSB

GATE	C/T	M1	M0	GATE	C/T	M1	M0
Timer 1				**Timer 0**			

Bits TR1 and TR0 in the TCON register start their associated timers when set.

Table 41: TMOD Register Bit Description

Bit	Symbol	Function
TMOD.7 TMOD.3	Gate	If set, enables external gate control (USR pin(s) connected to T0 or T1 for Counter 0 or 1, respectively). When T0 or T1 is high, and TRx bit is set (see the TCON register), a counter is incremented every falling edge on T0 or T1 input pin. If not set, the TRx bit controls the corresponding timer.
TMOD.6 TMOD.2	C/T	Selects Timer or Counter operation. When set to 1, the counter operation is performed based on the falling edge of T0 or T1. When cleared to 0, the corresponding register will function as a timer.
TMOD.5 TMOD.1	M1	Selects the mode for Timer/Counter 0 or Timer/Counter 1, as shown in the TMOD description.
TMOD.4 TMOD.0	M0	Selects the mode for Timer/Counter 0 or Timer/Counter 1, as shown in the TMOD description.

1.7.11 Keypad Interface

The 73S1209F supports a 30-button (6 row x 5 column) keypad (SPST Mechanical Contact Switches) interface using 11 dedicated I/O pins. Figure 11 shows a simplified block diagram of the keypad interface.

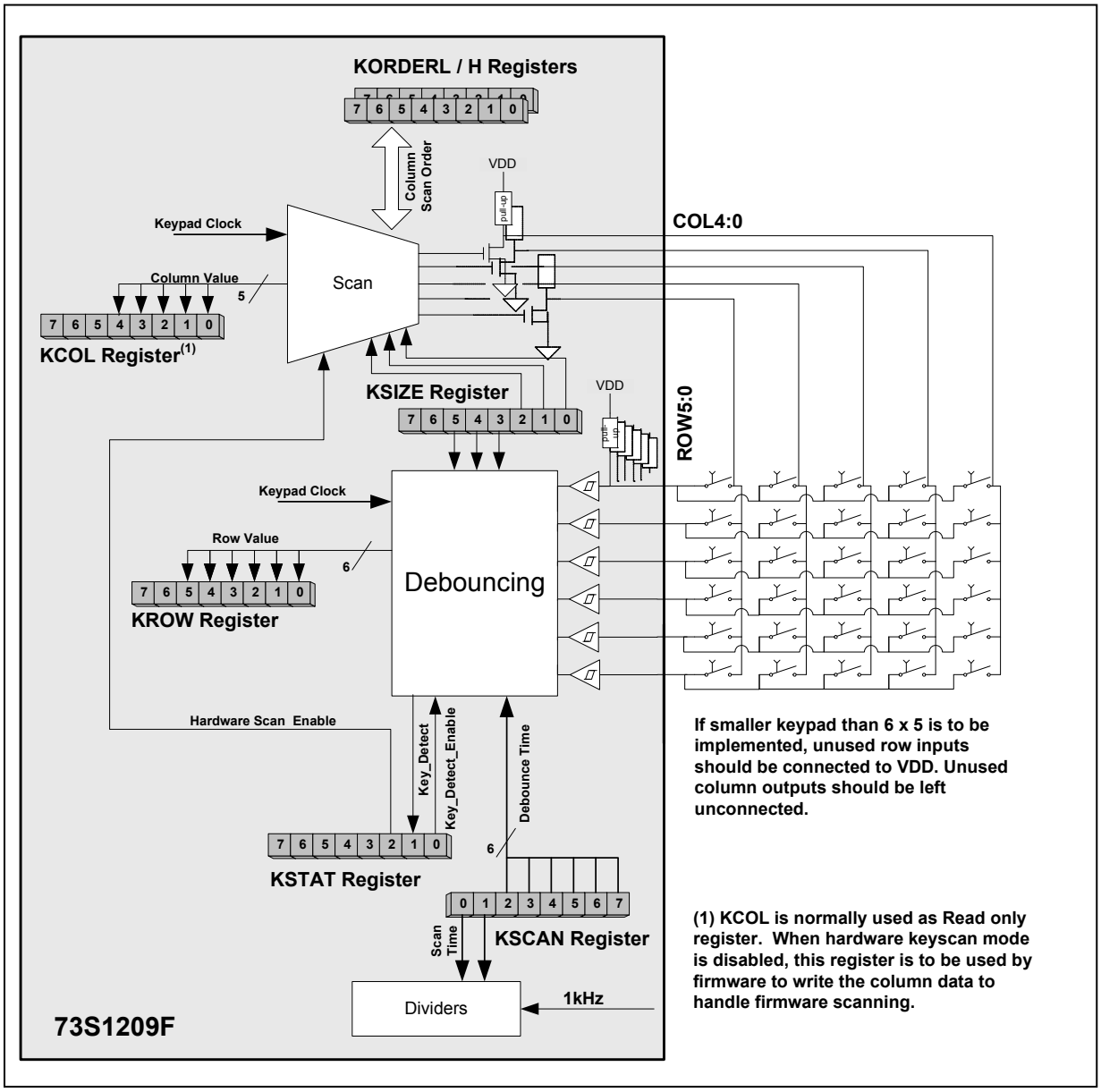

Figure 11: Simplified Keypad Block Diagram

There are 5 drive lines (outputs) corresponding to columns and 6 sense lines (inputs) corresponding to rows. Hysteresis and pull-ups are provided on all inputs (rows), which eliminate the need for external resistors in the keypad. Key scanning happens by asserting one of the 5 column lines low and looking for a low on a sense line indicating that a key is pressed (switch closed) at the intersection of the drive/sense (col/row) line in the keypad. Key detection is performed by hardware with an incorporated debounce timer. Debouncing time is adjustable through the KSCAN Register. Internal hardware circuitry performs column scanning at an adjustable scanning rate and column scanning order through registers KSCAN and KORDERL / KORDERH. Key scanning is disabled at reset and must be enabled by firmware. When a valid key is detected, an interrupt is generated and the valid value of the pressed key is automatically

written into KCOL and KROW registers. The keypad interface uses a 1kHz clock derived from the 12MHz crystal. The clock is enabled by setting bit 6 – KBEN – in the MCLKCtl register (see the Oscillator and Clock Generation section) to carry out scanning and debouncing. The keypad size can be adjusted within the KSIZE register.

Normal scanning is performed by hardware when the SCNEN bit is set to 1 in the KSTAT register. Figure 12 shows the flowchart of how the hardware scanning operates. In order to minimize power, scanning does not occur until a key-press is detected. Once hardware key scanning is enabled, the hardware drives all column outputs low and waits for a low to be detected on one of the inputs. When a low is detected on any row, and before key scanning starts, the hardware checks that the low level is still detected after a debounce time. The debounce time is defined by firmware in the KSCAN register (bits 7:0, DBTIME). Debounce times from 4ms to 256ms in 4ms increments are supported. If a key is not pressed after the debounce time, the hardware will go back to looking for any input to be low. If a key is confirmed to be pressed, key scanning begins.

Key scanning asserts one of the 5 drive lines (COL 4:0) low and looks for a low on a sense line indicating that a key is pressed at the intersection of the drive/sense line in the keypad. After all sense lines have been checked without a key-press being detected, the next column line is asserted. The time between checking each sense line is the scan time and is defined by firmware in the KSCAN register (bits 0:1 – SCTIME). Scan times from 1ms to 4ms are supported. Scanning order does not affect the scan time. This scanning continues until the entire keypad is scanned. If only one key is pressed, a valid key is detected. Simultaneous key presses are not considered as valid (If two keys are pressed, no key is reported to firmware).

Possible scrambling of the column scan order is provided by means of KORDERL and KORDERH registers that define the order of column scanning. Values in these registers must be updated every time a new keyboard scan order is desired. It is not possible to change the order of scanning the sense lines. The column and row intersection for the detected valid key are stored in the KCOL and KROW registers. When a valid key is detected, an interrupt is generated. Firmware can then read those registers to determine which key had been pressed. After reading the KCOL and KROW registers, the firmware can update the KORDERL / KORDERH registers if a new scan order is needed.

When the SCNEN bit is enabled in the KSTAT register, the KCOL and KROW registers are only updated after a valid key has been identified. The hardware does not wait for the firmware to service the interrupt in order to proceed with the key scanning process. Once the valid key (or invalid key – e.g. two keys pressed) is detected, the hardware waits for the key to be released. Once the key is released, the debounce timer is started. If the key is not still released after the debounce time, the debounce counter starts again. After a key release, all columns will be driven low as before and the process will repeat waiting for any key to be pressed.

When the SCNEN bit is disabled, all drive outputs are set to the value in the KCOL register. If firmware clears the SCNEN bit in the middle of a key scan, the KCOL register contains the last value stored in there which will then be reflected on the output pins.

A bypass mode is provided so that the firmware can do the key scanning manually (SCNEN bit must be cleared). In bypass mode, the firmware writes/reads the Column and Row registers to perform the key scanning.

1.7.13 Smart Card Interface Function

The 73S1209F integrates one ISO-7816 (T=0, T=1) UART, one complete ICC electrical interface as well as an external smart card interface to allow multiple smart cards to be connected using the Teridian 8010 family of interface devices. Figure 13 shows the simplified block diagram of the card circuitry (UART + interfaces), with detail of dedicated XRAM registers.

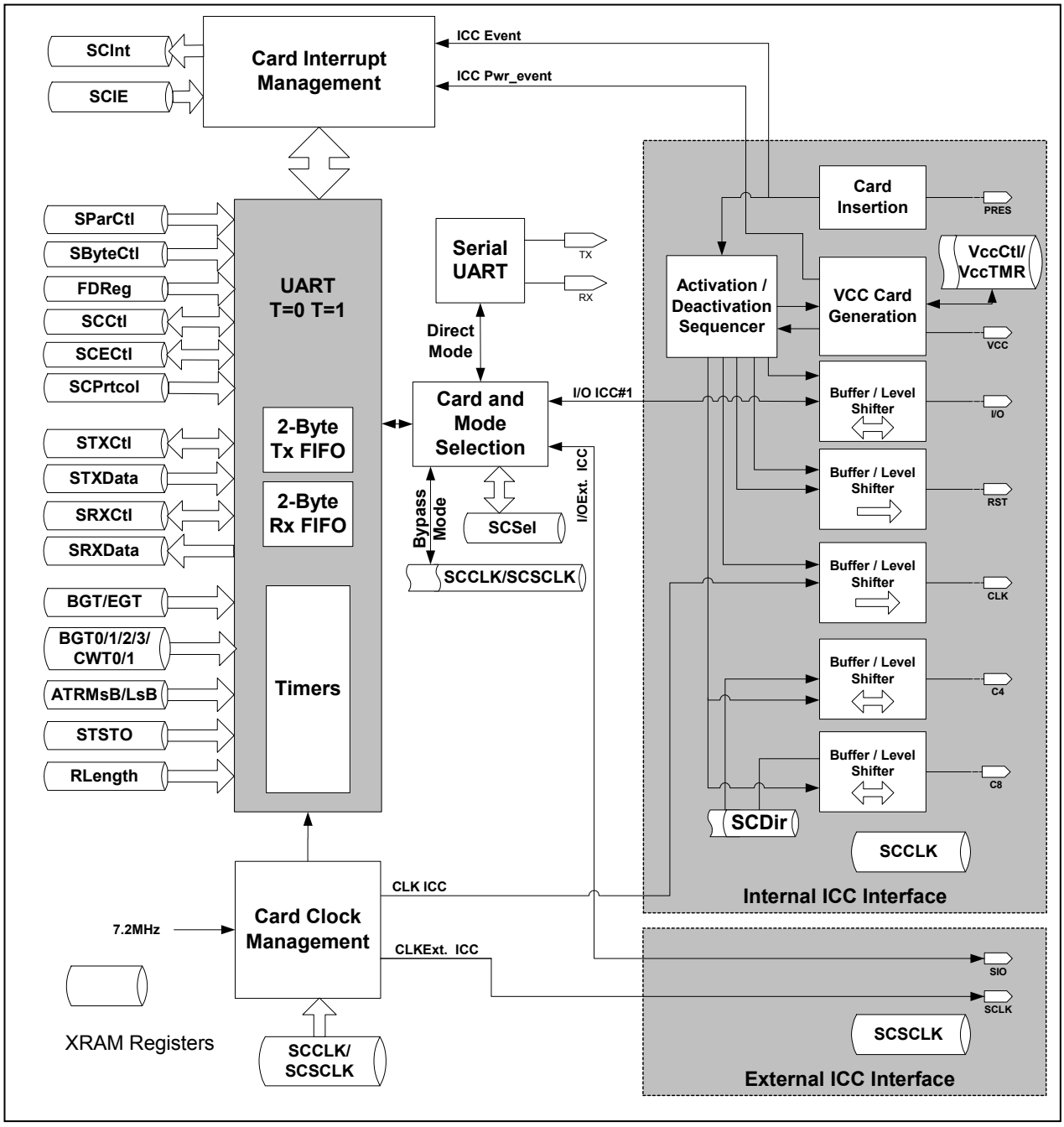

Figure 13: Smart Card Interface Block Diagram

Card interrupts are managed through two dedicated registers SCIE (Interrupt Enable to define which interrupt is enabled) and SCInt (Interrupt status). They allow the firmware to determine the source of an interrupt, that can be a card insertion / removal, card power fault, or a transmission (TX) or reception (RX) event / fault. It should be noted that even when card clock is disabled, an ICC interrupt can be generated

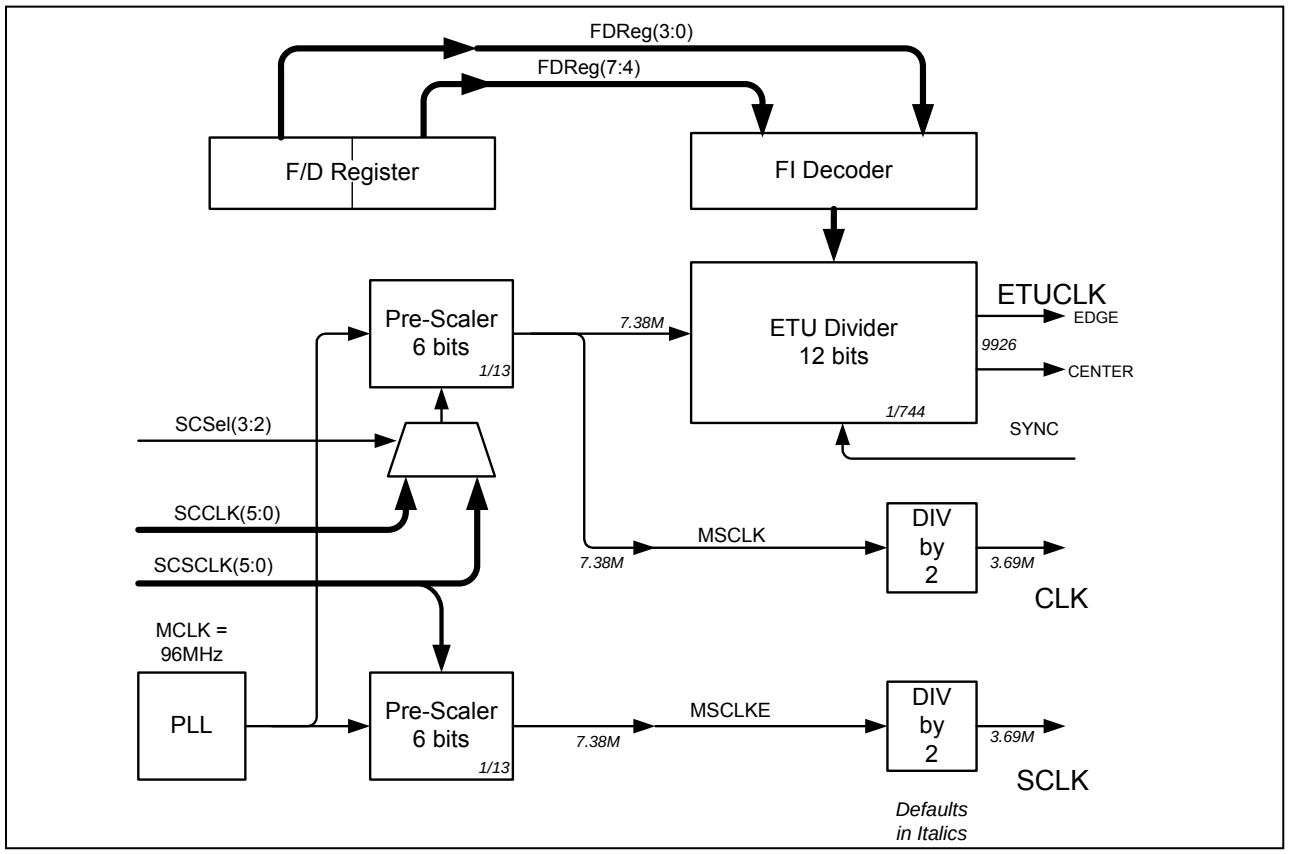

Figure 17: Smart Card CLK and ETU Generation

There are two, two-byte FIFOs that are used to buffer transmit and receive data. During a T=0 processing, if a parity error is detected by the 73S1209F during message reception, an error signal (BREAK) will be generated to the smart card. The byte received will be discarded and the firmware notified of the error. Break generation and receive byte dropping can be disabled under firmware control. During the transmission of a byte, if an error signal (BREAK) is detected, the last byte is retransmitted again and the firmware notified. Retransmission can be disabled by firmware. When a correct byte is received, an interrupt is generated to the firmware, which then reads the byte from the receive FIFO. Receive overruns are detected by the hardware and reported via an interrupt. During transmission of a message, the firmware will write bytes into the transmit FIFO. The hardware will send them to the smart card. When the last byte of a message has been written, the firmware will need to set the LASTTX bit in the STXCtl SFR. This will cause the hardware to insert the CRC/LRC if in a T=1 protocol mode. CRC/LRC generation/checking is only provided during T=1 processing. Firmware will need to instruct the smart function to go into receive mode after this last transmit data byte if it expects a response from the smart card. At the end of the smart card response, the firmware will put the interface back into transmit mode if appropriate.

The hardware can check for the following card-related timeouts:

- Character Waiting Time (CWT)
- Block Waiting Time (BWT)
- Initial Waiting Time (IWT)

The firmware will load the Wait Time registers with the appropriate value for the operating mode at the appropriate time. Figure 18 shows the guard, block, wait and ATR time definitions. If a timeout occurs, an interrupt will be generated and the firmware can take appropriate recovery steps. Support is provided for adding additional guard times between characters using the Extra Guard Time register (EGT) and between the last byte received by the 73S1209F and the first byte transmitted by the 73S1209F using the

Smart Card Interrupt Register (SCInt): 0xFE01 ← 0x00

When the smart card interrupt is asserted, the firmware can read this register to determine the actual cause of the interrupt. The bits are cleared when this register is read. Each interrupt can be disabled by the Smart Card Interrupt Enable register. Error processing must be handled by the firmware. This register relates to the interface that is active – see the SCSel register (above).

Table 74: The SCInt Register

MSB LSB

WAITTO	CRDEVT	VCCTMRI	RXDAV	TXEVT	TXSENT	TXERR	RXERR

Bit	Symbol	Function
SCInt.7	WAITTO	Wait Timeout – An ATR or card wait timeout has occurred. In sync mode, this interrupt is asserted when the RLen counter (it advances on falling edges of CLK/ETU) reaches the loaded (max) value. This bit is cleared when the SCInt register is read. When running in Synchronous Clock Stop Mode, this bit becomes RLenINT interrupt (set when the Rlen counter reaches the terminal count).
SCInt.6	CRDEVT	Card Event – A card event is signaled via pin DETCARD either when the Card was inserted or removed (read the CRDCtl register to determine card presence) or there was a fault condition in the interface circuitry. This bit is functional even if the smart card logic clock is disabled and when the PWRDN bit is set. This bit is cleared when the SCInt register is read.
SCInt.5	VCCTMRI	VCC Timer – This bit is set when the VCCTMR times out. This bit is cleared when the SCInt register is read.
SCInt.4	RXDAV	Rx Data Available – Data was received from the smart card because the Rx FIFO is not empty. In bypass mode, this interrupt is generated on a falling edge of the smart card I/O line. After receiving this interrupt in bypass mode, firmware should disable it until the firmware has received the entire byte and is waiting for the next start delimiter. This bit is cleared when there is no RX data available in the RX FIFO.
SCInt.3	TXEVNT	TX Event – Set whenever the TXEMTY or TXFULL bits are set in the SRXCtl SFR. This bit is cleared when the STXCtl register is read.
SCInt.2	TXSENT	TX Sent – Set whenever the ISO UART has successfully transmitted a byte to the smart card. Also set when a CRC/LRC byte is sent in T=1 mode. Will not be set in T=0 when a break is detected at the end of a byte (when break detection is enabled). This bit is cleared when the SCInt register is read.
SCInt.1	TXERR	TX Error – An error was detected during the transmission of data to the smart card as indicated by either BREAKD or TXUNDR bit being set in the STXCtl SFR. Additional information can be found in that register description. This bit is cleared when the STXCtl register is read.
SCInt.0	RXERR	RX Error – An error was detected during the reception of data from the smart card. Additional information can be found in the SRXCtl register. This interrupt will be asserted for RXOVRR, or RX Parity error events. This bit is cleared when the SRXCtl register is read.

STX Data Register (STXData): 0xFE07 ← 0x00

Table 80: The STXData Register

MSB							LSB
STXDAT.7	STXDAT.6	STXDAT.5	STXDAT.4	STXDAT.3	STXDAT.2	STXDAT.1	STXDAT.0

Bit	Function
STXData.7	Data to be transmitted to smart card. Gets stored in the TX FIFO and then extracted by the hardware and sent to the selected smart card. When the MPU reads this register, the byte pointer is changed to effectively "read out" the data. Thus, two reads will always result in an "empty" FIFO condition. The contents of the FIFO registers are not cleared, but will be overwritten by writes.
STXData.6	
STXData.5	
STXData.4	
STXData.3	
STXData.2	
STXData.1	
STXData.0	

SRX Control/Status Register (SRXCtl): 0xFE08 ← 0x00

This register is used to monitor reception of data from the smart card.

Table 81: The SRXCtl Register

MSB							LSB
BIT9DAT	–	LASTRX	CRCERR	RXFULL	RXEMTY	RXOVRR	PARITYE

Bit	Symbol	Function
SRXCtl.7	BIT9DAT	Bit 9 Data – When in sync mode and with MODE9/8B set, this bit will contain the data on IO (or SIO) pin that was sampled on the ninth CLK (or SCLK) rising edge. This is used to read data in synchronous 9-bit formats.
SRXCtl.6	–	
SRXCtl.5	LASTRX	Last RX Byte – User sets this bit during the reception of the last byte. When byte is received and this bit is set, logic checks CRC to match 0x1D0F (T=1 mode) or LRC to match 00h (T=1 mode), otherwise a CRC or LRC error is asserted.
SRXCtl.4	CRCERR	(Read only) 1 = CRC (or LRC) error has been detected.
SRXCtl.3	RXFULL	(Read only) RX FIFO is full. Status bit to indicate RX FIFO is full.
SRXCtl.2	RXEMTY	(Read only) RX FIFO is empty. This is only a status bit and does not generate a RX interrupt.
SRXCtl.1	RXOVRR	RX Overrun – (Read Only) Asserted when a receive-over-run condition has occurred. An over-run is defined as a byte was received from the smart card when the RX FIFO was full. Invalid data may be in the receive FIFO. Firmware should take appropriate action. Cleared when read. Additional writes to the RX FIFO are discarded when a RXOVRR occurs until the overrun condition is cleared. Will generate RXERR interrupt.
SRXCtl.0	PARITYE	Parity Error – (Read only) 1 = The logic detected a parity error on incoming data from the smart card. Cleared when read. Will generate RXERR interrupt.

Protocol Mode Register (SPrtcol): 0xFE0D ← 0x03

This register determines the protocol to be use when communicating with the selected smart card. This register should be updated as required when switching between smart card interfaces.

Table 86: The SPrtcol Register

MSB							LSB
SCISYN	MOD9/8B	SCESYN	0	TMODE	CRCEN	CRCMS	RCVATR

Bit	Symbol	Function
SPrtcol.7	SCISYN	Smart Card Internal Synchronous mode – Configures internal smart card interface for synchronous mode. This mode routes the internal interface buffers for RST, IO, C4, C8 to SCCtl register bits for direct firmware control. CLK is generated by the ETU counter.
SPrtcol.6	MOD9/8B	Synchronous 8/9 bit mode select – For sync mode, in protocols with 9-bit words, set this bit. The first eight bits read go into the RX FIFO and the ninth bit read will be stored in the IO (or SIO) data bit of the SRXCtl register.
SPrtcol.5	SCESYN	Smart Card External Synchronous mode – Configures External Smart Card interface for synchronous mode. This mode routes the external smart card interface buffers for SIO to SCECtl register bits for direct firmware control. SCLK is generated by the ETU counter.
SPrtcol.4	0	Reserved bit, must always be set to 0.
SPrtcol.3	TMODE	Protocol mode select – 0: T=0, 1: T=1. Determines which smart card protocol is to be used during message processing.
SPrtcol.2	CRCEN	CRC Enable – 1 = Enabled, 0 = Disabled. Enables the checking/generation of CRC/LRC while in T=1 mode. Has no effect in T=0 mode. If enabled and a message is being transmitted to the smart card, the CRC/LRC will be inserted into the message stream after the last TX byte is transmitted to the smart card. If enabled, CRC/LRC will be checked on incoming messages and the value made available to the firmware via the CRC LS/MS registers.
SPrtcol.1	CRCMS	CRC Mode Select - 1 = CRC, 0 = LRC. Determines type of checking algorithm to be used.
SPrtcol.0	RCVATR	Receive ATR – 1 = Enable ATR timeout, 0 = Disable ATR timeout. Set by firmware after the smart card has been turned on and the hardware is expecting ATR.

1.7.14 VDD Fault Detect Function

The 73S1209F contains a circuit to detect a low-voltage condition on the supply voltage V_{DD}. If enabled, it will deactivate the active internal smart card interface when V_{DD} falls below the V_{DD} Fault threshold. The register configures the V_{DD} Fault threshold for the nominal default of 2.3V* or a user selectable threshold. The user's code may load a different value using the FOVRVDDF bit =1 after the power-up cycle has completed

VDDFault Control Register (VDDFCtl): 0xFFD4 ← 0x00

Table 109: The VDDFCtl Register

MSB LSB

–	FOVRVDDF	VDDFLTEN	–	STXDAT.3	VDDFTH.2	VDDFTH.1	VDDFTH.0

Bit	Symbol	Function
VDDFCtl.7	–	
VDDFCtl.6	FOVRVDDF	Setting this bit high will allow the VDDFLT(2:0) bits set in this register to control the VDDFault threshold. When this bit is set low, the VDDFault threshold will be set to the factory default setting of 2.3V*.
VDDFCtl.5	VDDFLTEN	Set = 1 will disable VDD Fault operation.
VDDFCtl.4	–	
VDDFCtl.3	–	
VDDFCtl.2	VDDFTH.2	VDD Fault Threshold. Bit value(2:0) VDDFault voltage 000 2.3 (nominal default) 001 2.4 010 2.5 011 2.6 100 2.7 101 2.8 110 2.9 111 3.0
VDDFCtl.1	VDDFTH.1	
VDDFCtl.0	VDDFTH.0	

* Note: The V_{DD} Fault factory default can be set to any threshold as defined by bits VDDFTH(2:0). The 73S1209F has the capability to burn fuses at the factory to set the factory default to any of these voltages. Contact Teridian for further details.

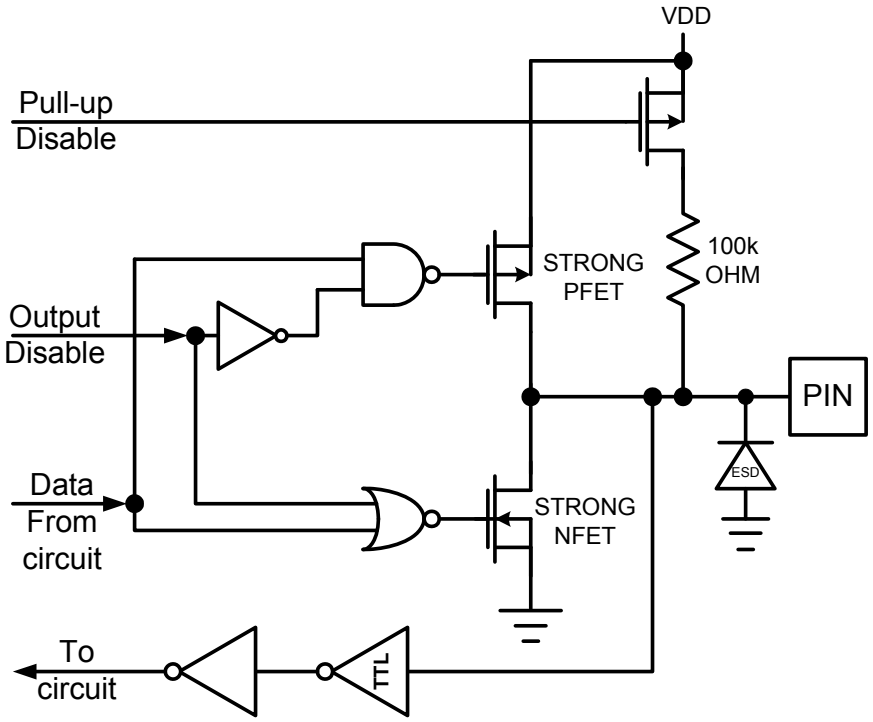

Figure 32: Keypad Row Circuit

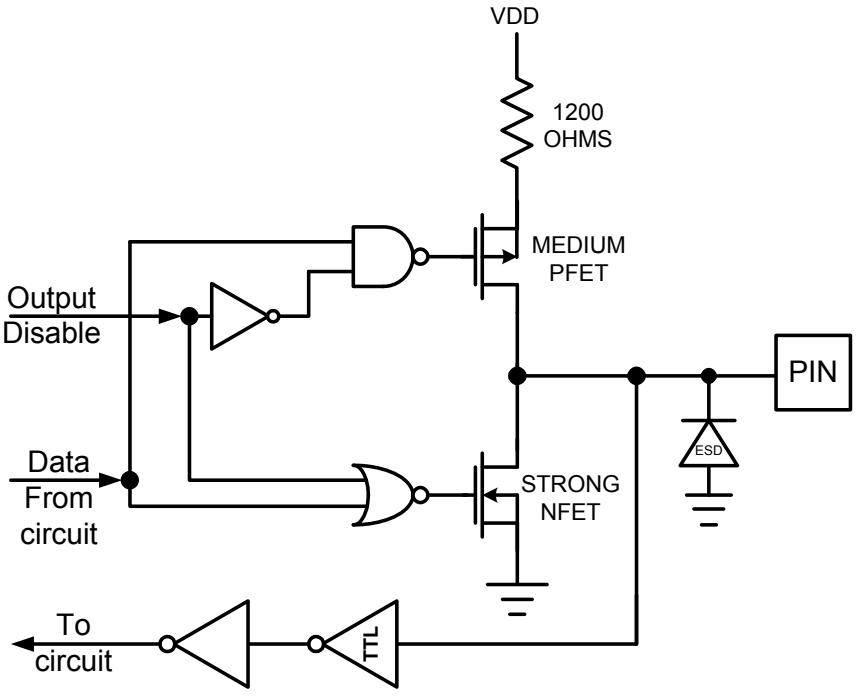

Figure 33: Keypad Column Circuit

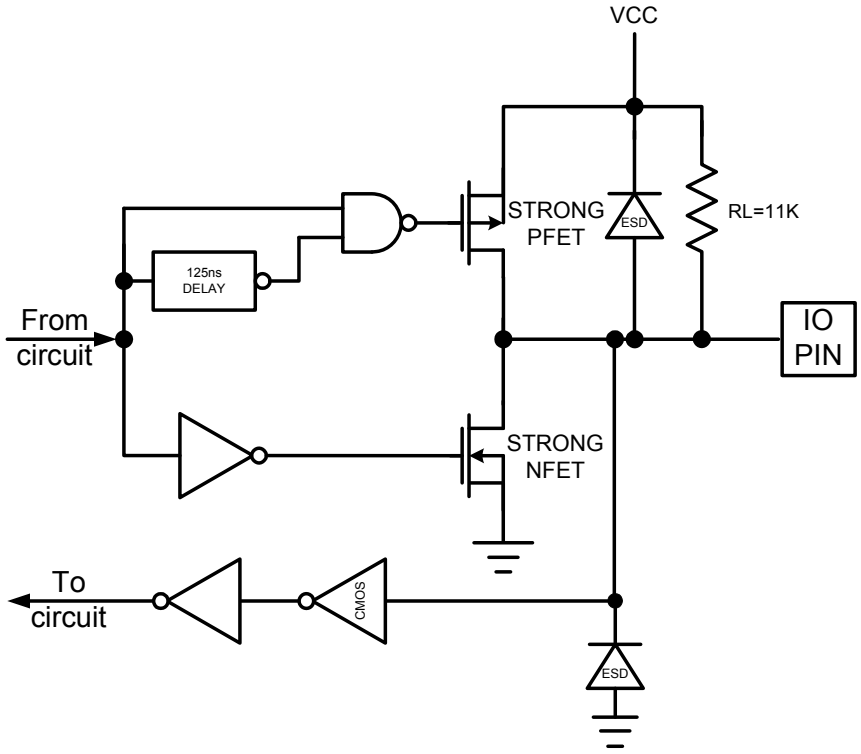

Figure 38: Smart Card I/O Circuit

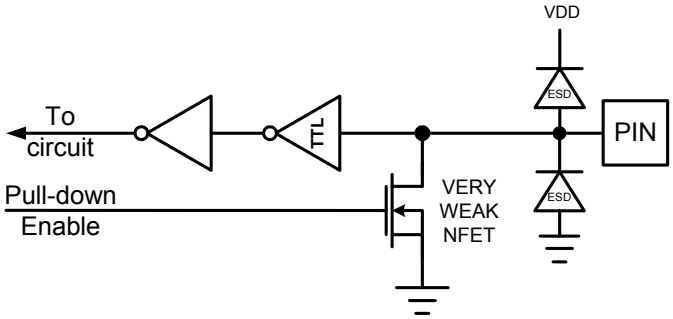

Figure 39: PRES Input Circuit

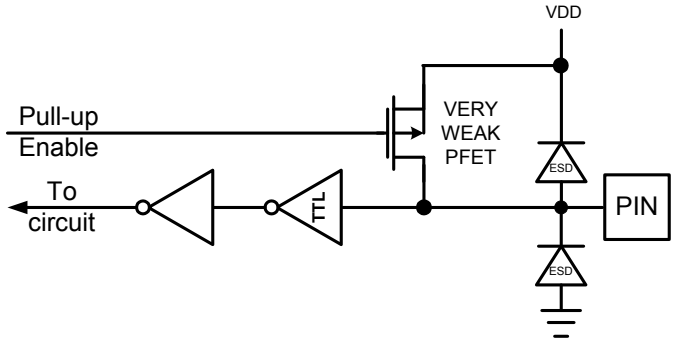

Figure 40: $\overline{\text{PRES}}$ Input Circuit

44-Pin QFN PACKAGE OUTLINE

Notes: 5.1mm x 5.1mm exposed pad area must remain UNCONNECTED (clear of PCB traces or vias). Controlling dimensions are in mm.

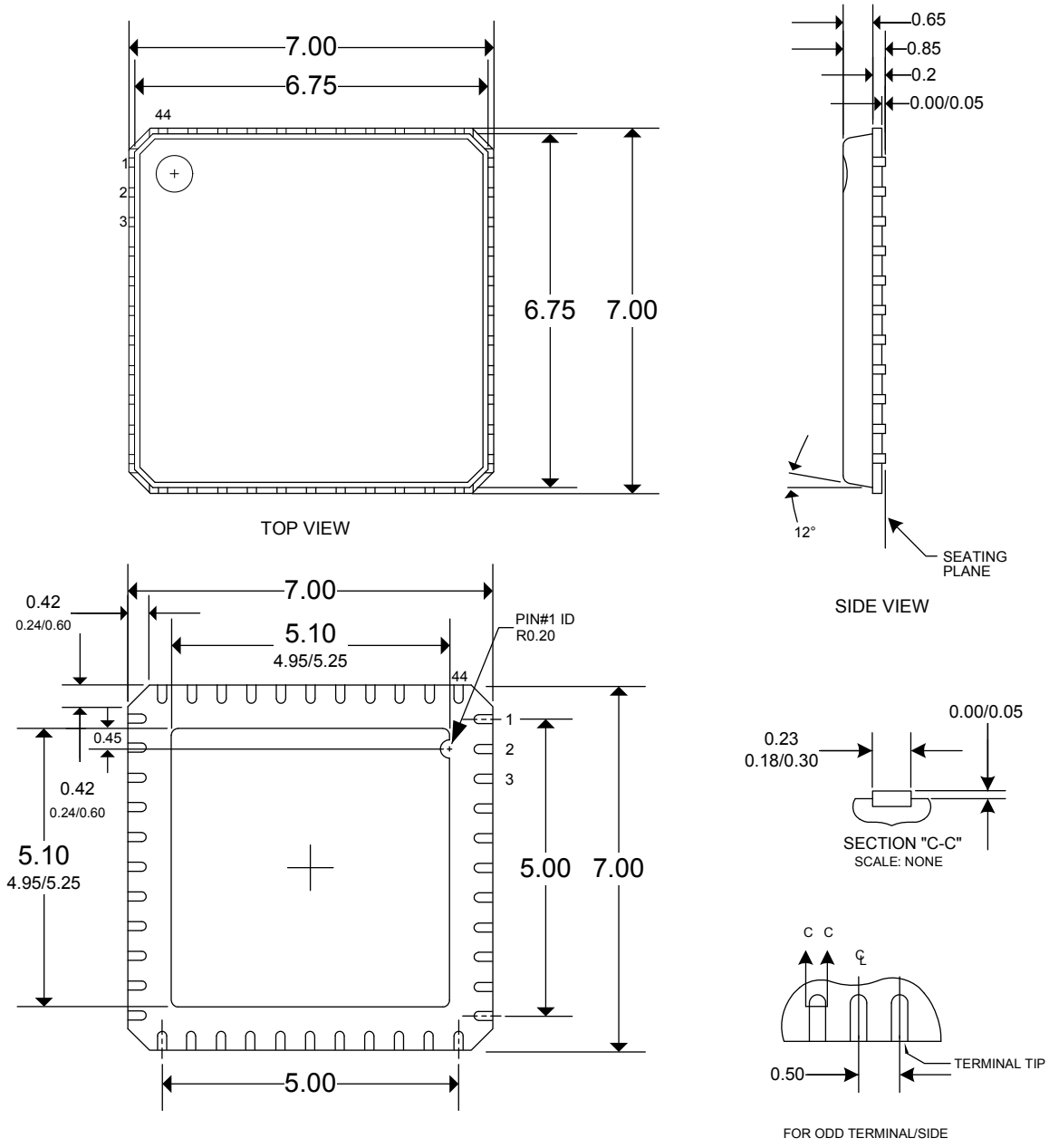

Figure 44: 73S1209F 44 QFN Pinout

5 Ordering Information

Table 110 lists the order numbers and packaging marks used to identify 73S1209F products.

Table 110: Order Numbers and Packaging Marks

Part Description	Order Number	Packaging Mark
73S1209F 68-Pin QFN Lead Free	73S1209F-68IM/F	73S1209F68IM
73S1209F 68-Pin QFN Lead Free, Tape and Reel	73S1209F-68IMR/F	73S1209F68IM
73S1209F 44-Pin QFN Lead Free	73S1209F-44IM/F	73S1209F44IM
73S1209F 44-Pin QFN Lead Free, Tape and Reel	73S1209F-44IMR/F	73S1209F44IM

6 Related Documentation

The following 73S1209F documents are available from Teridian Semiconductor Corporation:

73S1209F Data Sheet (this document)
73S1209F Development Board Quick Start Guide
73S1209F Software Development Kit Quick Start Guide
73S1209F Evaluation Board User's Guide
73S12xxF Software User's Guide
73S12xxF Synchronous Card Design Application Note

7 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73S1209F, contact us at:

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For a complete list of worldwide sales offices, go to http://www.teridian.com.