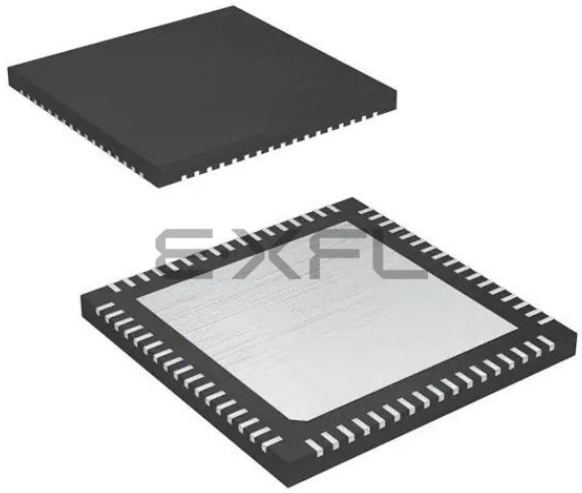
Analog Devices Inc./Maxim Integrated - 73S1209F-68IM/F/P Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	80515
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SmartCard, UART/USART
Peripherals	LED, POR, WDT
Number of I/O	9
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/73s1209f-68im-f-p

1.5 Special Function Registers (SFRs)

The 73S1209F utilizes numerous SFRs to communicate with the 73S1209F s many peripherals. This results in the need for more SFR locations outside the direct address IRAM space (0x80 to 0xFF). While some peripherals are mapped to unused IRAM SFR locations, additional SFRs for the smart card and other peripheral functions are mapped to the top of the XRAM data space (0xFC00 to 0xFFFF).

1.5.1 Internal Data Special Function Registers (SFRs)

A map of the Special Function Registers is shown in Table 6.

Table 6: IRAM Special Function Registers Locations

Hex\ Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/ Hex
F8									FF
F0	B								F7
E8									EF
E0	A								E7
D8	BRCON								DF
D0	PSW	**KCOL**	**KROW**	**KSCAN**	**KSTAT**	**KSIZE**	**KORDERL**	**KORDERH**	D7
C8	T2CON								CF
C0	IRCON								C7
B8	IEN1	IP1	S0RELH	S1RELH					BF
B0			**FLSHCTL**					**PGADDR**	B7
A8	IEN0	IP0	S0RELL						AF
A0	**USR8**	**UDIR8**							A7
98	S0CON	S0BUF	IEN2	S1CON	S1BUF	S1RELL			9F
90	**USR70**	**UDIR70**	DPS		**ERASE**				97
88	TCON	TMOD	TL0	TL1	TH0	TH1		**MCLKCtl**	8F
80		SP	DPL	DPH	DPL1	DPH1	WDTREL	PCON	87

Only a few addresses are used, the others are not implemented. SFRs specific to the 73S1209F are shown in **bold** print (gray background). Any read access to unimplemented addresses will return undefined data, while most write access will have no effect. However, a few locations are reserved and not user configurable in the 73S1209F. **Writes to the unused SFR locations can affect the operation of the core and therefore must not be written to. This applies to all the SFR areas in both the IRAM and XRAM spaces. In addition, all unused bit locations within valid SFR registers must be left in their default (power on default) states.**

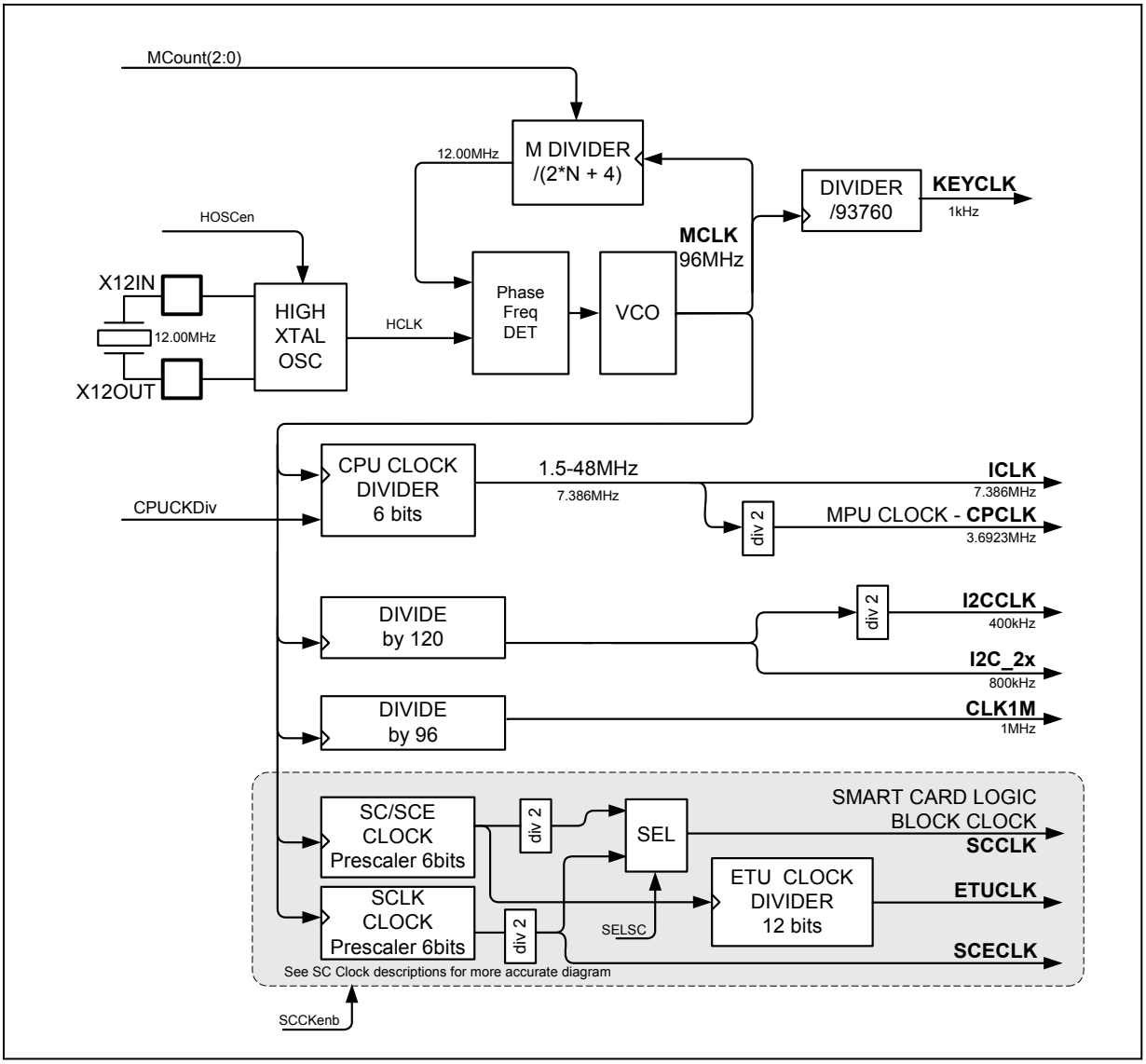


Figure 3: Clock Generation and Control Circuits

1.7.3 Interrupts

The 80515 core provides 10 interrupt sources with four priority levels. Each source has its own request flag(s) located in a special function register (TCON, IRCON, and SCON). Each interrupt requested by the corresponding flag can be individually enabled or disabled by the enable bits in SFRs IEN0, IEN1, and IEN2. Some of the 10 sources are multiplexed in order to expand the number of interrupt sources. These will be described in more detail in the respective sections.

External interrupts are the interrupts external to the 80515 core, i.e. signals that originate in other parts of the 73S1209F, for example the USR I/O, smart card interface, analog comparators, etc. The external interrupt configuration is shown in Figure 8.

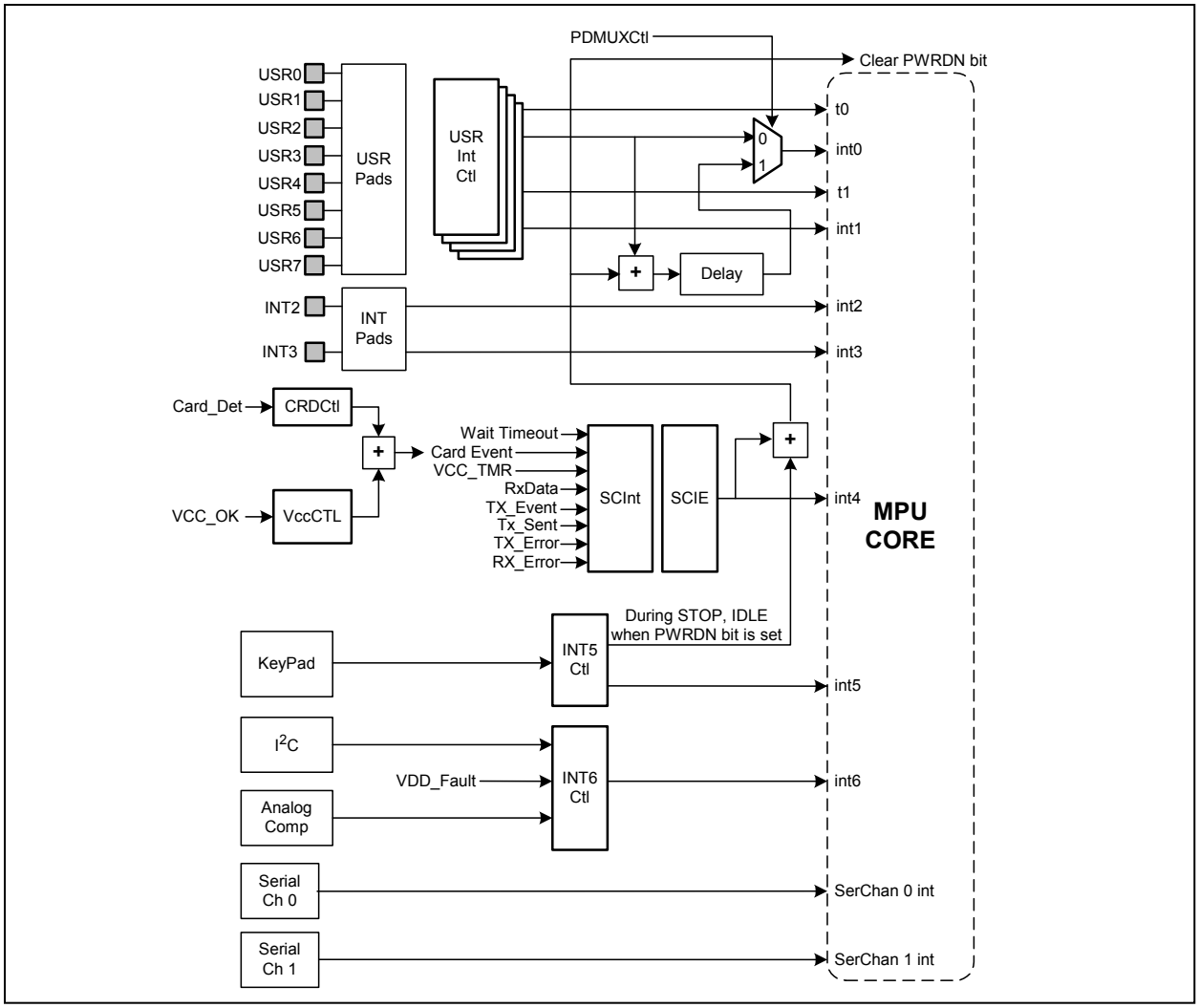


Figure 8: External Interrupt Configuration

Serial Interface 0 Control Register (S0CON): 0x9B ← 0x00

Transmit and receive data are transferred via this register.

Table 38: The S0CON Register

MSB LSB

SM0	SM1	SM20	REN0	TB80	RB80	TI0	RI0

Bit	Symbol	Function
S0CON.7	SM0	These two bits set the UART0 mode:
S0CON.6	SM1	
S0CON.5	SM20	Enables the inter-processor communication feature.
S0CON.4	REN0	If set, enables serial reception. Cleared by software to disable reception.
S0CON.3	TB80	The 9th transmitted data bit in Modes 2 and 3. Set or cleared by the MPU, depending on the function it performs (parity check, multiprocessor communication etc.).
S0CON.2	RB80	In Modes 2 and 3 it is the 9th data bit received. In Mode 1, if SM20 is 0, RB80 is the stop bit. In Mode 0 this bit is not used. Must be cleared by software.
S0CON.1	TI0	Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.
S0CON.0	RI0	Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software.

Mode	Description	SM0	SM1
0	N/A	0	0
1	8-bit UART	0	1
2	9-bit UART	1	0
3	9-bit UART	1	1

1.7.4.2 Serial Interface 1

The Serial Interface 1 can operate in 2 modes:

- **Mode A**

  This mode is similar to Mode 2 and 3 of Serial interface 0, 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB81 in S1CON is outputted as the 9th bit, and at receive, the 9th bit affects RB81 in Special Function Register S1CON. The only difference between Mode 3 and A is that in Mode A only the internal baud rate generator can be use to specify baud rate.

- **Mode B**

  This mode is similar to Mode 1 of Serial interface 0. Pin RX serves as input, and TX serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading S1BUF, and stop bit sets the flag RB81 in the Special Function Register S1CON. In mode 1, the internal baud rate generator is use to specify the baud rate.

The S1BUF register is used to read/write data to/from the serial 1 interface.

Table 42: Timers/Counters Mode Description

M1	M0	Mode	Function
0	0	Mode 0	13-bit Counter/Timer.
0	1	Mode 1	16-bit Counter/Timer.
1	0	Mode 2	8-bit auto-reload Counter/Timer.
1	1	Mode 3	If Timer 1 M1 and M0 bits are set to '1', Timer 1 stops. If Timer 0 M1 and M0 bits are set to '1', Timer 0 acts as two independent 8-bit Timer/Counters.

Mode 0

Putting either timer/counter into mode 0 configures it as an 8-bit timer/counter with a divide-by-32 prescaler. In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1's to all 0's, it sets the timer overflow flag TF0. The overflow flag TF0 then can be used to request an interrupt. The counted input is enabled to the timer when TRx = 1 and either GATE = 0 or TX = 1 (setting GATE = 1 allows the timer to be controlled by external input TX, to facilitate pulse width measurements). TRx are control bits in the special function register TCON; GATE is in TMOD. The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TRx) does not clear the registers. Mode 0 operation is the same for timer 0 as for timer 1.

Mode 1

Mode 1 is the same as mode 0, except that the timer register is run with all 16 bits.

Mode 2

Mode 2 configures the timer register as an 8-bit counter (TLx) with automatic reload. The overflow from TLx not only sets TFx, but also reloads TLx with the contents of THx, which is preset by software. The reload leaves THx unchanged.

Mode 3

Mode 3 has different effects on timer 0 and timer 1. Timer 1 in mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in mode 3 establishes TL0 and TH0 as two separate counters. TL0 uses the timer 0 control bits: C/T, GATE, TR0, INT0, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from timer 1. Thus, TH0 now controls the "timer 1" interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter. When timer 0 is in mode 3, timer 1 can be turned on and off by switching it out of and into its own mode 3, or can still be used by the serial channel as a baud rate generator, or in fact, in any application not requiring an interrupt from timer 1 itself.

Interrupt Enable 0 Register (IEN0): 0xA8 ← 0x00

Table 44: The IEN0 Register

MSB							LSB
EAL	WDT	ET2	ES0	ET1	EX1	ET0	EX0

Bit	Symbol	Function
IEN0.7	EAL	EAL = 0 – disable all interrupts.
IEN0.6	WDT	Watchdog timer refresh flag. Set to initiate a refresh of the watchdog timer. Must be set directly before SWDT is set to prevent an unintentional refresh of the watchdog timer. WDT is reset by hardware 12 clock cycles after it has been set.
IEN0.5	–	
IEN0.4	ES0	ES0 = 0 – disable serial channel 0 interrupt.
IEN0.3	ET1	ET1 = 0 – disable timer 1 overflow interrupt.
IEN0.2	EX1	EX1 = 0 – disable external interrupt 1.
IEN0.1	ET0	ET0 = 0 – disable timer 0 overflow interrupt.
IEN0.0	EX0	EX0 = 0 – disable external interrupt 0.

Interrupt Enable 1 Register (IEN1): 0xB8 ← 0x00

Table 45: The IEN1 Register

MSB							LSB
–	SWDT	EX6	EX5	EX4	EX3	EX2	

Bit	Symbol	Function
IEN1.7	–	
IEN1.6	SWDT	Watchdog timer start/refresh flag. Set to activate/refresh the watchdog timer. When directly set after setting WDT, a watchdog timer refresh is performed. Bit SWDT is reset by the hardware 12 clock cycles after it has been set.
IEN1.5	EX6	EX6 = 0 – disable external interrupt 6.
IEN1.4	EX5	EX5 = 0 – disable external interrupt 5.
IEN1.3	EX4	EX4 = 0 – disable external interrupt 4.
IEN1.2	EX3	EX3 = 0 – disable external interrupt 3.
IEN1.1	EX2	EX2 = 0 – disable external interrupt 2.
IEN1.0	–	

External Interrupt Control Register (USRIntCtl1) : 0xFF90 ← 0x00

Table 51: The USRIntCtl1 Register

MSB							LSB
–	U1IS.6	U1IS.5	U1IS.4	–	U0IS.2	U0IS.1	U0IS.0

External Interrupt Control Register (USRIntCtl2) : 0xFF91 ← 0x00

Table 52: The USRIntCtl2 Register

MSB							LSB
–	U3IS.6	U3IS.5	U3IS.4	–	U2IS.2	U2IS.1	U2IS.0

External Interrupt Control Register (USRIntCtl3) : 0xFF92 ← 0x00

Table 53: The USRIntCtl3 Register

MSB							LSB
–	U5IS.6	U5IS.5	U5IS.4	–	U4IS.2	U4IS.1	U4IS.0

External Interrupt Control Register (USRIntCtl4) : 0xFF93 ← 0x00

Table 54: The USRIntCtl4 Register

MSB							LSB
–	U7IS.6	U7IS.5	U7IS.4	–	U6IS.2	U6IS.1	U6IS.0

Device Address Register (DAR): 0xFF80 ← 0x00

Table 58: The DAR Register

MSB							LSB
DVADR.6	DVADR.5	DVADR.4	DVADR.3	DVADR.2	DVADR.1	DVADR.0	I2CRW

Bit	Symbol	Function
DAR.7	DVADR [0:6]	Slave device address.
DAR.6		
DAR.5		
DAR.4		
DAR.3		
DAR.2		
DAR.1		
DAR.0	I2CRW	If set = 0, the transaction is a write operation. If set = 1, read.

I2C Write Data Register (WDR): 0XFF81 ← 0x00

Table 59: The WDR Register

MSB							LSB
WDR.7	WDR.6	WDR.5	WDR.4	WDR.3	WDR.2	WDR.1	WDR.0

Bit	Function
WDR.7	Data to be written to the I^2C slave device.
WDR.6	
WDR.5	
WDR.4	
WDR.3	
WDR.2	
WDR.1	
WDR.0	

External Interrupt Control Register (INT6Ctl): 0xFF95 ← 0x00

Table 64: The INT6Ctl Register

MSB LSB

–	–	VFTIEN	VFTINT	I2CIEN	I2CINT	ANIEN	ANINT

Bit	Symbol	Function
INT6Ctl.7	–	
INT6Ctl.6	–	
INT6Ctl.5	VFTIEN	VDD fault interrupt enable.
INT6Ctl.4	VFTINT	VDD fault interrupt flag.
INT6Ctl.3	I2CIEN	When set = 1, the I^2C interrupt is enabled.
INT6Ctl.2	I2CINT	When set =1, the I^2C transaction has completed. Cleared upon the start of a subsequent I^2C transaction.
INT6Ctl.1	ANIEN	Analog compare interrupt enable.
INT6Ctl.0	ANINT	Analog compare interrupt flag.

Keypad Column MS Scan Order Register (KORDERH): 0xD7 ← 0x00

Table 71: The KORDERH Register

MSB							LSB
–	5COL.2	5COL.1	5COL.0	4COL.2	4COL.1	4COL.0	3COL.2

Bit	Symbol	Function
KORDERH.7	–	
KORDERH.6	5COL.2	Column to scan 5th.
KORDERH.5	5COL.1	
KORDERH.4	5COL.0	
KORDERH.3	4COL.2	Column to scan 4th.
KORDERH.2	4COL.1	
KORDERH.1	4COL.0	
KORDERH.0	3COL.2	Column to scan 3rd (msb).

External Interrupt Control Register (INT5Ctl): 0xFF94 ← 0x00

Table 72: The INT5Ctl Register

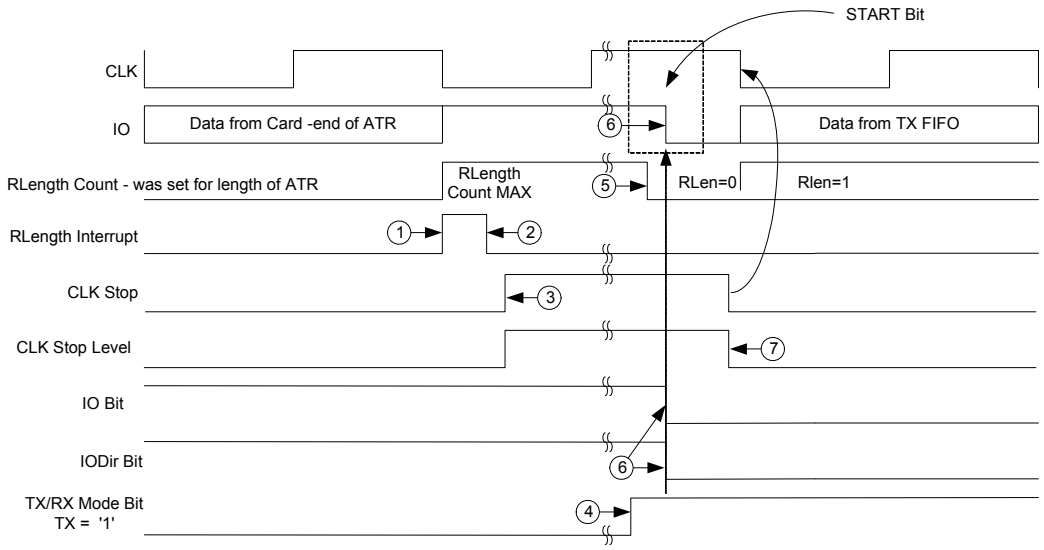
MSB							LSB
PDMUX	–	RTCIEN	RTCINT	USBIEN	USBINT	KPIEN	KPINT

Bit	Symbol	Function
INT5Ctl.7	PDMUX	Power down multiplexer control.
INT5Ctl.6	–	
INT5Ctl.5	RTCIEN	When set =1, enables RTC interrupt.
INT5Ctl.4	RTCINT	When set =1, indicates interrupt from Real Time Clock function. Cleared on read of register.
INT5Ctl.3	USBIEN	USB interrupt enable.
INT5Ctl.2	USBINT	USB interrupt flag.
INT5Ctl.1	KPIEN	Enables Keypad interrupt when set = 1.
INT5Ctl.0	KPINT	This bit indicates the Keypad logic has set Key_Detect bit and a key location may be read. Cleared on read of register.

1.7.12 Emulator Port

The emulator port, consisting of the pins E_RST, E_TCLK and E_RXTX, provides control of the MPU through an external in-circuit emulator. The E_TBUS[3:0] pins, together with the E_ISYNC/BRKRQ, add trace capability to the emulator. The emulator port is compatible with the ADM51 emulators manufactured by Signum Systems.

If code trace capability is needed on this interface, 20pF capacitors (to ground) need to be added to allow the trace function capability to run properly. These capacitors should be attached to the TBUS0:3 and ISBR signals.

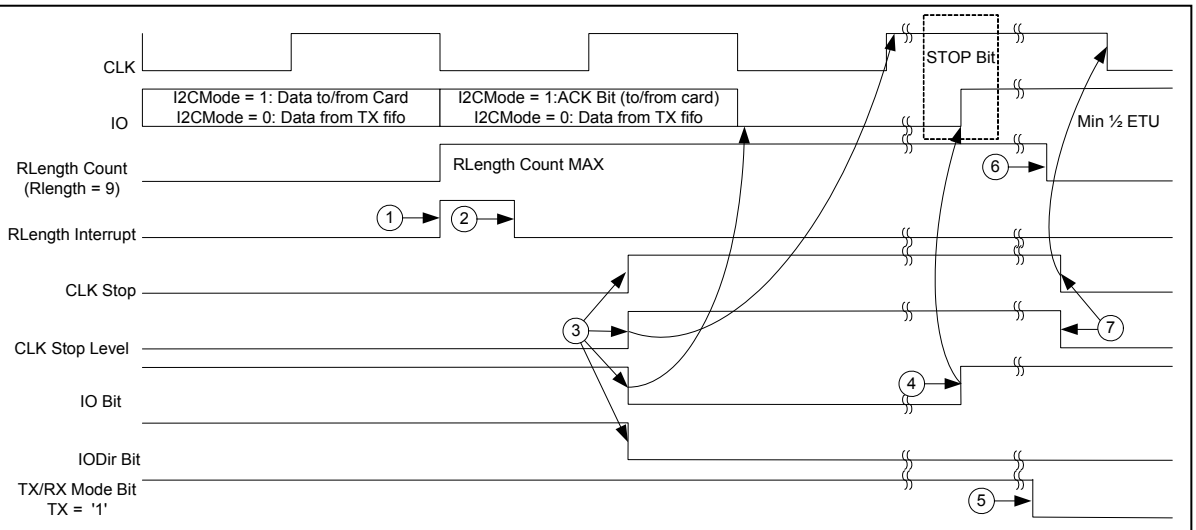


1. Interrupt generated when Rlength counter is MAX.
2. Read and clear Interrupt.
3. Set CLK Stop and CLK Stop level high in Interrupt routine.
4. Set TX/RX Bit to TX mode.
5. Reload Rlength Counter.
6. Set IO Bit low and IODir = Output. Since Rlen=(MAX or 0) and TX/RX =1, IO pin is controlled by IO bit.
7. Clear CLK Stop and CLK Stop level.

Note: Data in TX fifo should not be Empty here.

Synchronous Clock Start/Stop Mode style Start bit procedure. This procedure should be used to generate the start bit insertion in Synchronous mode for Synchronous Clock Start/Stop Mode protocol.

Figure 21: Creation of Synchronous Clock Start/Stop Mode Start Bit in Sync Mode



1. Interrupt generated when Rlength counter is MAX.
2. Read and clear Interrupt.
3. Set CLK Stop and CLK Stop level high, set IO Bit low and IODir = Output.
4. Set IO Bit High and IODir = Output.
5. Set TX/RX Bit to RX mode.
6. Reload Rlength Counter.
7. Clear CLK Stop and CLK Stop level.

Synchronous Clock Start/Stop Mode Stop bit procedure. This procedure should be used to generate the Stop bit in Synchronous Mode.

Figure 22: Creation of Synchronous Clock Start/Stop Mode Stop Bit in Sync Mode

Smart Card Interrupt Register (SCInt): 0xFE01 ← 0x00

When the smart card interrupt is asserted, the firmware can read this register to determine the actual cause of the interrupt. The bits are cleared when this register is read. Each interrupt can be disabled by the Smart Card Interrupt Enable register. Error processing must be handled by the firmware. This register relates to the interface that is active – see the SCSel register (above).

Table 74: The SCInt Register

MSB LSB

WAITTO	CRDEVT	VCCTMRI	RXDAV	TXEVT	TXSENT	TXERR	RXERR

Bit	Symbol	Function
SCInt.7	WAITTO	Wait Timeout – An ATR or card wait timeout has occurred. In sync mode, this interrupt is asserted when the RLen counter (it advances on falling edges of CLK/ETU) reaches the loaded (max) value. This bit is cleared when the SCInt register is read. When running in Synchronous Clock Stop Mode, this bit becomes RLenINT interrupt (set when the Rlen counter reaches the terminal count).
SCInt.6	CRDEVT	Card Event – A card event is signaled via pin DETCARD either when the Card was inserted or removed (read the CRDCtl register to determine card presence) or there was a fault condition in the interface circuitry. This bit is functional even if the smart card logic clock is disabled and when the PWRDN bit is set. This bit is cleared when the SCInt register is read.
SCInt.5	VCCTMRI	VCC Timer – This bit is set when the VCCTMR times out. This bit is cleared when the SCInt register is read.
SCInt.4	RXDAV	Rx Data Available – Data was received from the smart card because the Rx FIFO is not empty. In bypass mode, this interrupt is generated on a falling edge of the smart card I/O line. After receiving this interrupt in bypass mode, firmware should disable it until the firmware has received the entire byte and is waiting for the next start delimiter. This bit is cleared when there is no RX data available in the RX FIFO.
SCInt.3	TXEVNT	TX Event – Set whenever the TXEMTY or TXFULL bits are set in the SRXCtl SFR. This bit is cleared when the STXCtl register is read.
SCInt.2	TXSENT	TX Sent – Set whenever the ISO UART has successfully transmitted a byte to the smart card. Also set when a CRC/LRC byte is sent in T=1 mode. Will not be set in T=0 when a break is detected at the end of a byte (when break detection is enabled). This bit is cleared when the SCInt register is read.
SCInt.1	TXERR	TX Error – An error was detected during the transmission of data to the smart card as indicated by either BREAKD or TXUNDR bit being set in the STXCtl SFR. Additional information can be found in that register description. This bit is cleared when the STXCtl register is read.
SCInt.0	RXERR	RX Error – An error was detected during the reception of data from the smart card. Additional information can be found in the SRXCtl register. This interrupt will be asserted for RXOVRR, or RX Parity error events. This bit is cleared when the SRXCtl register is read.

Smart Card Interrupt Enable Register (SCIE): 0xFE02 ← 0x00

When set to a 1, the respective condition can cause a smart card interrupt. When set to a 0, the respective condition cannot cause an interrupt. When disabled, the respective bit in the Smart Card Interrupt register can still be set, but it will not interrupt the MPU.

Table 75: The SCIE Register

MSB LSB

WTOIEN	CDEVEN	VTMREN	RXDAEN	TXEVEN	TXSNTEN	TXEREN	RXEREN

Bit	Symbol	Function
SCIE.7	WTOIEN	Wait Timeout Interrupt Enable – Enable for ATR or Wait Timeout Interrupt. In sync mode, function is RLIEN (RLen = max.) interrupt enable.
SCIE.6	CDEVEN	Card Event Interrupt Enable.
SCIE.5	VTMREN	VCC Timer Interrupt Enable.
SCIE.4	RXDAEN	Rx Data Available Interrupt Enable.
SCIE.3	TXEVEN	TX Event Interrupt Enable.
SCIE.2	TXSNTEN	TX Sent Interrupt Enable.
SCIE.1	TXEREN	TX Error Interrupt Enable.
SCIE.0	RXEREN	RX Error Interrupt Enable.

STX Data Register (STXData): 0xFE07 ← 0x00

Table 80: The STXData Register

MSB							LSB
STXDAT.7	STXDAT.6	STXDAT.5	STXDAT.4	STXDAT.3	STXDAT.2	STXDAT.1	STXDAT.0

Bit	Function
STXData.7	Data to be transmitted to smart card. Gets stored in the TX FIFO and then extracted by the hardware and sent to the selected smart card. When the MPU reads this register, the byte pointer is changed to effectively "read out" the data. Thus, two reads will always result in an "empty" FIFO condition. The contents of the FIFO registers are not cleared, but will be overwritten by writes.
STXData.6	
STXData.5	
STXData.4	
STXData.3	
STXData.2	
STXData.1	
STXData.0	

SRX Control/Status Register (SRXCtl): 0xFE08 ← 0x00

This register is used to monitor reception of data from the smart card.

Table 81: The SRXCtl Register

MSB							LSB
BIT9DAT	–	LASTRX	CRCERR	RXFULL	RXEMTY	RXOVRR	PARITYE

Bit	Symbol	Function
SRXCtl.7	BIT9DAT	Bit 9 Data – When in sync mode and with MODE9/8B set, this bit will contain the data on IO (or SIO) pin that was sampled on the ninth CLK (or SCLK) rising edge. This is used to read data in synchronous 9-bit formats.
SRXCtl.6	–	
SRXCtl.5	LASTRX	Last RX Byte – User sets this bit during the reception of the last byte. When byte is received and this bit is set, logic checks CRC to match 0x1D0F (T=1 mode) or LRC to match 00h (T=1 mode), otherwise a CRC or LRC error is asserted.
SRXCtl.4	CRCERR	(Read only) 1 = CRC (or LRC) error has been detected.
SRXCtl.3	RXFULL	(Read only) RX FIFO is full. Status bit to indicate RX FIFO is full.
SRXCtl.2	RXEMTY	(Read only) RX FIFO is empty. This is only a status bit and does not generate a RX interrupt.
SRXCtl.1	RXOVRR	RX Overrun – (Read Only) Asserted when a receive-over-run condition has occurred. An over-run is defined as a byte was received from the smart card when the RX FIFO was full. Invalid data may be in the receive FIFO. Firmware should take appropriate action. Cleared when read. Additional writes to the RX FIFO are discarded when a RXOVRR occurs until the overrun condition is cleared. Will generate RXERR interrupt.
SRXCtl.0	PARITYE	Parity Error – (Read only) 1 = The logic detected a parity error on incoming data from the smart card. Cleared when read. Will generate RXERR interrupt.

FD Control Register (FDReg): 0xFE13 ← 0x11

Table 91: The FDReg Register

MSB							LSB
FVAL.3	FVAL.2	FVAL.1	FVAL.0	DVAL.3	DVAL.2	DVAL.1	DVAL.0

Bit	Symbol	Function
FDReg.7	FVAL.3	Refer to Table 93 above. This value is converted per the table to set the divide ratio used to generate the baud rate (ETU). Default, also used for ATR, is 0001 (Fi = 372). This value is used by the selected interface.
FDReg.6	FVAL.2	
FDReg.5	FVAL.1	
FDReg.4	FVAL.0	
FDReg.3	DVAL.3	Refer to Table 93 above. This value is used to set the divide ratio used to generate the smart card CLK. Default, also used for ATR, is 0001 (Di = 1).
FDReg.2	DVAL.2	
FDReg.1	DVAL.1	
FDReg.0	DVAL.0	

This register uses the transmission factors F and D to set the ETU (baud) rate. The values in this register are mapped to the ISO 7816 conversion factors as described below. The CLK signal for each interface is created by dividing a high-frequency, intermediate signal (MSCLK) by 2. The ETU baud rate is created by dividing MSCLK by 2 times the Fi/Di ratio specified by the codes below. For example, if FI = 0001 and DI = 0001, the ratio of Fi/Di is 372/1. Thus the ETU divider is configured to divide by 2 * 372 = 744. The maximum supported F/D ratio is 4096.

Table 92: Divider Ratios Provided by the ETU Counter

FI (code)	0000	0001	0010	0011	0100	0101	0110	0111
Fi (ratio)	372	372	558	744	1116	1488	1860	1860⊕
FCLK max	4	5	6	8	12	16	20	20⊕

FI(code)	1000	1001	1010	1011	1100	1101	1110	1111
Fi(ratio)	512⊕	512	768	1024	1536	2048	2048⊕	2048⊕
FCLK max	5⊕	5	7.5	10	15	20	20⊕	20⊕

DI(code)	0000	0001	0010	0011	0100	0101	0110	0111
Di(ratio)	1⊕	1	2	4	8	16	32	32⊕

DI(code)	1000	1001	1010	1011	1100	1101	1110	1111
Di(ratio)	12	20	16⊕	16⊕	16⊕	16⊕	16⊕	16⊕

Note: values marked with ⊕ are not included in the ISO definition and arbitrary values have been assigned.

The values given below are used by the ETU divider to create the ETU clock. The entries that are not shaded will result in precise CLK/ETU per ISO requirements. Shaded areas are not precise but are within 1% of the target value.

Block Guard Time Register (BGT): 0xFE16 ← 0x10

This register contains the Extra Guard Time Value (EGT) most-significant bit. The Extra Guard Time indicates the minimum time between the leading edges of the start bit of consecutive characters. The delay is depends on the T=0/T=1 mode. Used in transmit mode. This register also contains the Block Guard Time (BGT) value. Block Guard Time is the minimum time between the leading edge of the start bit of the last character received and the leading edge of the start bit of the first character transmitted. This should not be set less than the character length. The transmission of the first character will be held off until BGT has elapsed regardless of the TX data and TX/RX control bit timing.

Table 96: The BGT Register

MSB							LSB
EGT.8	–	–	BGT.4	BGT.3	BGT.1	BGT.2	BGT.0

Bit	Symbol	Function
BGT.7	EGT.8	Most-significant bit for 9-bit EGT timer. See EGT below.
BGT.6	–	
BGT.5	–	
BGT.4	BGT.4	Time in ETUs between the start bit of the last received character to start bit of the first character transmitted to the smart card. Default value is 22.
BGT.3	BGT.3	
BGT.2	BGT.2	
BGT.1	BGT.1	
BGT.0	BGT.0	

Extra Guard Time Register (EGT): 0xFE17 ← 0x0C

This register contains the Extra Guard Time Value (EGT) least-significant byte. The Extra Guard Time indicates the minimum time between the leading edges of the start bit of consecutive characters. The delay is depends on the T=0/T=1 mode. Used in transmit mode.

Table 97: The EGT Register

MSB							LSB
EGT.7	EGT.6	EGT.5	EGT.4	EGT.3	EGT.1	EGT.2	EGT.0

Bit	Function
EGT.7	Time in ETUs between start bits of consecutive characters. In T=0 mode, the minimum is 1. In T=0, the leading edge of the next start bit may be delayed if there is a break detected from the smart card. Default value is 12. In T=0 mode, regardless of the value loaded, the minimum value is 12, and for T=1 mode, the minimum value is 11.
EGT.6	
EGT.5	
EGT.4	
EGT.3	
EGT.2	
EGT.1	
EGT.0	

Block Wait Time Registers (BWTB0): 0xFE1B ← 0x00, (BWTB1): 0xFE1A ← 0x00, (BWTB2): 0xFE19 ← 0x00, (BWTB3): 0xFE18 ← 0x00

Table 98: The BWTB0 Register

MSB							LSB
BWT.7	BWT.6	BWT.5	BWT.4	BWT.3	BWT.1	BWT.2	BWT.0

Table 99: The BWTB1 Register

MSB							LSB
BWT.15	BWT.14	BWT.13	BWT.12	BWT.11	BWT.10	BWT.9	BWT.8

Table 100: The BWTB2 Register

MSB							LSB
BWT.23	BWT.22	BWT.21	BWT.20	BWT.19	BWT.18	BWT.17	BWT.16

Table 101: The BWTB3 Register

MSB							LSB
–	–	–	–	BWT.27	BWT.26	BWT.25	BWT.24

These registers (BWTB0, BWTB1, BWTB2, BWTB3) are used to set the Block Waiting Time(27:0) (BWT). All of these parameters define the maximum time the 73S1209F will have to wait for a character from the smart card. These registers serve a dual purpose. When T=1, these registers are used to set up the block wait time. The block wait time defines the time in ETUs between the beginning of the last character sent to smart card and the start bit of the first character received from smart card. It can be used to detect an unresponsive card and should be loaded by firmware prior to writing the last TX byte. When T = 0, these registers are used to set up the work wait time. The work wait time is defined as the time between the leading edge of two consecutive characters being sent to or from the card. If a timeout occurs, an interrupt is generated to the firmware. The firmware can then take appropriate action. A Wait Time Extension (WTX) is supported with the 28-bit BWT.

Character Wait Time Registers (CWTB0): 0xFE1D ← 0x00, (CWTB1): 0xFE1C ← 0x00

Table 102: The CWTB0 Register

MSB							LSB
CWT.7	CWT.6	CWT.5	CWT.4	CWT.3	CWT.1	CWT.2	CWT.0

Table 103: The CWTB1 Register

MSB							LSB
CWT.15	CWT.14	CWT.13	CWT.12	CWT.11	CWT.10	CWT.9	CWT.8

These registers (CWTB0, CWTB1) are used to hold the Character Wait Time(15:0) (CWT) or Initial Waiting Time(15:0) (IWT) depending on the situation. Both the IWT and the CWT measure the time in ETUs between the leading edge of the start of the current character received from the smart card and the leading edge of the start of the next character received from the smart card. The only difference is the mode in which the card is operating. When T=1 these registers are used to configure the CWT and these registers configure the IWT when the ATR is being received. These registers should be loaded prior to receiving characters from the smart card. Firmware must manage which time is stored in the register. If a timeout occurs, an interrupt is generated to the firmware. The firmware can then take appropriate action.

3.3 Digital IO Characteristics

These requirements pertain to digital I/O pin types with consideration of the specific pin function and configuration. The LED(1:0) pins have pull-ups that may be enabled. The Row pins have 100KΩ pull-ups.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Voh	Output level, high	Ioh =-2mA	0.8 *VDD		VDD	V
Vol	Output level, low	Iol=2mA	0		0.3	V
Vih	Input voltage, high	2.7v < VDD <3.6v	1.8		VDD+0.3	V
Vil	Input voltage, low	2.7v < VDD <3.6v	-0.3		0.6	V
Ileak	Leakage current	0 < Vin < VDD All output modes disabled, pull-up/downs disabled	-5		5	μA
Ipu	Pull-up current	If provided and enabled, Vout < 0.1v	-5			μA
Ipd	Pull-down current	If provided and enabled, Vout > VDD – 0.1v			5	μA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Iled	LED drive current	Vout = 1.3V, 2.7v < VDD < 3.6v		2 4 10		mA
Iolkrow	Keypad Row output low current	0.0v < Voh < 0.1v when pull-up R is enabled			-100	μA
Iolkcol	Keypad column output high current	0.0v < Voh < 0.1v when col. is pulled low			-3	mA

3.4 Oscillator Interface Requirements

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
High-Frequency Oscillator (Xin) Parameters. XIN Is Used As Input For External Clock For Test Purposes Only. A Resistor Connecting X12in To X12out Is Required, Value = 1MΩ.						
VILX12IN	Input Low Voltage – X12IN		-0.3		0.3*VDD	V
VIHX12IN	Input High Voltage – X12IN		0.7*VDD		Vdd+.0.3	V
IILXTAL	Input Current – X12IN	GND < Vin < Vdd	-10		10	μA
Fxtal	Crystal resonant frequency	Fundamental mode	6		12	MHz

3.5 DC Characteristics: Analog Input

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
V_{THTOL}	Voltage Threshold Tolerance	Selected Threshold Value	-3%		+3%	V

3.7 DC Characteristics

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
I_{DD}	Supply Current	CPU clock @ 24MHz		20	25	mA
		CPU clock @ 12MHz		14	20	mA
		CPU clock @ 6MHz		10	15	mA
		CPU clock @ 3.69MHz		9	14	mA
		Power down (-40° to 85°C)		8	50	µA
		Power down (25°C)		6	13	µA
I_{PC}	Supply Current	V_{CC} on, ICC=0 I/O, AUX1, AUX2=high, CLK not toggling		450	650	µA
		Power down		1	10	
I_{PCOFF}	V_{PC} supply current when V_{CC} = 0	Smart card deactivated		345		µA

3.8 Voltage / Temperature Fault Detection Circuits

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
V_{PCF}	V_{PC} fault (V_{PC} Voltage supervisor threshold)	V_{PC}<V_{CC}, a transient event		V_{CC} > V_{PC} + 0.3		V
V_{CCF}	VCCOK = 0 (V_{CC} Voltage supervisor threshold)	V_{CC} = 5V			4.6	V
		V_{CC}= 3V			2.7	V
		V_{CC}= 1.8V			1.65	
T_F	Die over temperature fault		115		145	°C
ICCF	Vcc over current fault		110			mA

4.2 Package Pin Designation (44-pin QFN)

CAUTION: Use handling procedures necessary for a static sensitive component

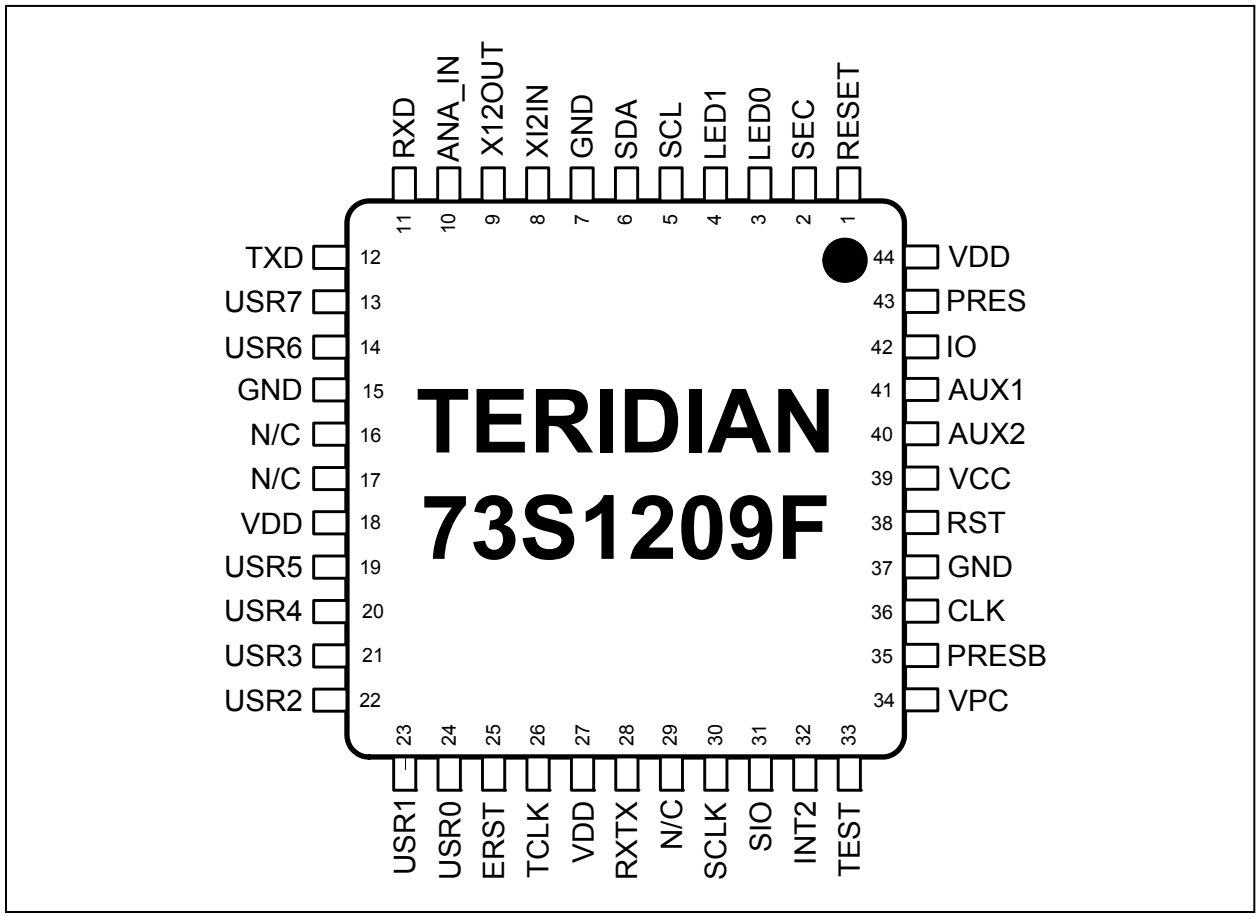


Figure 42: 73S1209F Pinout