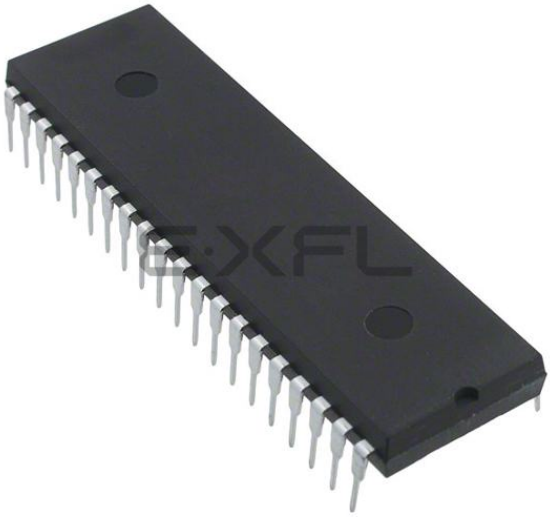

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Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	LED, POR
Number of I/O	32
Program Memory Size	3.75KB (3.75K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705sr3cpe

MC68HC05SR3
MC68HC705SR3

High-density Complementary Metal Oxide Semiconductor (HCMOS) Microcontroller Units

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The external oscillator clock frequency, f_{OSC}, is divided by two to produce the internal operating frequency, f_{OP}.

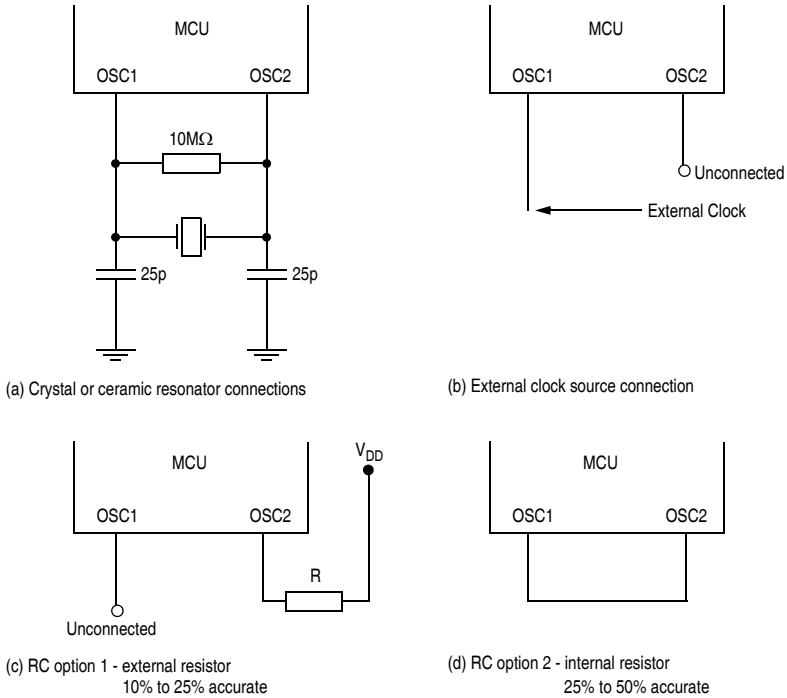


Figure 2-1 Oscillator Connections

2.2.1 Crystal Oscillator

The circuit in Figure 2-1(a) shows a typical oscillator circuit for an AT-cut, parallel resonant crystal. The crystal manufacturer's recommendations should be followed, as the crystal parameters determine the external component values required to provide maximum stability and reliable start-up. The load capacitance values used in the oscillator circuit design should include all stray capacitances. The crystal and components should be mounted as close as possible to the pins for start-up stabilization and to minimize output distortion. An external start-up resistor of approximately 10MΩ is needed between OSC1 and OSC2 for the crystal type oscillator.

2.2.2 External Clock

An external clock from another CMOS-compatible device can be connected to the OSC1 input, with the OSC2 input not connected, as shown in Figure 2-1(b).

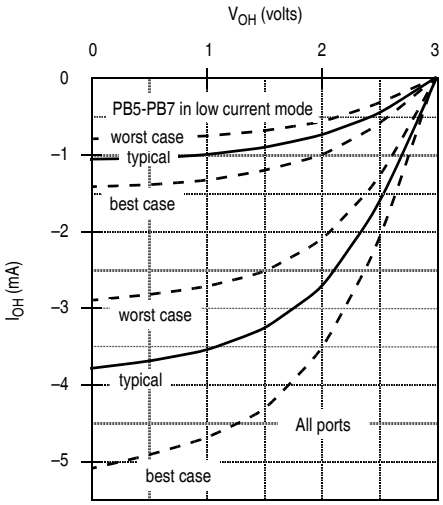


Figure 3-5 Typical I_{OL} vs V_{OL} @V_{DD}=3V

3.6 Programmable Pull-Up Devices

Ports B, C, and D have 20KΩ pull-up resistors, which can be connected or disconnected, by setting appropriate bits in the Port Option Register (at $0A).

3.6.1 Port Option Register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port Option Register (POPR)	$0A			PIL	PDP	PCP	PBP	PB1	PB0	0000 0000

PIL — PB5:PB7 current drive select

1 (set) – PB5-PB7 are configured to 2mA drive port.

0 (clear) – PB5-PB7 are configured to 10mA drive port.

PDP — Port D Pull-up

1 (set) – The internal 20KΩ pull-up resistors are connected to the inputs of Port D.

0 (clear) – No pull-up resistor is connected to the inputs of Port D.

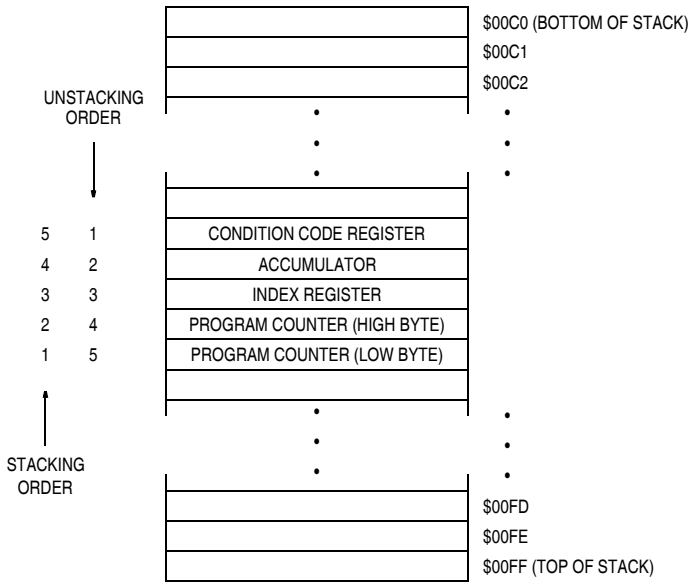


Figure 5-1 Interrupt Stacking Order

Table 5-1 Reset/Interrupt Vector Addresses

Register	Flag Name	Interrupt	CPU Interrupt	Vector Address	Priority
—	—	Reset	$\overline{\text{RESET}}$	$1FFE-$1FFF	highest
—	—	Software	SWI	$1FFC-$1FFD	
—	—	External Interrupt	$\overline{\text{IRQ}}$	$1FFA-$1FFB	
—	—	External Interrupt 2	$\overline{\text{IRQ2}}$	$1FF8-$1FF9	
TCR	TIF	Timer Overflow	TIF	$1FF6-$1FF7	
—	—	Keyboard	KBI	$1FF4-$1FF5	lowest

5.2.1 Non-maskable Software Interrupt (SWI)

The software interrupt (SWI) is an executable instruction and a non-maskable interrupt: it is execute regardless of the state of the I-bit in the CCR. If the I-bit is zero (interrupt enabled), SWI is executed after interrupts that were pending when the SWI was fetched, but before interrupts generated after the SWI was fetched. The SWI interrupt service routine address is specified by the contents of memory locations $1FFC and $1FFD.

TIF — Timer Interrupt Flag

1 (set) – A timer interrupt (timer overflow) has occurred.

0 (clear) – A timer interrupt (timer overflow) has not occurred.

The I-bit in the CCR must be cleared in order for the timer interrupt to be processed. The interrupt will vector to the interrupt service routine at the address specified by the contents in $1FF6-$0FF7.

5.2.2.4 Keyboard Interrupt (KBI)

Keyboard interrupt function is associated with Port A pins. The keyboard interrupt function is enabled by setting the keyboard interrupt enable bit KBIE (bit 7 of MCR at $0C) and the individual enable bits KBE0-KBE7 (bits 0-7 of KBIM at $0B). When the KBEx bit is set, the corresponding Port A pin will be configured as an input pin, regardless of the DDR setting, and a 20KΩ pull-up resistor is connected to the pin, as shown in Figure 5-4. When a high to low transition is sensed on the pin, a keyboard interrupt will be generated. An interrupt to the CPU will be generated if the I-bit in the CCR is cleared.

The keyboard interrupt flag should be cleared in the interrupt service routine (by writing a “1” to KBIC bit in the MCR at $0C) after the key is debounced. Debouncing will avoid spurious false triggering.

The keyboard interrupt is negative-edge sensitive only, and the interrupt service routine is specified by the contents in $1FF4-$1FF5.

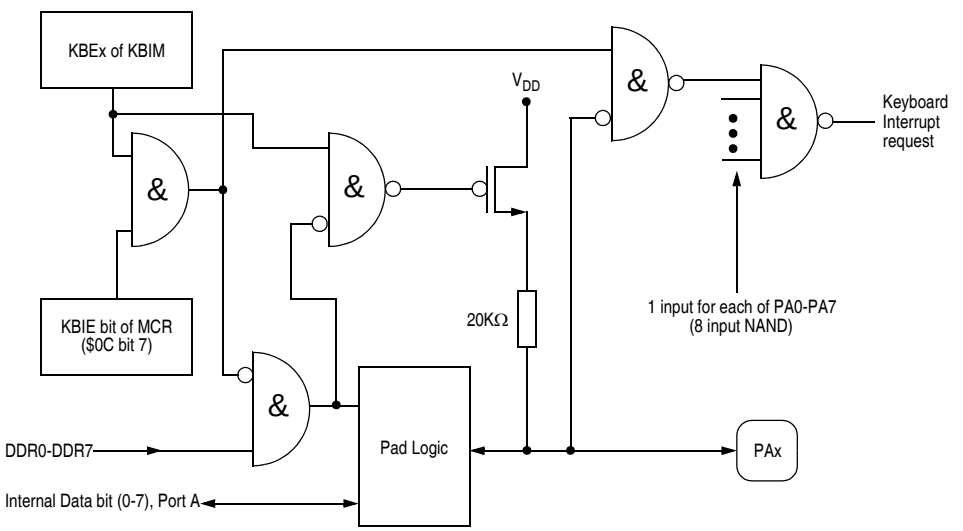
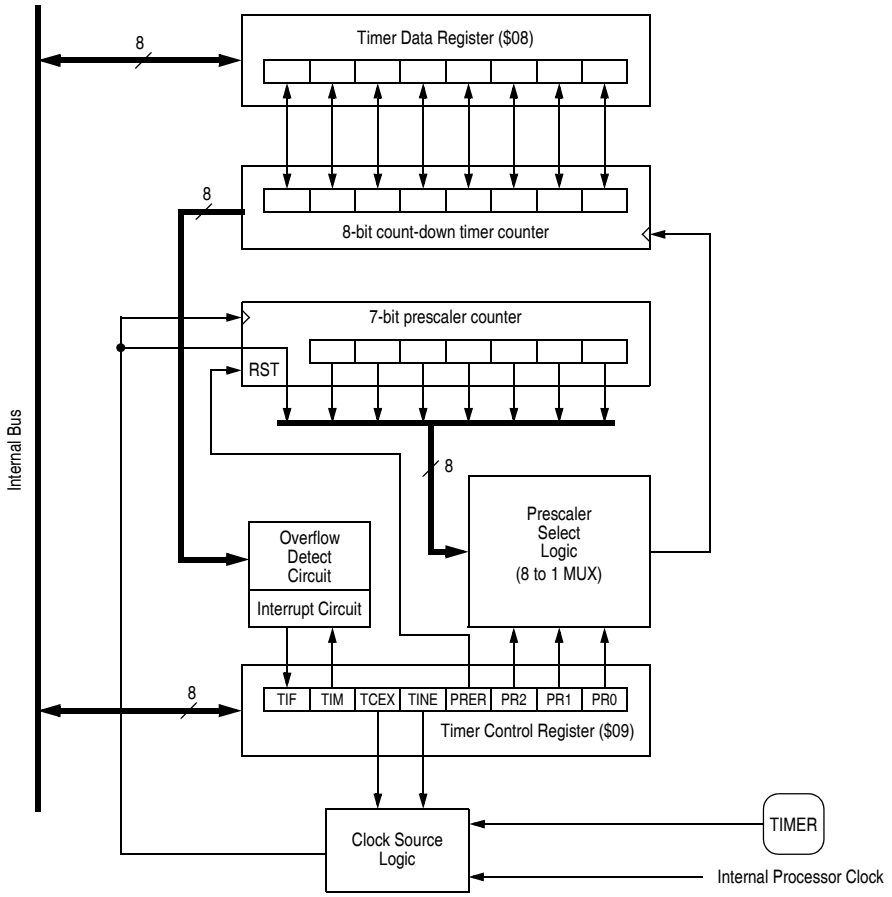


Figure 5-4 Keyboard Interrupt Circuitry



TCEX	TINE	Clock Source
0	0	Internal clock to timer
0	1	“AND” of internal clock and TIMER pin to timer
1	0	Input clock to timer disabled
1	1	TIMER pin to timer

Figure 6-1 Timer Block Diagram

PR2:PR0

These three bits enable the program to select the division ratio of the prescaler. On reset, these three bits are set to “100”, which corresponds to a division ratio of 16.

PR2	PR1	PR0	Divide Ratio
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

6.3 Timer Data Register (TDR)

The TDR is a read/write register which contains the current value of the 8-bit count-down timer counter when read. Reading this register does not disturb the counter operation.

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$08	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0	1111 1111

6.4 Operation during Low Power Modes

The timer ceases counting in STOP mode. When STOP mode is exited by an external interrupt ($\overline{\text{IRQ}}$ or $\overline{\text{IRQ2}}$), the internal oscillator will resume its operation, followed by internal processor stabilization delay. The timer is then cleared to zero and resumes its operation. The TIF bit in the TCR will be set. To avoid generating a timer interrupt when exiting STOP mode, it is recommended to set the TIM bit prior entering STOP mode. After exiting STOP mode TIF bit can then be cleared.

The CPU clock halts during the WAIT mode, but the timer remains active. If the interrupts are enabled, the timer interrupt will cause the processor to exit the WAIT mode.

8
CPU CORE AND INSTRUCTION SET

This section provides a description of the CPU core registers, the instruction set and the addressing modes of the MC68HC05SR3.

8.1 Registers

The MCU contains five registers, as shown in the programming model of Figure 8-1. The interrupt stacking order is shown in Figure 8-2.

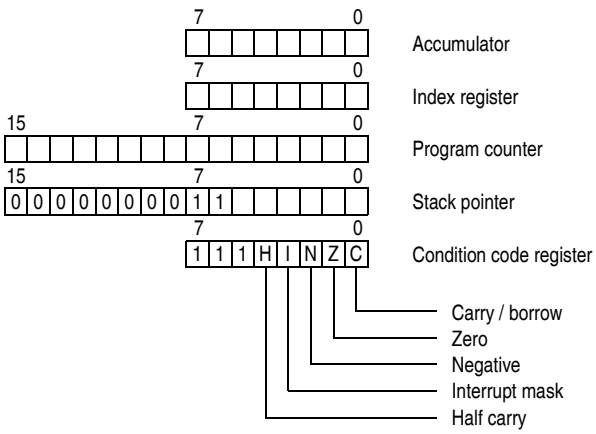


Figure 8-1 Programming model

8.1.1 Accumulator (A)

The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

8.2.1 Register/memory Instructions

Most of these instructions use two operands. The first operand is either the accumulator or the index register. The second operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 8-2 for a complete list of register/memory instructions.

8.2.2 Branch instructions

These instructions cause the program to branch if a particular condition is met; otherwise, no operation is performed. Branch instructions are two-byte instructions. Refer to Table 8-3.

8.2.3 Bit manipulation instructions

The MCU can set or clear any writable bit that resides in the first 256 bytes of the memory space (page 0). All port data and data direction registers, timer and serial interface registers, control/status registers and a portion of the on-chip RAM reside in page 0. An additional feature allows the software to test and branch on the state of any bit within these locations. The bit set, bit clear, bit test and branch functions are all implemented with single instructions. For the test and branch instructions, the value of the bit tested is also placed in the carry bit of the condition code register. Refer to Table 8-4.

8.2.4 Read/modify/write instructions

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to this sequence of reading, modifying and writing, since it does not modify the value. Refer to Table 8-5 for a complete list of read/modify/write instructions.

8.2.5 Control instructions

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to Table 8-6 for a complete list of control instructions.

8.2.6 Tables

Tables for all the instruction types listed above follow. In addition there is a complete alphabetical listing of all the instructions (see Table 8-7), and an opcode map for the instruction set of the M68HC05 MCU family (see Table 8-8).

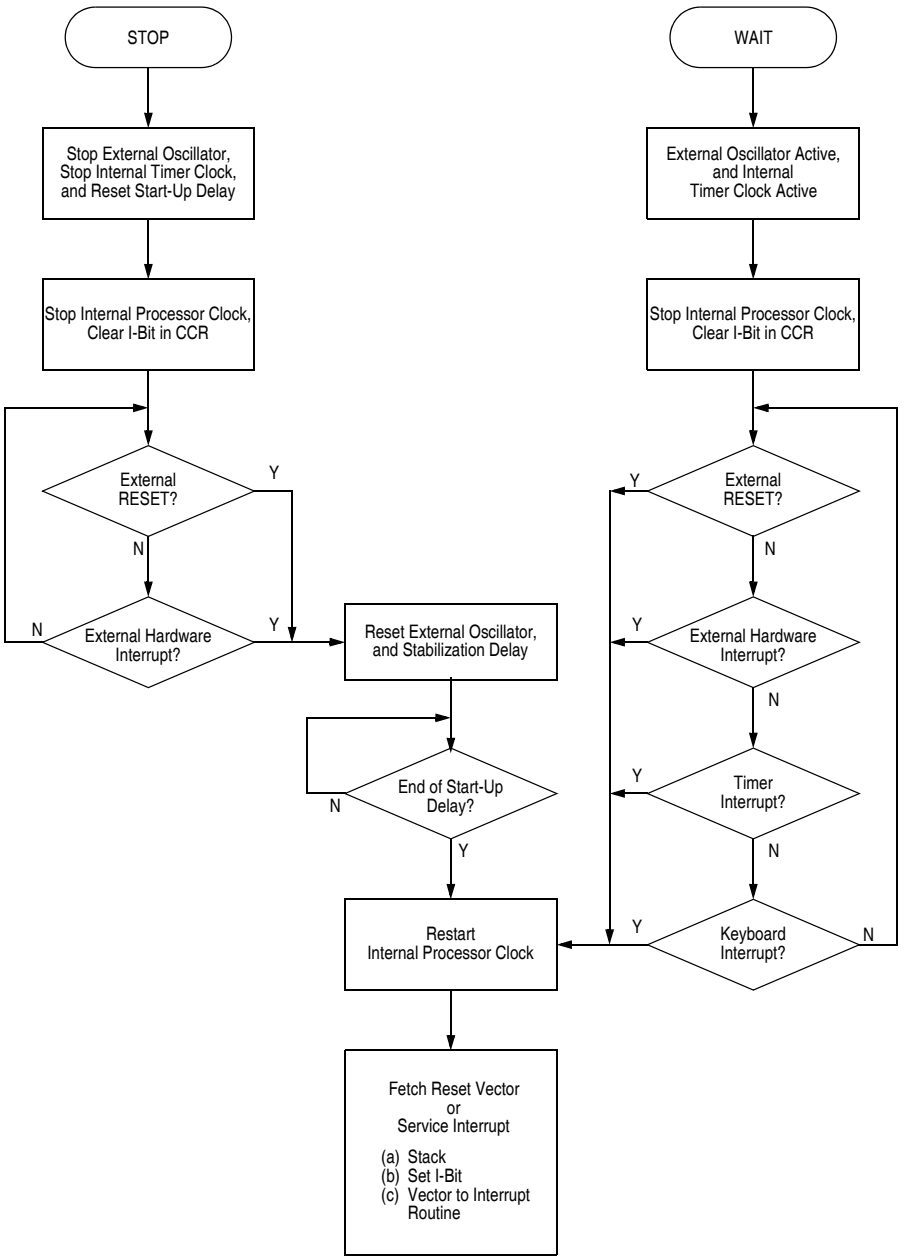


Figure 9-1 STOP and WAIT Mode Flowcharts

9.3 SLOW Mode

The SLOW mode function is controlled by the SM bit in the Miscellaneous Control Register. When the SM bit is set, the internal bus clock is divided by 16, resulting to a frequency equal to the oscillator frequency divide by 32. This feature permits a slow down of all the internal operations and thus reduces power consumption — particularly useful while in WAIT mode. The SM bit is automatically cleared while going to STOP mode.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous Control Register	$0C	KBIE	KBIC	INTO	INTE	LVRE	SM	IRQ2F	IRQ2E	0001 0000

SM — Slow Mode

1 (set) – Slow mode enabled. Internal bus frequency $f_{OP}=f_{OSC} \div 32$.

0 (clear) – Slow mode disabled. Internal bus frequency $f_{OP}=f_{OSC} \div 2$.

9.4 Data-Retention Mode

If the Low Voltage Reset function is not enabled, the contents of RAM and CPU registers are retained at supply voltages as low as 2Vdc. This is called the data-retention mode where the data is held, but the device is not guaranteed to operate. The $\overline{\text{RESET}}$ pin must be held low during data-retention mode.

The Low Voltage Reset Function is enabled/disabled by the LVRE bit in the Miscellaneous Control Register ($0C).

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous Control Register	$0C	KBIE	KBIC	INTO	INTE	LVRE	SM	IRQ2F	IRQ2E	0001 0000

LVRE — Low Voltage Reset Enable

1 (set) – Low Voltage Reset function enabled.

0 (clear) – Low Voltage Reset function disabled.

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11.4 ADC Electrical Characteristics

Table 11-3 ADC Electrical Characteristics for 5V and 3V Operation

CHARACTERISTICS	PARAMETER	MINIMUM	MAXIMUM	UNIT
Resolution	Number of bits resolved by the ADC	8	8	bits
Absolute accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary code output code for all errors.(1)	— —	±1.5 (V_{DD}=5V) ±2 (V_{DD}=3.3V)	LSB LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
Power-up time	ADC power-up time delay, t_{ADON}	—	500	µs
V_{RH}	Maximum analog reference voltage	V_{RL}	V_{DD}+0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS}–0.1	V_{RH}	V
Conversion time	Total time to perform a single analog to digital conversion (a) External clock (OSC1, OSC2) (b) Internal RC oscillator	 — —	 32 32	 t_{CYC} t_{CYC}
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	Inherent (within total error)		
Zero-input reading	Conversion result when V_{IN}=V_{RL}	00	—	hex
Full-scale reading	Conversion result when V_{IN}=V_{RH}	—	FF	hex
Sample acquisition time	Analog input acquisition sampling(2) (a) External clock (OSC1, OSC2) (b) Internal RC oscillator	 — —	 12 12	 t_{CYC} µs
Input capacitance	Input capacitance on AN0-AN3	—	8	pF
Input leakage	Input leakage on ADC pins(3) AN0, AN1, AN2, AN3, V_{RL}, V_{RH}	—	±400	nA

Notes:

(1) Error includes quantization. ADC accuracy may decrease proportionately as V_{DD} is reduced below 3.0V.

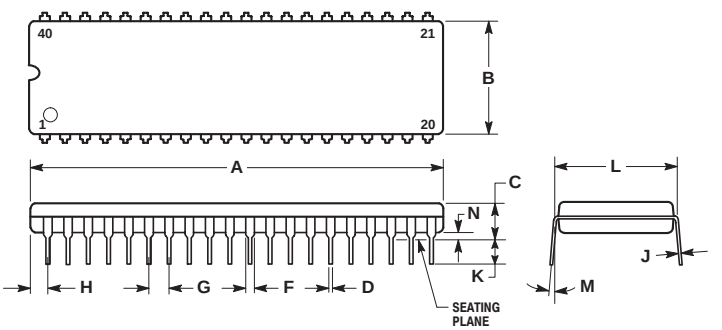
(2) Source impedances greater than 10KΩ adversely affect internal RC charging time during input sampling.

(3) The external system error caused by input leakage current is approximately equal to the product of R source and input current.

12
MECHANICAL SPECIFICATIONS

This section provides the mechanical dimensions for the 40-pin DIP, 42-pin SDIP and 44-pin QFP packages for the MC68HC05SR3.

12.1 40-Pin DIP Package (Case 711-03)

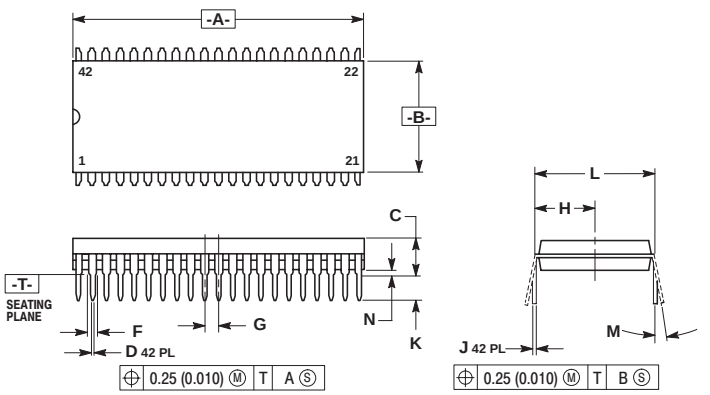


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

Figure 12-1 40-pin DIP Package

12.2 42-Pin SDIP Package (Case 858-01)



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

Figure 12-2 42-pin SDIP Package

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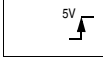
A.2 Modes of Operation

The MC68HC705SR3 has two modes of operation – user mode and EPROM bootstrap mode. Table A-1 shows the conditions required to enter each mode on the rising edge of $\overline{\text{RESET}}$.

Table A-1 MC68HC705SR3 Operating Mode Entry Conditions

$\overline{\text{RESET}}$	V_{PP}	PB1	MODE
	V_{SS} to V_{DD}	V_{SS} to V_{DD}	USER
	V_{TST}	V_{DD}	BOOTSTRAP

$V_{TST}=2\times V_{DD}$

A.3 User Mode

The normal operating mode of the MC68HC705SR3 is the user mode. User mode will be entered on the rising edge of $\overline{\text{RESET}}$ when the V_{PP} and PB1 pins are between V_{SS} and V_{DD}.

Warning: In the MC68HC705SR3, all vectors are fetched from EPROM in user mode; therefore, the EPROM must be programmed (via the bootstrap mode) before the device is powered up in user mode.

A.4 Bootstrap Mode

The bootstrap mode is provided as a mean of self-programming MC68HC705SR3 EPROM with minimal circuitry, and can only run in the crystal oscillator mode. Bootstrap mode will be entered on the rising edge of RESET when the V_{PP} pin is at V_{TST} ($2\times V_{DD}$) and PB1 pin is at V_{DD}. Once in the bootstrap mode, PB1 can then be used for other purposes. After entering the bootstrap mode, CPU branches to the bootstrap program and carries out the EPROM programming routine. The user EPROM consists of 3840 bytes, from location $1000 to $1EFF.

This program handles copying of user code from an external EPROM into the on-chip EPROM. The bootstrap function does not have to be done from an external EPROM, but it may be done from a host.

The user code must be a one-to-one correspondence with the internal EPROM addresses.

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