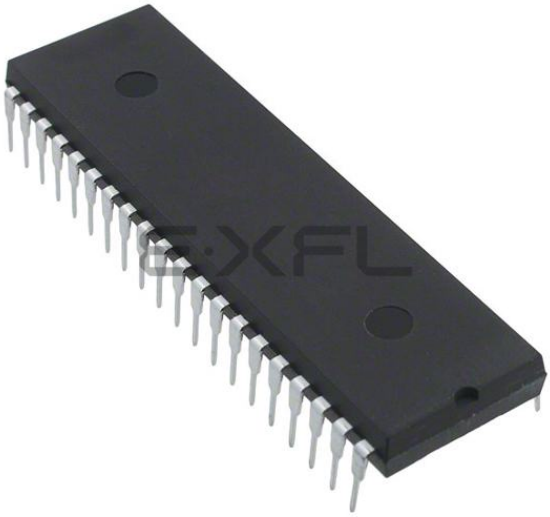

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	LED, POR
Number of I/O	32
Program Memory Size	3.75KB (3.75K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705sr3pe

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MC68HC705SR3

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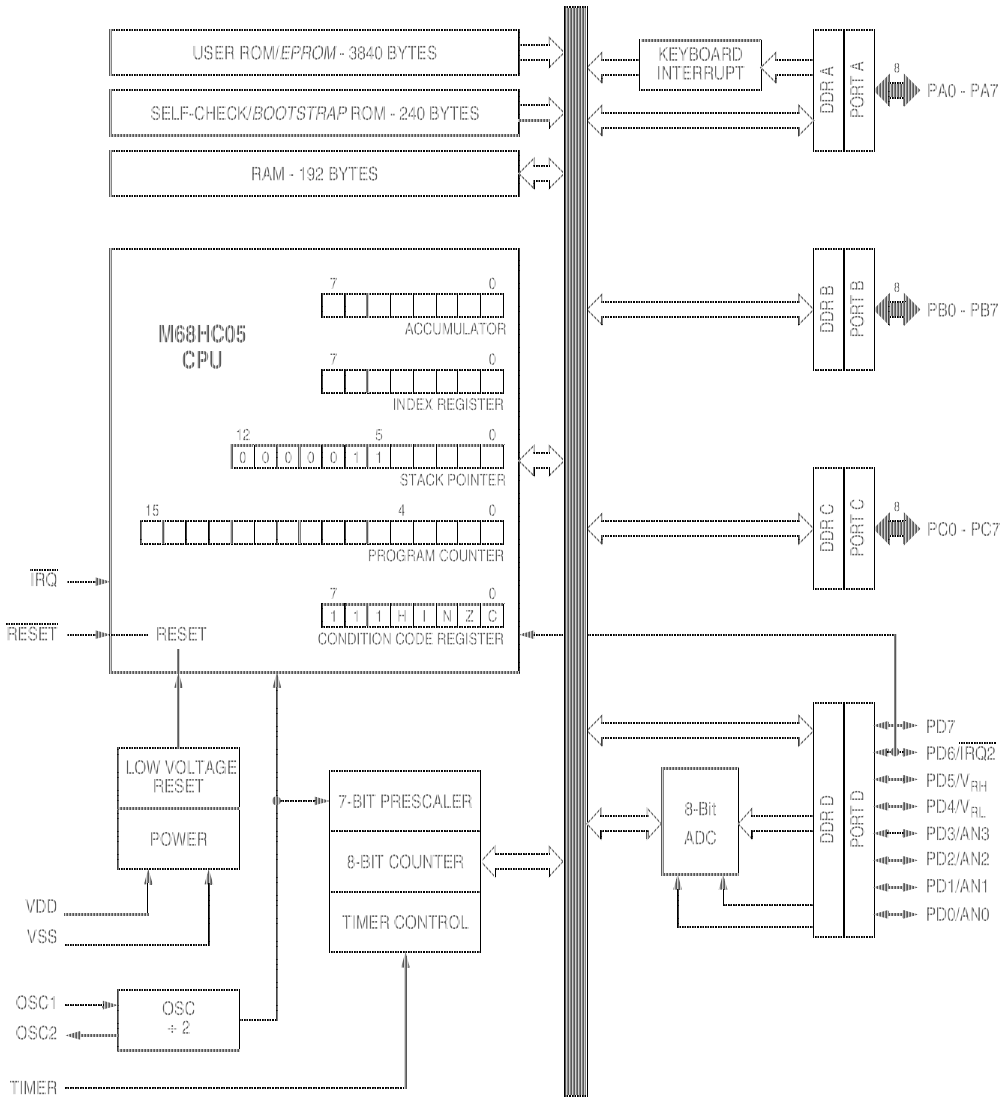

Figure 1-1 MC68HC05SR3/*MC68HC705SR3* Block Diagram

3
INPUT/OUTPUT PORTS

The MC68HC05SR3 has 32 bidirectional I/O lines, arranged as four 8-bit I/O ports (Port A, B, C, and D). The individual bits in these ports are programmable as either inputs or outputs under software control by the Data Direction Registers (DDRs). All port pins each has an associated 20KΩ pull-up resistor, which can be connected/disconnected under software control. Also, each port pin is capable of sinking and driving a maximum current of 10mA (e.g. direct drive for LEDs). Port A can also be configured for keyboard interrupts.

3.1 Parallel Ports

Port A, B, C, and D are 8-bit bidirectional ports. Each Port pin is controlled by the corresponding bits in a Data Direction Register and a Data Register as shown in Figure 3-1. The functions of the I/O pins are summarized in Table 3-1.

Table 3-1 I/O Pin Functions

R/$\overline{W}$	DDR	I/O Pin Function
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in an output mode. The output data latch is read.

3.1.1 Port Data Registers

Each Port I/O pin has a corresponding bit in the Port Data Register. When a Port I/O pin is programmed as an output the state of the corresponding data register bit determines the state of the output pin. All Port I/O pins can drive a current of 10mA when programmed as outputs. When a Port pin is programmed as an input, any read of the Port Data Register will return the logic state of the corresponding I/O pin. The locations of the Data Registers for Port A, B, C, and D are at $00, $01, $02, and $03 respectively. The Port Data Registers are unaffected by reset.

5
RESETS AND INTERRUPTS

This section describes the reset and interrupt functions on the MCU.

5.1 RESETS

The MC68HC05SR3 can be reset in three ways:

- by initial power-on reset function, (POR),
- by an active low input to the $\overline{\text{RESET}}$ pin, ($\overline{\text{RESET}}$), and
- by a Low Voltage Reset, (LVR).

All of these resets will cause the program to go to the starting address, specified by the contents of memory locations $1FFE and $1FFF, and cause the interrupt mask (I-bit) of the Condition Code Register (CCR) to be set.

5.1.1 Power-On Reset (POR)

The power-on reset (POR) occurs on power-up to allow the clock oscillator to stabilize. The POR is strictly for power-up conditions, and should not be used to detect any drops in power supply voltage.

There is an oscillator stabilization delay of t_{PORL} internal processor bus clock cycles after the oscillator becomes active. The $\overline{\text{RESET}}$ pin will be pulled down internally during these cycles. If the $\overline{\text{RESET}}$ pin is low (by external circuit) at the end of the t_{PORL} period, the processor remains in the reset condition until $\overline{\text{RESET}}$ goes high.

5.1.2 $\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ input pin is used to reset the MCU to provide an orderly software start-up procedure. When using the external reset, the $\overline{\text{RESET}}$ pin must stay low for a minimum of $1.5t_{CYC}$. The $\overline{\text{RESET}}$ pin is connected to a Schmitt Trigger circuit as part of its input to improve noise immunity.

5.1.3 Low Voltage Reset (LVR)

When the LVR function is enabled, an internal reset is generated if the supply voltage, V_{DD}, drops below V_{LVR}. (See Section 11 for value of V_{LVR}).

This LVR function is enabled by setting the LVRE bit in the Miscellaneous Control Register.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous Control Register	$0C	KBIE	KBIC	INTO	INTE	LVRE	SM	IRQ2F	IRQ2E	0001 0000

LVRE — Low Voltage Reset Enable

1 (set) – Low Voltage Reset function enabled.

0 (clear) – Low Voltage Reset function disabled.

Note: The LVR function should not be enabled when operating V_{DD}=3V.

5.2 INTERRUPTS

The MC68HC05SR3 MCU can be interrupted by different sources – four maskable hardware interrupt and one non-maskable software interrupt:

- Software Interrupt Instruction (SWI)
- External signal on $\overline{\text{IRQ}}$ pin
- External signal on $\overline{\text{IRQ2}}$ pin
- TImer Overflow
- Keyboard

If the interrupt mask bit (I-bit) in the Condition Code Register (CCR) is set, all maskable interrupts are disabled. Clearing the I-bit enables interrupts.

Interrupts cause the processor to save the register contents on the stack and to set the interrupt mask (I-bit) to prevent additional interrupts. The RTI instruction causes the register contents to be recovered from the stack and normal processing to resume.

Unlike reset, hardware interrupts do not cause the current instruction execution to be halted, but are considered pending until the current instruction is complete. The current instruction is the one already fetched and being operated on. When the current instruction is complete, the processor checks all pending hardware interrupts. If interrupts are not masked (CCR I-bit clear) the processor proceeds with interrupt processing; otherwise, the next instruction is fetched and executed. Table 5-1 shows the relative priority of all the possible interrupt sources. Figure 5-2 shows the interrupt processing flow.

6
TIMER

This section describes the operation of the 8-bit count-down timer in the MC68HC05SR3.

6.1 Timer Overview

The MC68HC05SR3 timer block diagram is shown in Figure 6-1. The timer contains a single 8-bit software programmable count-down counter with a 7-bit software selectable prescaler. The counter may be preset under software control and decrements towards zero. When the counter decrements to zero, the timer interrupt flag (TIF bit in Timer Control Register, TCR) is set. Once timer interrupt flag is set, an interrupt is generated to the CPU only if the TIM bit in the TCR and I-bit in the CCR are cleared. When a interrupt is recognized, after completion of the current instruction, the processor proceeds to store the appropriate registers on the stack and then fetches the timer interrupt vector from locations $1FF6 and $1FF7.

The counter continues to count after it reaches zero, allowing the software to determine the number of internal or external clocks since the timer interrupt flag was set. The counter may be read at any time by the processor without disturbing the count. The contents of the counter become stable prior to the read portion of a cycle and do not change during the read. The timer interrupt flag remains set until cleared by the software. If a write occurs before the timer interrupt is served, the interrupt is lost. The timer interrupt flag may also be used as a scanned status bit in a non-interrupt mode of operation.

The prescaler is a 7-bit divider which is used to extend the maximum length of the timer. Bit 0, 1, 2 (PR0, PR1, PR2) of TCR are programmed to choose the appropriate prescaler output which is used as the 8-bit counter clock input. The processor cannot write into or read from the prescaler; however, its contents can be cleared to all zeros by writing to the PRER bit in the TCR. This will allow for truncation-free counting.

The input clock for the timer sub-system is selectable from internal, external, or a combination of internal and external sources. The TCEX and TINE bits in the Timer Control Register selects the timer input clock.

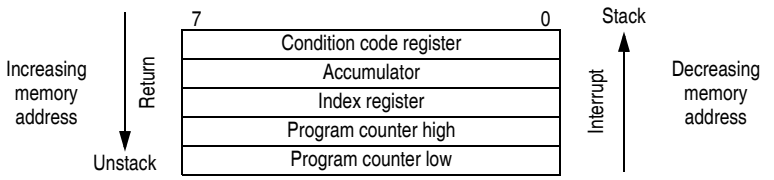

Figure 8-2 Stacking order

8.1.2 Index register (X)

The index register is an 8-bit register, which can contain the indexed addressing value used to create an effective address. The index register may also be used as a temporary storage area.

8.1.3 Program counter (PC)

The program counter is a 16-bit register, which contains the address of the next byte to be fetched.

8.1.4 Stack pointer (SP)

The stack pointer is a 16-bit register, which contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location $00FF. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

When accessing memory, the ten most significant bits are permanently set to 0000000011. These ten bits are appended to the six least significant register bits to produce an address within the range of $00C0 to $00FF. Subroutines and interrupts may use up to 64 (decimal) locations. If 64 locations are exceeded, the stack pointer wraps around and overwrites the previously stored information. A subroutine call occupies two locations on the stack; an interrupt uses five locations.

8.1.5 Condition code register (CCR)

The CCR is a 5-bit register in which four bits are used to indicate the results of the instruction just executed, and the fifth bit indicates whether interrupts are masked. These bits can be individually tested by a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.

Half carry (H)

This bit is set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

9
LOW POWER MODES

The MC68HC05SR3 has three low-power operating modes. The WAIT and STOP instructions provide two modes that reduce the power required for the MCU by stopping various internal clocks and/or the on-chip oscillator. The flow of the STOP and WAIT modes is shown in Figure 9-1. The third low-power operating mode is the SLOW mode.

9.1 STOP Mode

Execution of the STOP instruction places the MCU in its lowest power consumption mode. In the STOP mode the internal oscillator is turned off, halting all internal processing.

When the CPU enters STOP mode the I-bit in the Condition Code Register is cleared automatically, so that any hardware interrupts ($\overline{\text{IRQ}}$, $\overline{\text{IRQ2}}$ and KBI) can “wake” the MCU. All other registers and memory contents remain unaltered. All input/output lines remain unchanged.

The MCU can be brought out of the STOP mode only by a hardware interrupt or an externally generated reset. When exiting the STOP mode the internal oscillator will resume after a pre-defined number of internal processor clock cycles, due to oscillator stabilization.

9.2 WAIT Mode

The WAIT instruction places the MCU in a low-power mode, but consumes more power than the STOP mode. In the WAIT mode the internal processor clock is halted, suspending all processor and internal bus activities. Other Internal clocks remain active, permitting interrupts to be generated from the Timer. The Timer may be used to generate a periodic exit from the WAIT mode or, in conjunction with the external Timer pin, on the occurrence of external events. Execution of the WAIT instruction automatically clears the I-bit in the Condition Code Register, so that any hardware interrupt can “wake” the MCU. All other registers, memory, and input/output lines remain in their previous states.

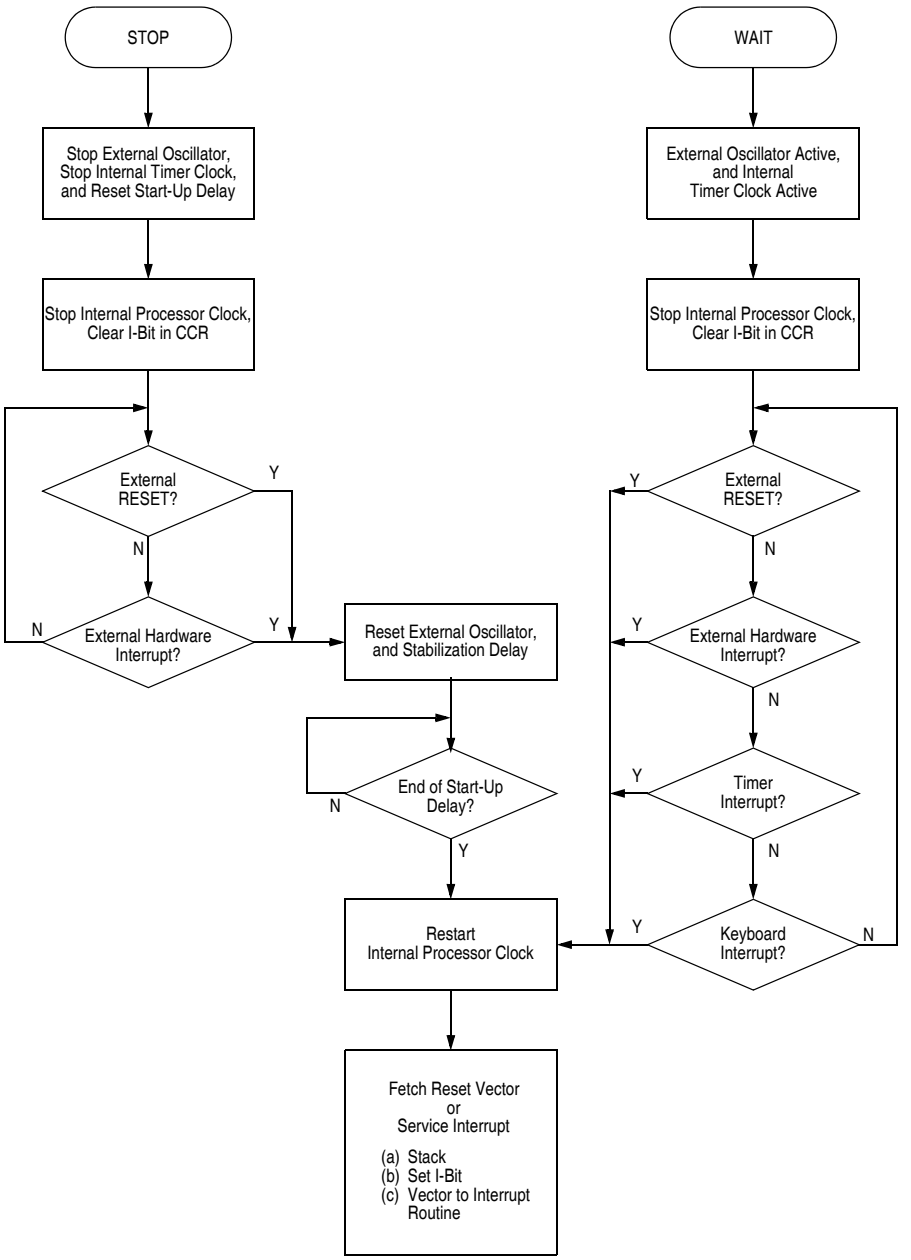

Figure 9-1 STOP and WAIT Mode Flowcharts

Table 11-2 DC Electrical Characteristics for 3V Operation

(V_{DD}=3.0Vdc ±10%, V_{SS}=0Vdc, temperature range=0 to 70°C)

CHARACTERISTICS	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
Output voltage I_{LOAD} = –10μA I_{LOAD} = +10μA	 V_{OH} V_{OL}	 V_{DD}–0.1 —	 — —	 — 0.1	 V V
Output high voltage (I_{LOAD}=–0.8mA) All Ports	V_{OH}	V_{DD}–0.3	—	—	V
Output low voltage (I_{LOAD}=+1.6mA) All Ports	V_{OL}	—	0.1	0.3	V
Output high current (V_{OH}=1.0V) All ports	I_{OH}	2.7	3.5	4.7	mA
Output low current (V_{OL}=2.0V) All ports	I_{OL}	3.0	4.0	5.2	mA
Total I/O port current Either source or sink	I_{PORT}	—	100	—	mA
Input high voltage PA0-PA7, PB0, PB1, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}	0.7×V_{DD}	—	V_{DD}	V
Input low voltage PA0-PA7, PB0, PB1, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2×V_{DD}	V
Supply current: Run Wait Stop 25°C 0°C to +70°C (Standard) –40°C to +85°C (Extended)	 I_{DD}	 — — — — —	 2.4 0.75 — — —	 3.5 1.5 20 30 40	 mA mA μA μA μA
I/O ports high-Z leakage current PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7	I_{IL}	—	—	±10	μA
Input current $\overline{RESET}$, $\overline{IRQ}$, OSC1	I_{IN}	—	—	±1	μA
Capacitance Ports (as input or output) $\overline{RESET}$, $\overline{IRQ}$, OSC1, OSC2	 C_{OUT} C_{IN}	 — —	 — —	 12 8	 pF pF
Pull-up resistor PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7 $\overline{RESET}$, $\overline{IRQ}$	R_{PU}	 14 85	 36 100	 50 176	 KΩ KΩ

Notes:
(1) All values shown reflect average measurements.

(2) Typical values at midpoint of voltage range, 25°C only.

(3) Wait I_{DD}: Only timer system active.

(4) Wait, Stop I_{DD}: All ports configured as inputs, V_{IL}=0.2Vdc, V_{IH}=V_{DD}–0.2Vdc.

(5) Run (operating) I_{DD}, Wait I_{DD}: Measured using external square wave clock source to OSC1 (f_{OSC}=2.0MHz), all inputs 0.2Vdc from rail; no DC loads, less than 50pF on all outputs, C_L=20pF on OSC2.

(6) Stop I_{DD} measured with OSC1=V_{SS}.

(7) Wait I_{DD} is affected linearly by the OSC2 capacitance.

A
MC68HC705SR3

This appendix summarizes the differences between the MC68HC05SR3 and MC68HC705SR3. The same information can also be found in appropriate sections of the book.

The MC68HC705SR3 is an EPROM version of the MC68HC05SR3. The 3840 bytes of user ROM in the MC68HC05SR3 are replaced by 3840 bytes of user EPROM.

A.1 Features

- Functionally equivalent to MC68HC05SR3
- 3840 bytes of user EPROM
- EPROM bootstrap mode replaces Self-Check mode on the MC68HC05SR3
- Available in the following packages: OTP 40-pin PDIP, windowed EPROM 40-pin Ceramic DIP, OTP 42-pin SDIP, and 44-pin QFP

```
CLR    PCR          ;reset PCR
LDX    #$00         ;load index register with 00
BSET   1,PCR        ;set ELAT bit
LDA    #$00         ;load data=00 in to A
STA    $1900,X      ;latch data and address
BSET   0,PCR        ;program
JSR    DELAY        ;call delay subroutine for 1ms
CLR    PCR          ;reset PCR
```

A.5 Mask Option Register (MOR)

The Mask Option Register (MOR) contains programmable EPROM bits to control mask options, and cannot be changed in User mode. The erased state are zeros. This register is latched upon reset going away.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Mask Option Register (MOR)	$0FFF			SMD	SEC	TMR2	TMR1	TMR0	RC	unaffected

SMD — SLOW Mode at Power-on

When programmed to “1”, this bit enables SLOW mode at power-up. Operating frequency, $f_{OP}=f_{OSC}\div2\div16=f_{OSC}\div32$.

SEC — EPROM Security

When programmed to “1”, this bit disables some functions of the Bootstrap mode, preventing external reading of EPROM content.

TMR2:TMR0 — Power-on Reset Delay

The amount Power-On Reset delay is set by programming these three bits. The delay is selected as follows:

TMR2	TMR1	TMR0	Delay (Instruction Cycles)
0	0	0	256
0	0	1	512
0	1	0	1024
0	1	1	2048
1	0	0	4096
1	0	1	8192
1	1	0	16384
1	1	1	32768

RC — RC or Crystal Oscillator Option

1 (set) – Resistor option selected.

0 (clear) – Crystal option selected.

A.6 Pin Assignments

See Section 2.3 for pin assignments for the available packages.

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