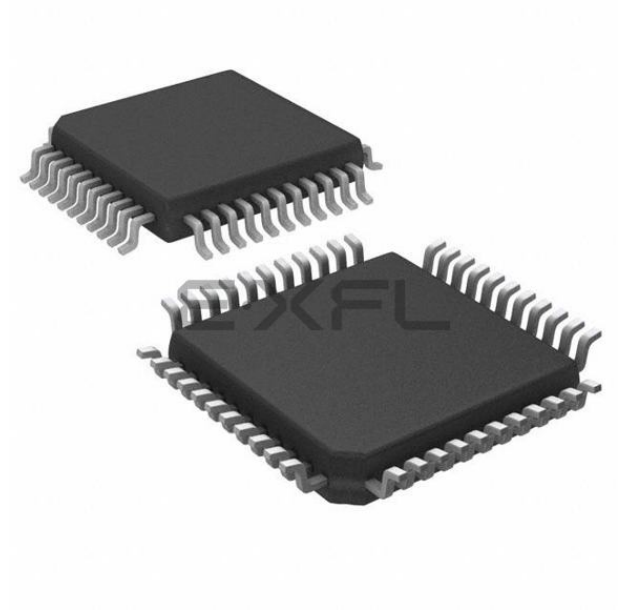

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	LED, POR
Number of I/O	32
Program Memory Size	3.75KB (3.75K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-QFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc705sr3cfbe

MC68HC05SR3
MC68HC705SR3

High-density Complementary Metal Oxide Semiconductor (HCMOS) Microcontroller Units

LIST OF FIGURES

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1
GENERAL DESCRIPTION

The MC68HC05SR3 HCMOS microcontroller is a member of the M68HC05 family of low-cost single-chip microcontrollers. This 8-bit microcontroller unit (MCU) contains on-chip oscillator, CPU, RAM, ROM, I/O, Timer, and Analog-to-Digital Converter. The MC68HC05SR3 is pin compatible with the MC6805R3 and is provided as a low power upgrade path for MC6805R3 applications. The low power advantage of CMOS is combined with the addition of I/O and port modifications which help eliminate external components in cost sensitive applications.

The MC68HC705SR3 is an EPROM version of the MC68HC05SR3; it is available in windowed and OTP packages. All references to the MC68HC05SR3 apply equally to the MC68HC705SR3, unless otherwise stated. *References specific to the MC68HC705SR3 are italicized in the text and also, for quick reference, they are summarized in Appendix A.*

1.1 Features

- Fully static chip design featuring the industry standard 8-bit M68HC05 core
- Pin compatible with the MC6805R3
- Power saving STOP, WAIT, and SLOW modes
- 3840 bytes of user ROM with security feature in MC68HC05SR3
  3840 bytes of EPROM with security bit in MC68HC705SR3
- 192 bytes of RAM (64 bytes for stack)
- 32 bidirectional I/O lines
- Keyboard interrupts
- 8-bit count-down timer with programmable 7-bit prescaler
- On-chip crystal oscillator, with built-in capacitor for RC option
- Second software programmable external interrupt line ($\overline{\text{IRQ2}}$)
- Direct LED drive capability on all ports
- Programmable 20KΩ pull-up resistors integrated into I/O ports

2.3 Pin Assignments

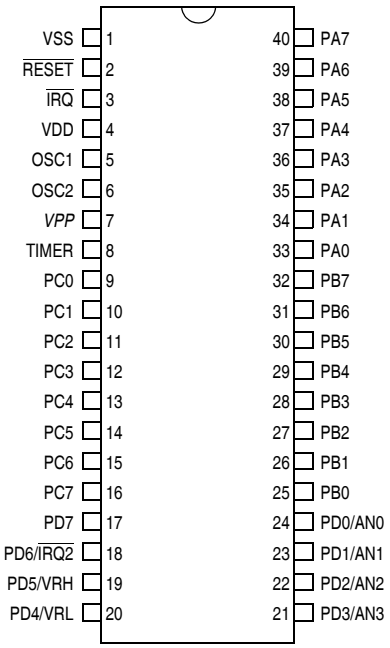

Figure 2-4 Pin Assignment for 40-pin PDIP

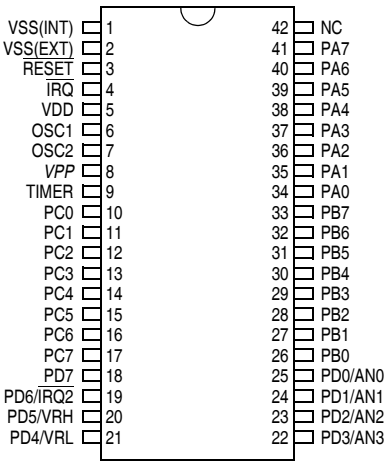

Figure 2-5 Pin Assignment for 42-pin SDIP

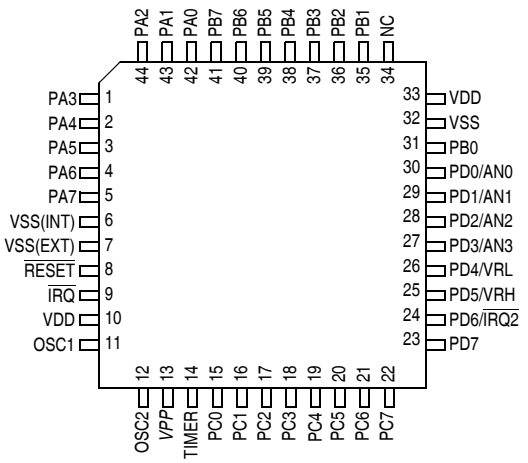

Figure 2-6 Pin Assignment for 44-pin QFP

PCP — Port C Pull-up

1 (set) – The internal 20KΩ pull-up resistors are connected to the inputs of Port C.

0 (clear) – No pull-up resistor is connected to the inputs of Port C.

PBP — PB2:PB7 Pull-up

1 (set) – The internal 20KΩ pull-up resistors are connected to the inputs of PB2-PB7.

0 (clear) – No pull-up resistor is connected to the inputs of PB2-PB7.

PB1 — PB1 pull-up

1 (set) – The internal 20KΩ pull-up resistor is connected to the input of PB1.

0 (clear) – No pull-up resistor is connected to the input of PB1.

PB0 — PB0 pull-up

1 (set) – The internal 20KΩ pull-up resistor is connected to the input of PB0.

0 (clear) – No pull-up resistor is connected to the input of PB0.

4.4 Memory Map

Figure 4-1 shows the memory map for MC68HC05SR3/*MC68HC705SR3* device.

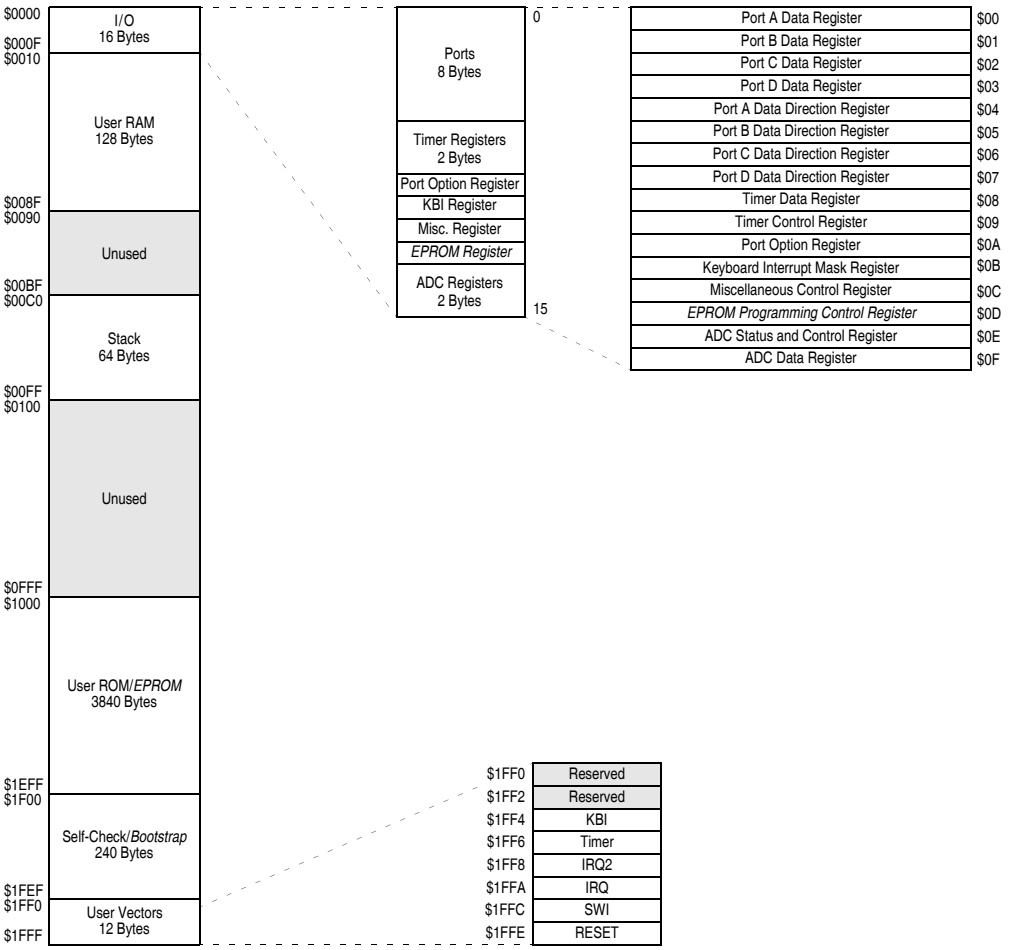

Figure 4-1 MC68HC05SR3/*MC68HC705SR3* Memory Map

7.1 ADC Operation

As shown in Figure 7-1, the ADC consists of an analog multiplexer, an 8-bit digital to analog capacitor array, a comparator and a successive approximation register (SAR).

There are eight options that can be selected by the multiplexer; the AN0 to AN3 input pins, V_{RH}, V_{RL}, $(V_{RH}+V_{RL})/4$, or $(V_{RH}+V_{RL})/2$. Selection is done via the CHx bits in the ADC Status and Control Register. AN0 to AN3 are input points for ADC conversion operations; the others are reference points which can be used for test purposes. The converter uses V_{RH} and V_{RL} as reference voltages. An input voltage equal to or greater than V_{RH} converts to $FF. An input voltage equal to or less than V_{RL}, but greater than V_{SS}, converts to $00. Maximum and minimum ratings must not be exceeded. Each analog input source should use V_{RH} as the supply voltage and should be referenced to V_{RL} for the ratiometric conversions. To maintain full accuracy of the ADC, the following should be noted:

1) V_{RH} should be equal to or less than V_{CC};
2) V_{RL} should be equal to or greater than V_{SS} but less than maximum specifications; and
3) $V_{RH}–V_{RL}$ should be equal to or greater than 4 Volts.

The ADC reference inputs (V_{RH} and V_{RL}) are applied to a precision internal digital to analog converter. Control logic drives this D/A converter and the analog output is successively compared with the selected analog input sampled at the beginning of the conversion. The conversion is monotonic with no missing codes.

The result of each successive comparison is stored in the successive approximation register (SAR) and, when the conversion is complete, the contents of the SAR are transferred to the read-only ADC Data Register ($0F), and the conversion complete flag, COCO, is set in the ADC Status and Control Register ($0E).

Warning: Any write to the ADC Status and Control Register will abort the current conversion, reset the conversion complete flag (COCO) and a new conversion starts on the selected channel.

At power-on or external reset, both the ADRC and ADON bits are cleared, thus the ADC is disabled.

Table 8-1 MUL instruction

Operation	**X:A ← X*A**			
Description	Multiplies the eight bits in the index register by the eight bits in the accumulator and places the 16-bit result in the concatenated accumulator and index register.			
Condition codes	H : Cleared I : Not affected N : Not affected Z : Not affected C : Cleared			
Source	MUL			
Form	Addressing mode	Cycles	Bytes	Opcode
	Inherent	11	1	$42

Table 8-2 Register/memory instructions

		Addressing modes																	
		Immediate			Direct			Extended			Indexed (no offset)			Indexed (8-bit offset)			Indexed (16-bit offset)		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**
Load A from memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in memory	STA				B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in memory	STX				BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add memory and carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract memory from A with borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND memory with A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR memory with A	EOR	A8	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic compare A with memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic compare X with memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit test memory with A (logical compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump unconditional	JMP				BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to subroutine	JSR				BD	2	5	CD	3	6	FD	1	5	ED	2	6	DD	3	7

8.3.4 Extended

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode byte. Instructions with extended addressing mode are capable of referencing arguments anywhere in memory with a single three-byte instruction. When using the Freescale assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the short form of the instruction.

EA = (PC+1):(PC+2); PC ← PC+3
Address bus high ← (PC+1); Address bus low ← (PC+2)

8.3.5 Indexed, no offset

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. This addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

EA = X; PC ← PC+1
Address bus high ← 0; Address bus low ← X

8.3.6 Indexed, 8-bit offset

In the indexed, 8-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode. Therefore the operand can be located anywhere within the lowest 511 memory locations. This addressing mode is useful for selecting the mth element in an n element table.

EA = X+(PC+1); PC ← PC+2
Address bus high ← K; Address bus low ← X+(PC+1)
where K = the carry from the addition of X and (PC+1)

8.3.7 Indexed, 16-bit offset

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This address mode can be used in a manner similar to indexed, 8-bit offset except that this three-byte instruction allows tables to be anywhere in memory. As with direct and extended addressing, the Freescale assembler determines the shortest form of indexed addressing.

EA = X+[(PC+1):(PC+2)]; PC ← PC+3
Address bus high ← (PC+1)+K; Address bus low ← X+(PC+2)
where K = the carry from the addition of X and (PC+2)

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9.3 SLOW Mode

The SLOW mode function is controlled by the SM bit in the Miscellaneous Control Register. When the SM bit is set, the internal bus clock is divided by 16, resulting to a frequency equal to the oscillator frequency divide by 32. This feature permits a slow down of all the internal operations and thus reduces power consumption — particularly useful while in WAIT mode. The SM bit is automatically cleared while going to STOP mode.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous Control Register	$0C	KBIE	KBIC	INTO	INTE	LVRE	SM	IRQ2F	IRQ2E	0001 0000

SM — Slow Mode

1 (set) – Slow mode enabled. Internal bus frequency $f_{OP}=f_{OSC} \div 32$.

0 (clear) – Slow mode disabled. Internal bus frequency $f_{OP}=f_{OSC} \div 2$.

9.4 Data-Retention Mode

If the Low Voltage Reset function is not enabled, the contents of RAM and CPU registers are retained at supply voltages as low as 2Vdc. This is called the data-retention mode where the data is held, but the device is not guaranteed to operate. The $\overline{\text{RESET}}$ pin must be held low during data-retention mode.

The Low Voltage Reset Function is enabled/disabled by the LVRE bit in the Miscellaneous Control Register ($0C).

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous Control Register	$0C	KBIE	KBIC	INTO	INTE	LVRE	SM	IRQ2F	IRQ2E	0001 0000

LVRE — Low Voltage Reset Enable

1 (set) – Low Voltage Reset function enabled.

0 (clear) – Low Voltage Reset function disabled.

Table 10-2 Self-Check Report

D4	D3	D2	D1	REMARKS
Flashing				O.K. (self-check is on-going)
1	1	1	1	Bad port A
1	1	1	0	Bad port B
1	1	0	1	Bad port C
1	1	0	0	Bad port D
1	0	1	1	Bad RAM
1	0	1	0	Bad ROM
1	0	0	0	Bad SWI
0	1	1	1	Bad $\overline{IRQ}$

1=LED on, 0=LED off

10.3 Bootstrap Mode

The Bootstrap mode is provided in the EPROM part (MC68HC705SR3) as a mean of self-programming its EPROM with minimal circuitry. Bootstrap mode will be entered on the rising edge of $\overline{RESET}$ when the V_{PP} pin is at V_{TST} ($2 \times V_{DD}$) and PB1 pin is at V_{DD}. Once in the bootstrap mode, PB1 can then be used for other purposes. After entering the bootstrap mode, CPU branches to the bootstrap program and carries out the EPROM programming routine. The user EPROM consists of 3840 bytes, from location $1000 to $1EFF.

Refer to Appendix A for further details on MC68HC705SR3.

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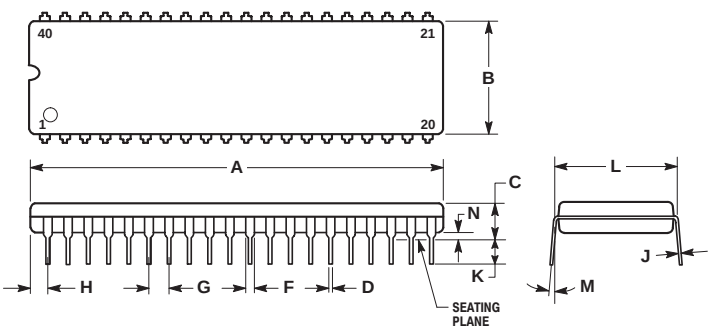
12.1 40-Pin DIP Package (Case 711-03)

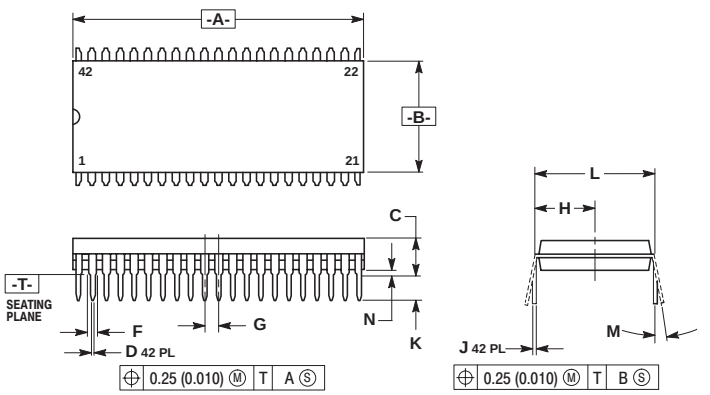


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

Figure 12-1 40-pin DIP Package

12.2 42-Pin SDIP Package (Case 858-01)

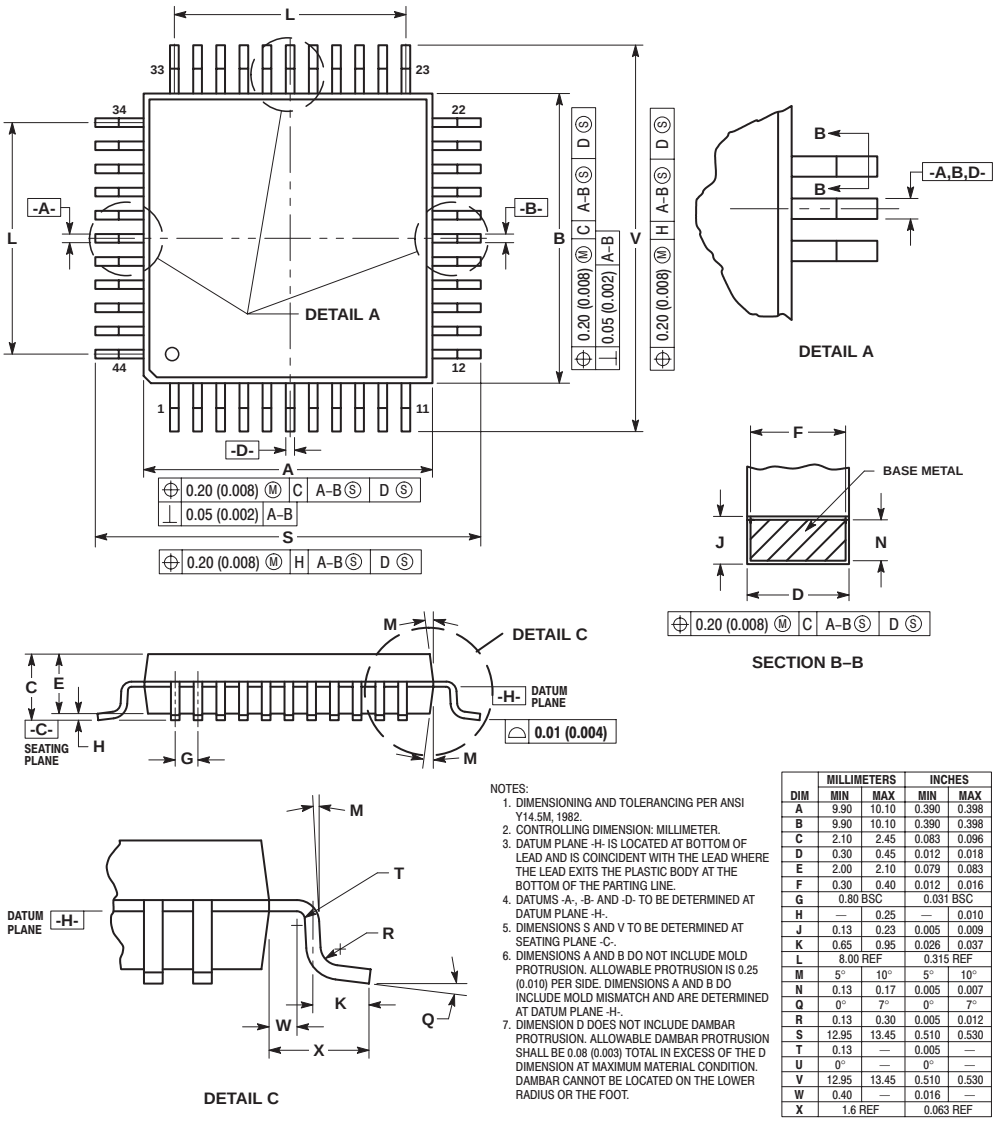


NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

Figure 12-2 42-pin SDIP Package

12.3 44-pin QFP Package (Case 824A-01)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.30	0.45	0.012	0.018
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	8.00 REF		0.315 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	—	0.005	—
U	0°	—	0°	—
V	12.95	13.45	0.510	0.530
W	0.40	—	0.016	—
X	1.6 REF		0.063 REF	

Figure 12-3 44-pin QFP Package

```
CLR    PCR          ;reset PCR
LDX    #$00         ;load index register with 00
BSET   1,PCR        ;set ELAT bit
LDA    #$00         ;load data=00 in to A
STA    $1900,X      ;latch data and address
BSET   0,PCR        ;program
JSR    DELAY        ;call delay subroutine for 1ms
CLR    PCR          ;reset PCR
```

A.5 Mask Option Register (MOR)

The Mask Option Register (MOR) contains programmable EPROM bits to control mask options, and cannot be changed in User mode. The erased state are zeros. This register is latched upon reset going away.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Mask Option Register (MOR)	$0FFF			SMD	SEC	TMR2	TMR1	TMR0	RC	unaffected

SMD — SLOW Mode at Power-on

When programmed to “1”, this bit enables SLOW mode at power-up. Operating frequency, $f_{OP}=f_{OSC}\div2\div16=f_{OSC}\div32$.

SEC — EPROM Security

When programmed to “1”, this bit disables some functions of the Bootstrap mode, preventing external reading of EPROM content.

TMR2:TMR0 — Power-on Reset Delay

The amount Power-On Reset delay is set by programming these three bits. The delay is selected as follows:

TMR2	TMR1	TMR0	Delay (Instruction Cycles)
0	0	0	256
0	0	1	512
0	1	0	1024
0	1	1	2048
1	0	0	4096
1	0	1	8192
1	1	0	16384
1	1	1	32768

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