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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SIO, SPI, UART/USART
Peripherals	DMA, LVD, WDT
Number of I/O	73
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	109-TFBGA
Supplier Device Package	109-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/toshiba-semiconductor-and-storage/tmpm366fyxbg

Table 1-2 Pin Names and Functions Sorted by Port (3/7)

PORT	Type	Pin No.	Pin Name	Input/ Out-put	Function
PORT E	Function	D11	PE0 TXD0 A20	I/O O O	I/O port Serial channel sending serial data Address bus
PORT E	Function	D12	PE1 RXD0 A21	I/O I O	GND pin Serial channel receiving serial data Address bus
PORT E	Function	C11	PE2 SCLK0 TB2OUT $\overline{CTS0}$ A22	I/O I/O O I O	I/O port Serial channel clock pin 16-bit timer / event counter output Serial channel handshake input pin Address bus
PORT E	Function	C12	PE3 INT5 A15 TB3OUT A23	I/O I O O O	I/O port External interrupt pin Address bus 16-bit timer / event counter output Address bus
PORT E	Function	C7	PE4 SDA1/SO1 A14	I/O I/O O	I/O port Data in I2C mode/Data in SIO mode Address bus
PORT E	Function	B7	PE5 SCL1/SI1 A13	I/O I/O O	I/O port Clock in I2C mode/Data in SIO mode Address bus
PORT E	Function	C6	PE6 SCK1 A12	I/O I/O O	I/O port Clock in SIO mode Address bus
PORT E	Function	B6	PE7 INT4 A11	I/O I O	I/O port External interrupt pin Address bus
PORT F	Function/ Control	M5	PF0 TB6OUT $\overline{BOOT}$	I/O O I	I/O port 16-bit timer / event counter output Setting a boot mode TMPM366FDXBG/FYXBG/FWXBG goes into single boot mode by sampling "Low" at the rising edge of a $\overline{RESET}$ pin.
PORT F	Function	L5	PF1 $\overline{RD}$	I/O O	I/O port Read strobe signal
PORT F	Function	K6	PF2 $\overline{WR}$	I/O O	I/O port Write strobe signal
PORT F	Function	L6	PF3 $\overline{BELL}$	I/O O	I/O port Byte enable signal as an external 8-bit memory access
PORT F	Function	M6	PF4 $\overline{BELH}$ INT6 TB5IN0	I/O O I I	I/O port Byte enable signal as an external 8-bit memory access External interrupt pin Inputting 16-bit timer / event counter capture trigger

2.3 Exceptions/ Interruptions

Exceptions and interruptions are described in the following section.

2.3.1 Number of Interrupt Inputs

The number of interrupt inputs can optionally be defined from 1 to 240 in the Cortex-M3 core.

TMPM366FDXBG/FYXBG/FWXBG has 60 interrupt inputs. The number of interrupt inputs is reflected in <INTLINESNUM[4:0]> bit of NVIC register. In this product, if read <INTLINESNUM[4:0]> bit, 0x00 is read out.

2.3.2 Number of Priority Level Interrupt Bits

The Cortex-M3 core can optionally configure the number of priority level interrupt bits from 3 bits to 8 bits.

TMPM366FDXBG/FYXBG/FWXBG has 3 priority level interrupt bits. The number of priority level interrupt bits is used for assigning a priority level in the interrupt priority registers and system handler priority registers.

2.3.3 SysTick

The Cortex-M3 core has a SysTick timer which can generate SysTick exception.

For the detail of SysTick exception, refer to the section of "SysTick" in the exception and the register of SysTick in the NVIC register.

2.3.4 SYSRESETREQ

The Cortex-M3 core outputs SYSRESETREQ signal when <SYSRESETREQ> bit of Application Interrupt and Reset Control Register are set.

TMPM366FDXBG/FYXBG/FWXBG provides the same operation when SYSRESETREQ signal are output.

2.3.5 LOCKUP

When irreparable exception generates, the Cortex-M3 core outputs LOCKUP signal to show a serious error included in software.

TMPM366FDXBG/FYXBG/FWXBG does not use this signal. To return from LOCKUP status, it is necessary to use non-maskable interruput (NMI) or reset.

2.3.6 Auxiliary Fault Status register

The Cortex-M3 core provides auxiliary fault status registers to supply additional system fault information to software.

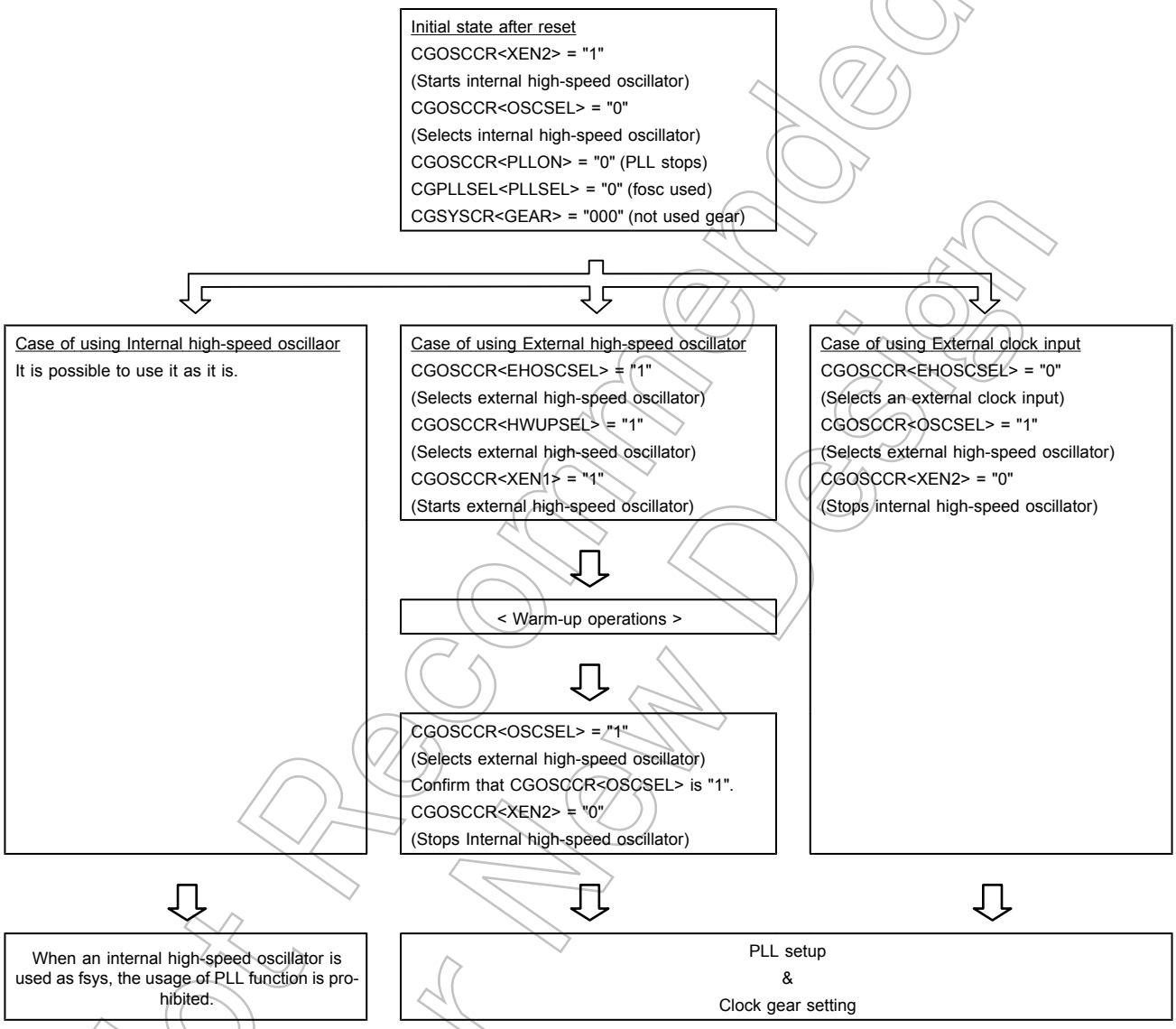
However, TMPM366FDXBG/FYXBG/FWXBG is not defined this function. If auxiliary fault status register is read, always "0x0000_0000" is read out.

8.3.6.1 System Clock setting

The system clock can be selected by CGOSCCR. After the clock is selected, the PLL setting is done if necessary with CGPLLSEL and CGOSCCR. And, the clock gear is set with CGSYSCR.

The clock setup sequence is shown as follow.

Clock setup sequence



9. Exceptions

This chapter describes features, types and handling of exceptions.

Exceptions have close relation to the CPU core. Refer to "Cortex-M3 Technical Reference Manual" if needed.

9.1 Overview

An exception causes the CPU to stop the currently executing process and handle another process.

There are two types of exceptions: those that are generated when some error condition occurs or when an instruction to generate an exception is executed; and those that are generated by hardware, such as an interrupt request signal from an external pin or peripheral function.

All exceptions are handled by the Nested Vectored Interrupt Controller (NVIC) in the CPU according to the respective priority levels. When an exception occurs, the CPU stores the current state to the stack and branches to the corresponding interrupt service routine (ISR). Upon completion of the ISR, the information stored to the stack is automatically restored.

9.1.1 Exception Types

The following types of exceptions exist in the Cortex-M3.

For detailed descriptions on each exception, refer to "Cortex-M3 Technical Reference Manual".

- Reset
- Non-Maskable Interrupt (NMI)
- Hard Fault
- Memory Management
- Bus Fault
- Usage Fault
- SVCall (Supervisor Call)
- Debug Monitor
- PendSV
- SysTick
- External Interrupt

10.2.6 Port F (PF0 to PF7)

The port F is a general-purpose, 1-bit output port and 7-bit input/output port. For this port, inputs and outputs can be specified in units of bits. Besides the general-purpose port function, the port F performs the functions of the external bus interface, the external interrupt input, 16-bit timer / event counter and the mode setting function ($\overline{\text{BOOT}}$).

Reset initializes from bit7 to bit1 of the port F as general-purpose ports with input, output and pull-up disabled. Reset initializes bit0 of PF as output port with output disabled and pull-up enabled.

The port F has three types of function register. If you use the port F as a general-purpose port, set "0" to the corresponding bit of the three registers. If you use the port F as other than a general-purpose port, set "1" to the corresponding bit of the function register. Do not set "1" to the some function registers at the same time.

While $\overline{\text{RESET}}$ pin is "Low", input and pull-up of PF0 ($\overline{\text{BOOT}}$) are enabled. At the rising edge of $\overline{\text{RESET}}$ pin, if PF0 ($\overline{\text{BOOT}}$) is "High", TMPM366FDXBG/FYXBG/FWXBG enters the single chip mode and boots from the on chip Flash ROM. If PF0 ($\overline{\text{BOOT}}$) is "Low", TMPM366FDXBG/FYXBG/FWXBG enters the single boot mode and boots from the on chip BOOTROM. For details of the single boot mode, refer to "Flash memory operation".

Note: In modes other than STOP mode, interrupt input is enabled regardless of the PxFR register setting if input is enabled in PxIE. Make sure to disable unused interrupts when programming the device.

10.2.6.1 Port F Register

Base Address = 0x400C_0500

Register name		Address (Base+)
Port F data register	PFDATA	0x0000
Port F output control register	PFCR	0x0004
Port F function register 1	PFFR1	0x0008
Port F function register 2	PFFR2	0x000C
Port F function register 3	PFFR3	0x0010
Reserved	-	0x0014
Reserved	-	0x0018
Reserved	-	0x001C
Reserved	-	0x0020
Reserved	-	0x0024
Port F open drain control register	PFOD	0x0028
Port F pull-up control register	PFPUP	0x002C
Reserved	-	0x0030
Reserved	-	0x0034
Port F input control register	PFIE	0x0038

Note: Access to the "reserved" areas is prohibited.

10.2.6.7 PFOD (Port F open drain control register)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	PF7OD	PF6OD	PF5OD	PF4OD	PF3OD	PF2OD	PF1OD	PF0OD
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-8	−	R	Read as "0".
7-0	PF7OD-PF0OD	R/W	0: Push-pull output 1: Open-drain output

10.2.6.8 PFPUP (Port F pull-up control register)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	PF7UP	PF6UP	PF5UP	PF4UP	PF3UP	PF2UP	PF1UP	PF0UP
After reset	0	0	0	0	0	0	0	1

Bit	Bit Symbol	Type	Function
31-8	−	R	Read as "0".
7-0	PF7UP-PF1UP	R/W	Pull-up 0: Disable 1: Enable

10.2.10.5 PJFR3 (Port J function register 3)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	PJ7F3	PJ6F3	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-8	−	R	Read as "0".
7	PJ7F3	R/W	0: PORT 1: TB0IN1
6	PJ6F3	R/W	0: PORT 1: TB0IN0
5-0	-	R	Read as "0".

Table 13-3 Prescaler Output Clock Resolutions(fc = 48MHz)

Select peripheral clock CGSYSCR <FPSEL>	Clock gear value CGSYSCR <GEAR[2:0]>	Select prescaler clock CGSYSCR <PRCK[2:0]>	Prescaler output clock function			
			φT32	φT64	φT128	φT256
1 (fc)	000 (fc)	000 (fperiph/1)	fc/2^6 (1.33 μs)	fc/2^7 (2.67 μs)	fc/2^8 (5.33 μs)	fc/2^9 (10.67 μs)
		001 (fperiph/2)	fc/2^7 (2.67 μs)	fc/2^8 (5.33 μs)	fc/2^9 (10.67 μs)	fc/2^{10} (21.33 μs)
		010 (fperiph/4)	fc/2^8 (5.33 μs)	fc/2^9 (10.67 μs)	fc/2^{10} (21.33 μs)	fc/2^{11} (42.67 μs)
		011 (fperiph/8)	fc/2^9 (10.67 μs)	fc/2^{10} (21.33 μs)	fc/2^{11} (42.67 μs)	fc/2^{12} (85.33 μs)
		100 (fperiph/16)	fc/2^{10} (21.33 μs)	fc/2^{11} (42.67 μs)	fc/2^{12} (85.33 μs)	fc/2^{13} (170.67 μs)
		101 (fperiph/32)	fc/2^{11} (42.67 μs)	fc/2^{12} (85.33 μs)	fc/2^{13} (170.67 μs)	fc/2^{14} (341.33 μs)
	100 (fc/2)	000 (fperiph/1)	fc/2^6 (1.33 μs)	fc/2^7 (2.67 μs)	fc/2^8 (5.33 μs)	fc/2^9 (10.67 μs)
		001 (fperiph/2)	fc/2^7 (2.67 μs)	fc/2^8 (5.33 μs)	fc/2^9 (10.67 μs)	fc/2^{10} (21.33 μs)
		010 (fperiph/4)	fc/2^8 (5.33 μs)	fc/2^9 (10.67 μs)	fc/2^{10} (21.33 μs)	fc/2^{11} (42.67 μs)
		011 (fperiph/8)	fc/2^9 (10.67 μs)	fc/2^{10} (21.33 μs)	fc/2^{11} (42.67 μs)	fc/2^{12} (85.33 μs)
		100 (fperiph/16)	fc/2^{10} (21.33 μs)	fc/2^{11} (42.67 μs)	fc/2^{12} (85.33 μs)	fc/2^{13} (170.67 μs)
		101 (fperiph/32)	fc/2^{11} (42.67 μs)	fc/2^{12} (85.33 μs)	fc/2^{13} (170.67 μs)	fc/2^{14} (341.33 μs)
	101 (fc/4)	000 (fperiph/1)	fc/2^6 (1.33 μs)	fc/2^7 (2.67 μs)	fc/2^8 (5.33 μs)	fc/2^9 (10.67 μs)
		001 (fperiph/2)	fc/2^7 (2.67 μs)	fc/2^8 (5.33 μs)	fc/2^9 (10.67 μs)	fc/2^{10} (21.33 μs)
		010 (fperiph/4)	fc/2^8 (5.33 μs)	fc/2^9 (10.67 μs)	fc/2^{10} (21.33 μs)	fc/2^{11} (42.67 μs)
		011 (fperiph/8)	fc/2^9 (10.67 μs)	fc/2^{10} (21.33 μs)	fc/2^{11} (42.67 μs)	fc/2^{12} (85.33 μs)
		100 (fperiph/16)	fc/2^{10} (21.33 μs)	fc/2^{11} (42.67 μs)	fc/2^{12} (85.33 μs)	fc/2^{13} (170.67 μs)
		101 (fperiph/32)	fc/2^{11} (42.67 μs)	fc/2^{12} (85.33 μs)	fc/2^{13} (170.67 μs)	fc/2^{14} (341.33 μs)
	110 (fc/8)	000 (fperiph/1)	fc/2^6 (1.33 μs)	fc/2^7 (2.67 μs)	fc/2^8 (5.33 μs)	fc/2^9 (10.67 μs)
		001 (fperiph/2)	fc/2^7 (2.67 μs)	fc/2^8 (5.33 μs)	fc/2^9 (10.67 μs)	fc/2^{10} (21.33 μs)
		010 (fperiph/4)	fc/2^8 (5.33 μs)	fc/2^9 (10.67 μs)	fc/2^{10} (21.33 μs)	fc/2^{11} (42.67 μs)
		011 (fperiph/8)	fc/2^9 (10.67 μs)	fc/2^{10} (21.33 μs)	fc/2^{11} (42.67 μs)	fc/2^{12} (85.33 μs)
		100 (fperiph/16)	fc/2^{10} (21.33 μs)	fc/2^{11} (42.67 μs)	fc/2^{12} (85.33 μs)	fc/2^{13} (170.67 μs)
		101 (fperiph/32)	fc/2^{11} (42.67 μs)	fc/2^{12} (85.33 μs)	fc/2^{13} (170.67 μs)	fc/2^{14} (341.33 μs)
	111 (fc/16)	000 (fperiph/1)	fc/2^6 (1.33 μs)	fc/2^7 (2.67 μs)	fc/2^8 (5.33 μs)	fc/2^9 (10.67 μs)
		001 (fperiph/2)	fc/2^7 (2.67 μs)	fc/2^8 (5.33 μs)	fc/2^9 (10.67 μs)	fc/2^{10} (21.33 μs)
		010 (fperiph/4)	fc/2^8 (5.33 μs)	fc/2^9 (10.67 μs)	fc/2^{10} (21.33 μs)	fc/2^{11} (42.67 μs)
		011 (fperiph/8)	fc/2^9 (10.67 μs)	fc/2^{10} (21.33 μs)	fc/2^{11} (42.67 μs)	fc/2^{12} (85.33 μs)
		100 (fperiph/16)	fc/2^{10} (21.33 μs)	fc/2^{11} (42.67 μs)	fc/2^{12} (85.33 μs)	fc/2^{13} (170.67 μs)
		101 (fperiph/32)	fc/2^{11} (42.67 μs)	fc/2^{12} (85.33 μs)	fc/2^{13} (170.67 μs)	fc/2^{14} (341.33 μs)

Note 1: The prescaler output clock φTn must be selected so that φTn < fsys is satisfied (so that φTn is slower than fsys).
Note 2: Do not change the clock gear while the timer is operating.
Note 3: "−" denotes a setting prohibited.

14.4.2.7 UDFS2WVL(wValue register)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	value							
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	value							
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-16	−	R	Read as undefined.
15-8	value[15:8]	R	Indicates the data of the fourth byte received with the Setup-Token (wValue (High) field).
7-0	value[7:0]	R	Indicates the data of the third byte received with the Setup-Token (wValue (Low) field).

14.5.3 Operation Sequence

The operation sequence of UDC2AB is as follows:

1. Hardware reset
2. Set the interrupt signal

   Configure the INTUSB interrupt, the INTUSBWKUP interrupt and the USBPON interrupt.
3. VBUS detection (connect) and reset

   Refer to "14.5.5.2 Sequence of USB Bus Power (VBUS) Connection/Disconnection" and "14.5.1 Reset" for details.
4. USB enumeration response

   Refer to "14.6 USB Device Response" for details.
5. Master Read / Master Write transfer
   a. Master Read transfer

      Make a Master Read transfer corresponding to the receiving request from the USB host. Refer to "14.5.4.1 Master Read transfer" for details.
   b. Master Write transfer

      Make a Master Write transfer corresponding to the sending request from the USB host. Refer to "14.5.4.2 Master Write transfer" for details.
6. VBUS detection (disconnect)

   The USB bus power supply may be disconnected at any time.

   Refer to "14.5.5.2 Sequence of USB Bus Power (VBUS) Connection/Disconnection" for details.

4. When "Set_configuration" and "Set_interface" requests are received

   By setting 100 to the UDFS2ADR<configured> <addressed> <default> after receiving the "Set_configuration" and "Set_interface" requests, UDC2 will be in the "Configured" status.

   In the "Configured" status, you can make transfers to the EP to which status settings have been made.

   In order to make the EP "Ready," the following settings should be made:

   - Set the maximum packet size to UDFS2EPxMSZ
   - Set the transfer mode to UDFS2EPxSTS
   - Issue the EP_Reset command to UDFS2CMD

   EPs will be available for transmitting and receiving data after these settings have been made.

   Figure 14-21 shows the "Device State Diagram".

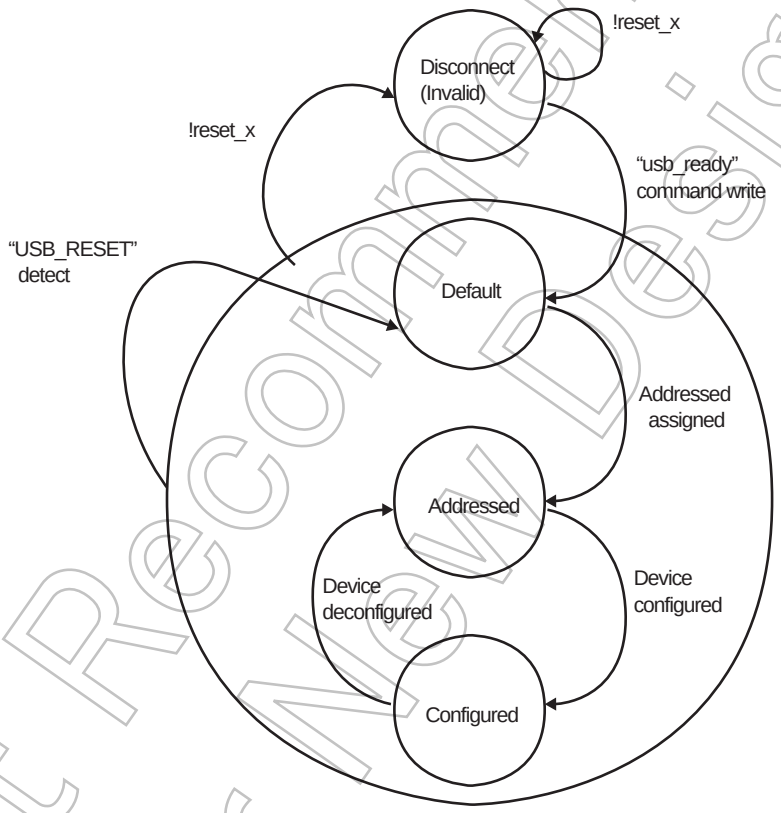


Figure 14-21 Device state diagram

16. Asynchronous Serial Channel (UART)

16.1 Overview

This device has the Asynchronous serial channel (UART) with Modem control.

Their features are given in the following.

- Transmit FIFO

  8-bit width/ 32 location deep.
- Receive FIFO

  12-bit width/ 32 location deep.
- Transmit /Receive data format
  - DATA bits: 5,6,7,8 bits can be selected.
  - PARITY : use / no use
  - STOP bit : 1bit / 2 bits
- FIFO ON/OFF
  - ON (FIFO mode)/
  - OFF (characters mode)
- Interrupt
  - Combined interrupt factors are output to interrupt controller.
  - The permission of each interrupt factor is programmable.
- Baud rate generator

  Generates a common transmit and receive internal clock form UART internal reference clock input.

  Supports baud rates of up to 2.95Mbps at fsys = 48MHz.
- DMA
- IrDA 1.0 Function
  - Max data rate : 115.2 kbps (half-duplex).
  - support low power mode
- Control pins

  TXD (IROUT)

  RXD (IRIN)

  $\overline{\text{CTS}}$

  RIN

  $\overline{\text{RTS}}$

  DCD

  DSR

  DTR
- Hardware flow control

  RTS support

  CTS support

16.3.3 UARTRSR (Receive status Register)

UARTRSR and UARTECR are mapped to same address.

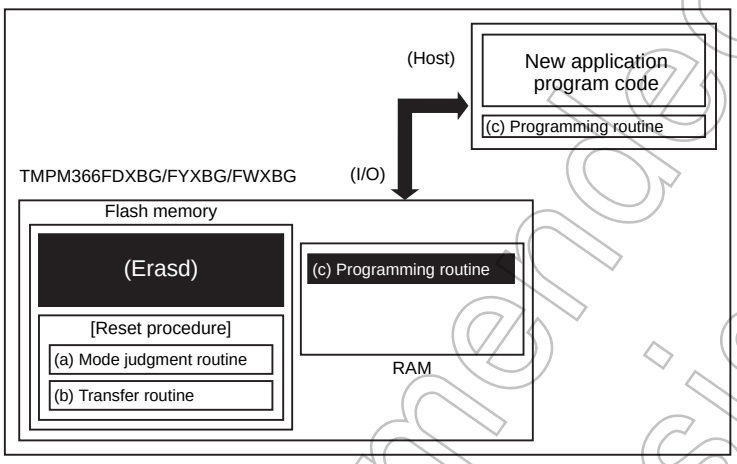
These functions differ in read and write operations.

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	-	-	-	-	OE	BE	PE	FE
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-4	−	R	Read as 0.
3	OE	R	Overrun error This bit is set to 1 if data is received and the FIFO is already full. This bit is cleared 0 by writing a data to UARTECR. When FIFO is already full, the received data is not stored in the FIFO. Therefore the contents of FIFO are valid and only the contents of shift register is over written. In this case, CPU must be read out a data from FIFO to make empty FIFO.
2	BE	R	Break error This bit is set to 1 if a break condition was detected, indicating that the receive data input (defined as start, data bit, data parity, and stop bits) was held Low for longer than a full-word transmission time. This bit is cleared 0 by writing a data to UARTECR. In FIFO mode, this error is occurred by the highest character in FIFO. Break is occurred only when one zero character is loaded in FIFO. The next character is enabled when received data makes 1 (marking state) and the next effective start bit is received.
1	PE	R	Parity error When this bit is set to 1, it indicates that the parity of the received data does not match the parity defined by bits 2 and 7 of the UARTxLCR_H register. This bit is cleared 0 by writing a data to UARTECR. In FIFO mode, this error is occurred by the highest character in FIFO.
0	FE	R	Framing error When this bit is set to 1, it indicates that the received data did not have a valid stop bit (a valid stop bit is 1). This bit is cleared 0 by writing a data to UARTECR. In FIFO mode, this error is occurred by the highest character in FIFO.

(4) Step-4

Jump program execution to the flash programming routine in the on-chip RAM to erase a flash block containing the old application program code.



(5) Step-5

Continue executing the flash programming routine to download new program code from the host controller and program it into the erased flash block. When the programming is completed, the writing or erase protection of that flash block in the user program area must be set.

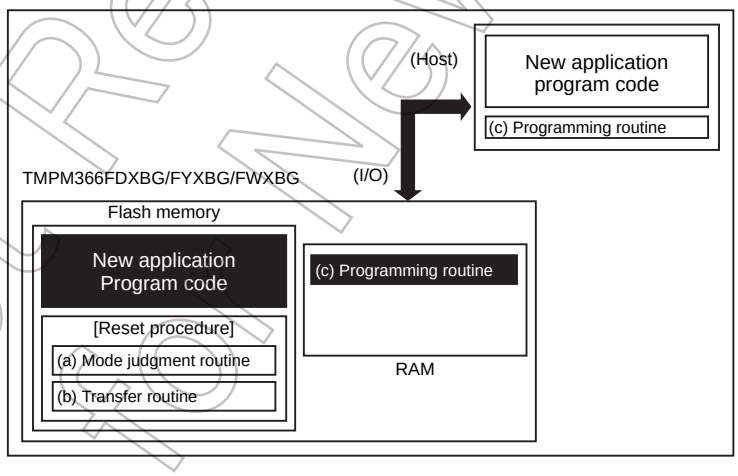


Table 20-3 Required Pin Connections

Pins		Interface		
		UART	I/O Interface Mode	USB
Mode-setting pin	MODE	Connect with Pull-down resistance		
	FTEST3	fixed to open		
	PE3	×	×	o (="L":Internal clock ,="H":External Clock)
	PE5	o (="L" input)	o (="L" input)	o (="H" input)
	PG5	×	×	o (for Vbus detection)
	$\overline{\text{BOOT}}$ (PF0)	o	o	o
	X1	-	-	o(12/16/48MHz)
Reset pin	$\overline{\text{RESET}}$	o	o	o
Communication pins	TXD0 (PE0)	o	o	×
	RXD0 (PE1)	o	o	×
	SCLK0 (PE2)	×	o (Input mode)	×
	PE4	×	o (Output mode)	o (Output mode)
	D+	×	×	o
	D-	×	×	o

o : used ×: unused

fifth bus write cycle, data is command written to the same page area. Even if it is desired to write the page only partially, it is required to perform the automatic page programming for the entire page. In this case, the address input for the fourth bus write cycle shall be set to the top address of the page. Be sure to perform command write operation with the input data set to "1" for the data cells not to be set to "0." For example, if the top address of a page is not to be written, set the input data of the fourth bus write cycle to 0xFFFFFFFF to command write the data.

Once the third bus cycle is executed, the automatic page programming is in operation. This condition can be checked by monitoring FCFLCS<RDY/BSY>. Any new command sequence is not accepted while it is in automatic page programming mode. If it is desired to stop operation, use the hardware reset function. Be careful in doing so because data cannot be written normally if the operation is interrupted. When a single page has been command written normally terminating the automatic page writing process, FCFLCS<RDY/BSY> is set to "1" and it returns to the read mode.

When multiple pages are to be written, it is necessary to execute the page programming command for each page because the number of pages to be written by a single execution of the automatic page program command is limited to only one page. It is not allowed for automatic page programming to process input data across pages.

Data cannot be written to a protected block. When automatic programming is finished, it automatically returns to the read mode. This condition can be checked by monitoring FCFLCS<RDY/BSY> . If automatic programming has failed, the flash memory is locked in the mode and will not return to the read mode. For returning to the read mode, it is necessary to execute hardware reset to reset the flash memory or the device. In this case, while writing to the address has failed, it is recommended not to use the device or not to use the block that includes the failed address.

Note: **Software reset becomes ineffective in bus write cycles on and after the fourth bus write cycle of the automatic page programming command.**

(2) Automatic chip erase

The automatic chip erase operation starts when the sixth bus write cycle of the command cycle is completed.

This condition can be checked by monitoring FCFLCS<RDY/BSY> . While no automatic verify operation is performed internally to the device, be sure to read the data to confirm that data has been correctly erased. Any new command sequence is not accepted while it is in an automatic chip erase operation. If it is desired to stop operation, use the hardware reset function. If the operation is forced to stop, it is necessary to perform the automatic chip erase operation again because the data erasing operation has not been normally terminated.

Also, any protected blocks cannot be erased. If all the blocks are protected, the automatic chip erase operation will not be performed and it returns to the read mode after completing the sixth bus read cycle of the command sequence. When an automatic chip erase operation is normally terminated, it automatically returns to the read mode. If an automatic chip erase operation has failed, the flash memory is locked in the mode and will not return to the read mode.

For returning to the read mode, it is necessary to execute hardware reset to reset the device. In this case, the failed block cannot be detected. It is recommended not to use the device anymore or to identify the failed block by using the block erase function for not to use the identified block anymore.

Table 20-25 Protection Bit Erase Address Table

Block	Protection bit	The seventh bus write cycle address [18:17]	
		Address[18]	Address[17]
Block0 to 3	<BLPRO[0:3]>	0	0
Block4 to 5	<BLPRO[4:5]>	0	1

Note: **The protection bit erase command cannot erase by individual block.**

20.3.1.8 Flowchart

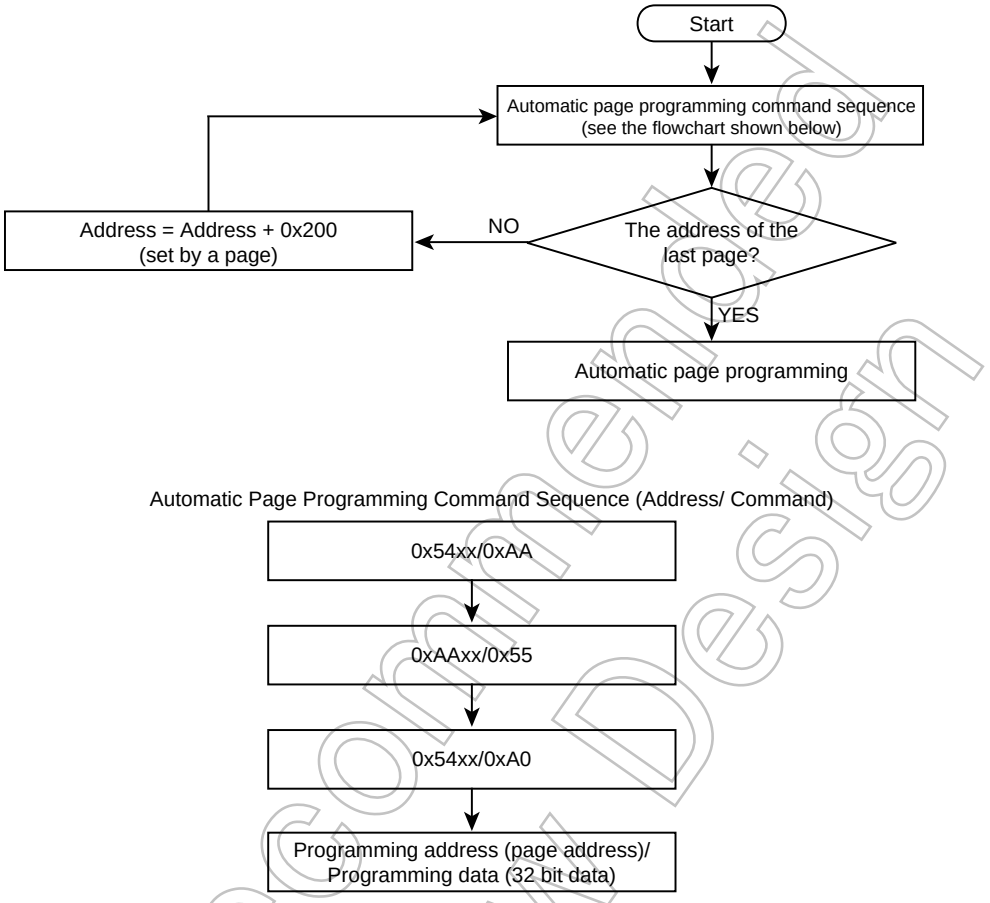
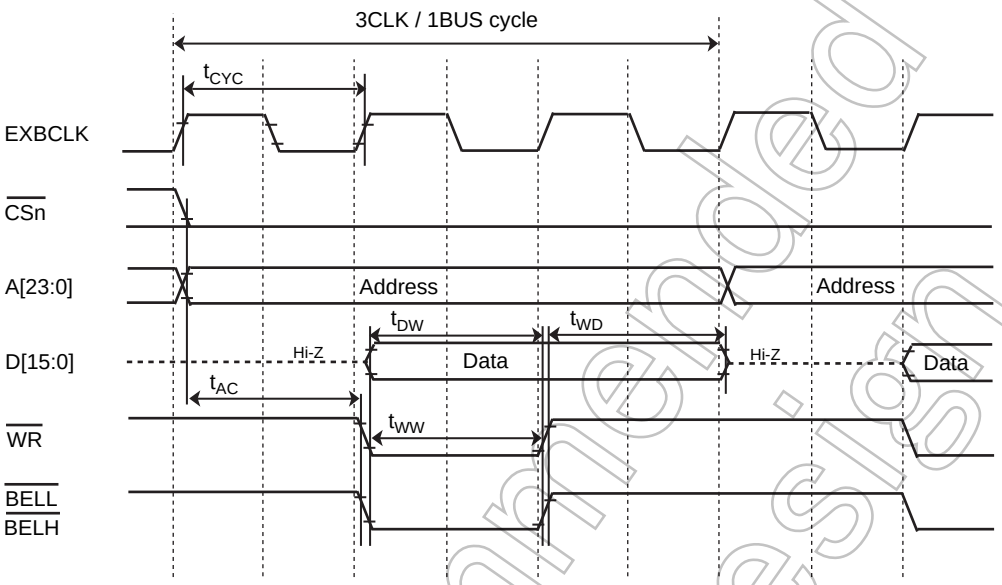


Figure 20-10 Automatic Programming

Note: Command sequence is executed by 0x54xx or 0x55xx.

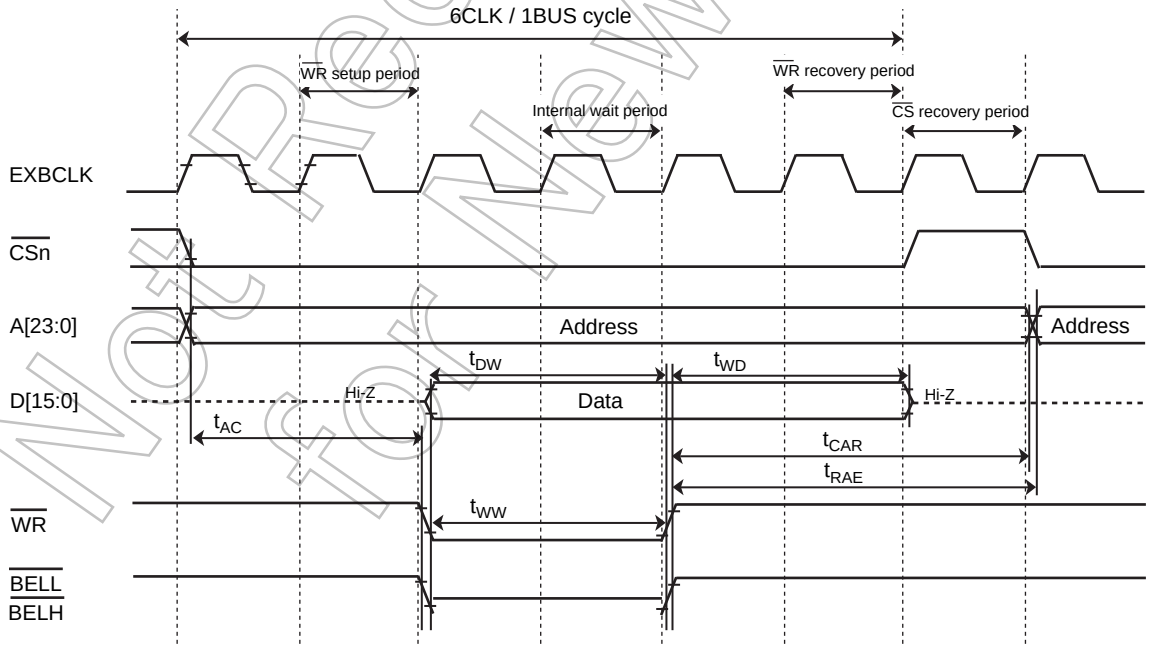
(3) Write cycle timing (minimum bus cycle)

(Neither Cycle expander, WR setup, Internal wait, CS recovery nor WR recovery function are used.)



(4) Write cycle timing (1 bus cycle per 6 clock)

(WR setup, Internal wait, CS recovery and WR recovery function are set to 1 cycle though Cycle expander function is not used.)



23.8 Handling Precaution

23.8.1 Power-on sequence

The power-on sequence must include the time for the internal regulator, internal flash memory and internal oscillator to be stable and the reset. In the TX03, the internal circuit automatically insert the time for the internal regulator which requires the time at least 1 ms and after this, internal reset operation requires 4096 cycles on internal oscillation, therefore, A little bit of time differences occur until CPU start operate. And there are multiple independent Power supply, however please operate the power-on procedure simultaneously.

The time required to achieve stable oscillation varies with system. At cold reset, the external reset pin must be kept "Low" for a duration of time sufficiently long enough for the internal regulator and oscillator to be stable.

Figure 23-2 shows the power-on sequence.

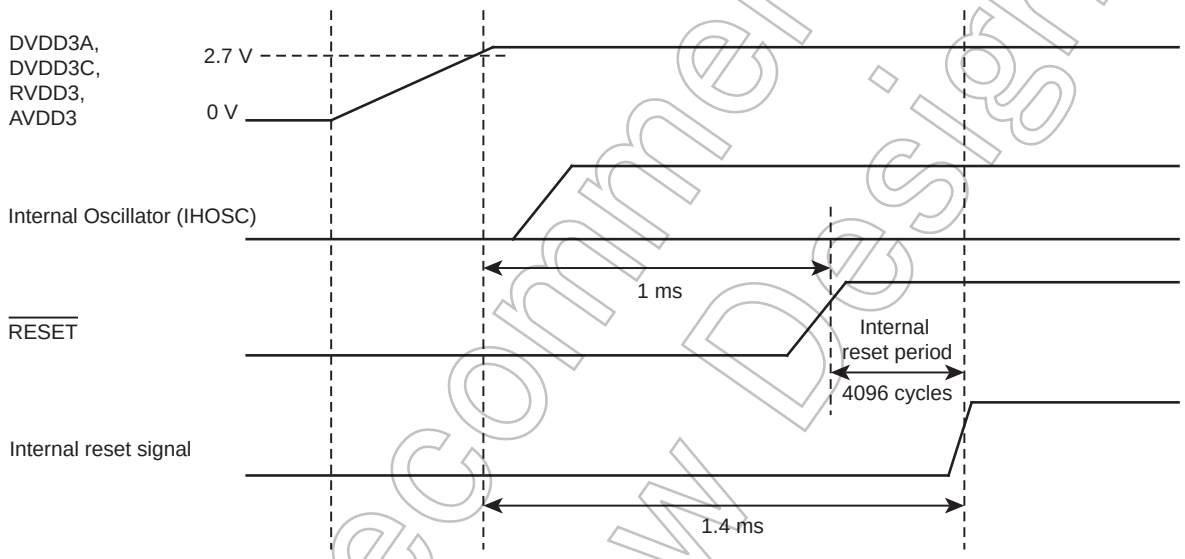


Figure 23-2 Power-on sequence