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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 6x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	25-UFBGA, WLCSP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1101lvukz

- UART with fractional baud rate generation and internal FIFO.
- One SPI controller with SSP features and with FIFO and multi-protocol capabilities.
- I^2C-bus interface supporting full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.

- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 2.5 % accuracy for T_{amb} = -20 °C to +85 °C and to 5 % accuracy for T_{amb} = -40 °C to -20 °C. The IRC can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
  - Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, and the Watchdog clock.
- Power control:
  - Two reduced power modes: Sleep and Deep-sleep mode.
  - Ultra-low power consumption in Deep-sleep mode ($\leq$ 1.6 μA).
  - 5 μs wake-up time from Deep-sleep mode.
  - Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 13 of the functional pins.
  - Power-On Reset (POR).
  - Brown-Out Detection (BOD) causing a forced reset.
- Unique device serial number for identification.
- Single power supply (1.65 V to 1.95 V)
- Available as WLCSP25, HVQFN24, and HVQFN33 package. Other package options are available for high-volume customers.

3. Applications

- Mobile phones
- Mobile accessories
- Cameras
- Tablets/Ultra books
- Active cables
- Portable medical electronics

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1101LVUK	WLCSP25	wafer level chip-size package; 25 bumps; 2.17 × 2.32 × 0.56 mm	-
LPC1102LVUK	WLCSP25	wafer level chip-size package; 25 bumps; 2.17 × 2.32 × 0.56 mm	-
LPC1112LVFHN24/003	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm	SOT616-3
LPC1114LVFHN24/103	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm	SOT616-3

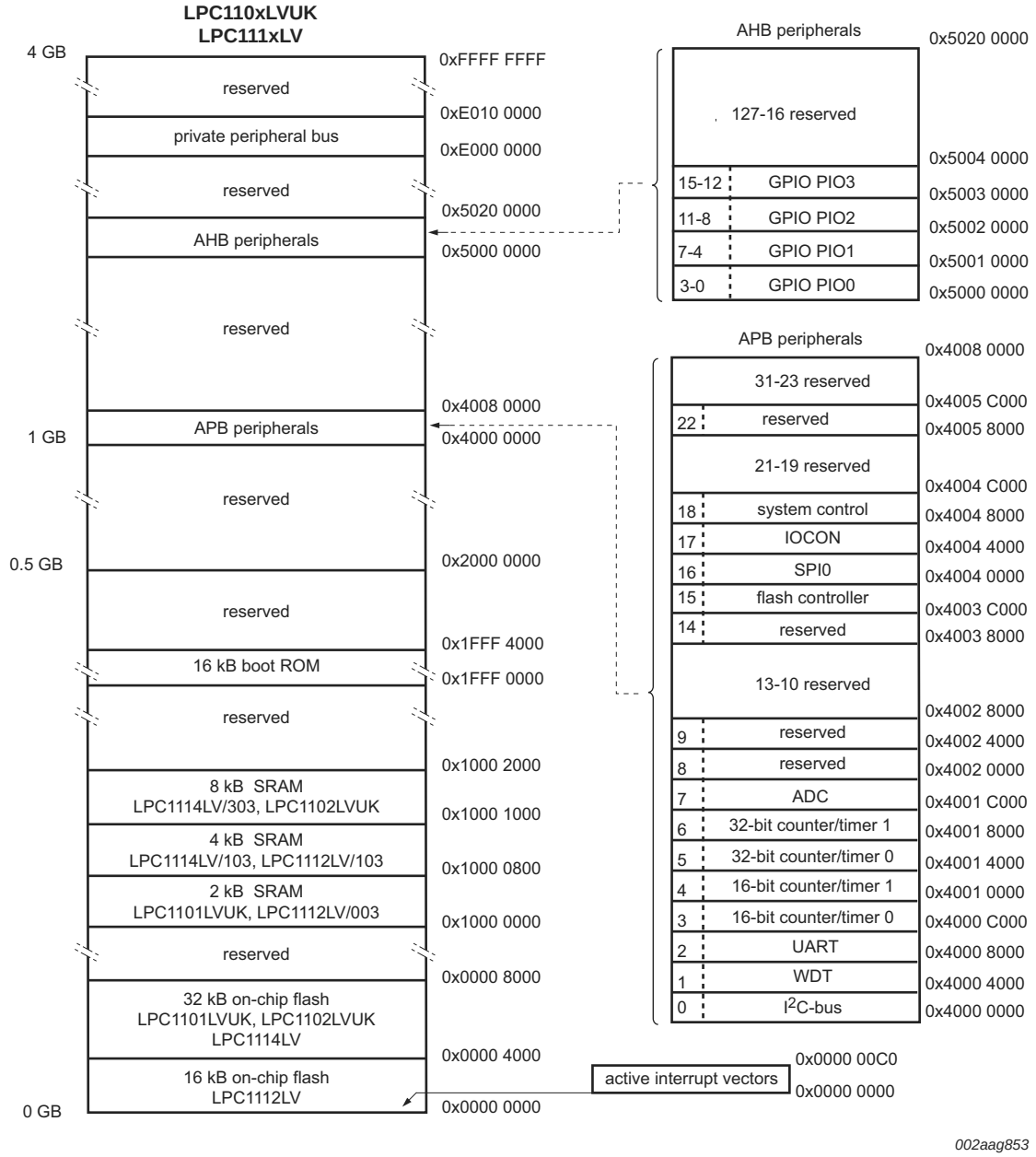


Fig 5. LPC111xLV/LPC11xxLVUK memory map

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.

- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

7.15 Clocking and power control

7.15.1 Crystal oscillators

The LPC111xLV/LPC11xxLVUK include three independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), and the Watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC111xLV/LPC11xxLVUK will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 6 for an overview of the LPC111xLV/LPC11xxLVUK clock generation.

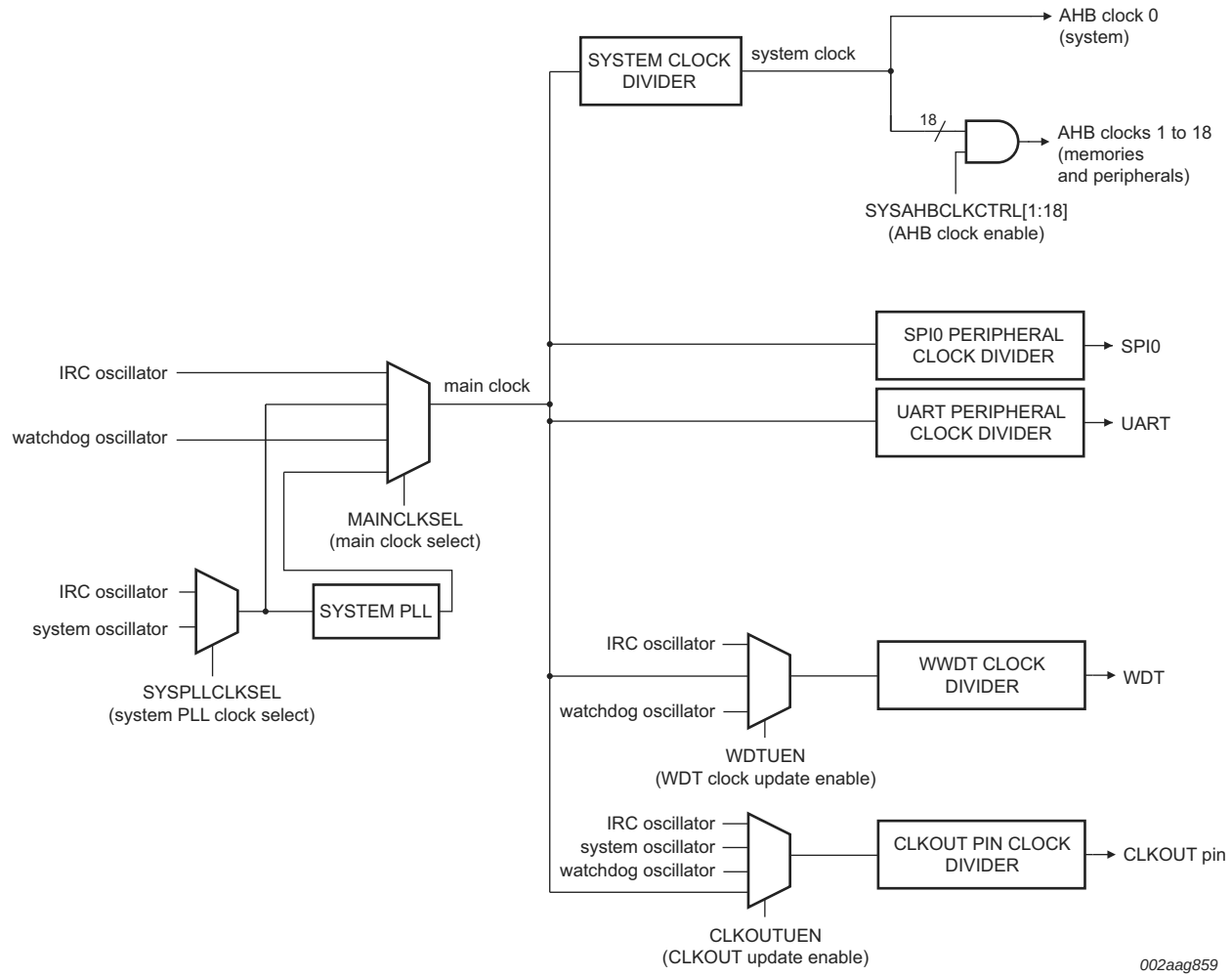


Fig 6. LPC111xLV/LPC11xxLVUK clock generation block diagram

7.15.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 2.5 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC111xLV/LPC11xxLVUK use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.15.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

7.15.5.2 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down. As an exception, the user has the option to keep the IRC, the BOD, and the watchdog timer/watchdog oscillator running for self-timed wake-up. Deep-sleep mode allows for additional power savings.

Up to 13 pins can serve as external wake-up pins to the start logic to wake up the chip from Deep-sleep mode.

Unless the watchdog oscillator or the IRC are selected to run in Deep-sleep mode, the clock source should be switched to IRC before entering Deep-sleep mode, because the IRC can be switched on and off glitch-free.

7.16 System control

7.16.1 Start logic

The start logic connects external pins to corresponding interrupts in the NVIC. Each pin shown in Table 3 as input to the start logic is connected to an individual interrupt in the NVIC interrupt vector table. The start logic pins can serve as external interrupt pins when the chip is in Active mode. In addition, an input signal on the start logic pins can wake up the chip from Deep-sleep mode when all clocks are shut down.

The start logic must be configured in the system configuration block and in the NVIC before being used.

7.16.2 Reset

Reset has four sources on the LPC111xLV/LPC11xxLVUK: the $\overline{\text{RESET}}$ pin, the Watchdog reset, the BrownOut Detection (BOD) circuit, and Power-On Reset (POR). The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

7.16.3 BrownOut Detection (BOD)

The LPC111xLV/LPC11xxLVUK includes a BOD circuit which monitors the voltage level on the V_{DD} pin. If this voltage falls below a fixed level (see Table 8), the BOD asserts a chip reset.

7.16.4 Code security (Code Read Protection - CRP)

This feature of the LPC111xLV/LPC11xxLVUK allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details see the *LPC111xLV user manual*.

Table 5. Static characteristics (single power supply *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[10]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[10]	-	-	50	mA
I_{pd}	pull-down current	V_I = 1.8 V (V_{DD} = 1.8 V)		10	29	90	μA
I_{pu}	pull-up current	V_I = 0 V; 1.65 V ≤ V_{DD} ≤ 1.95 V		−3	−13	−85	μA
		$V_{DD} < V_I < 3.0$ V		0	0	0	μA
High-drive output pin (PIO0_7)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function;	[8][9]				
		V_{DD} = 1.8 V		0	-	3.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	1.65 V ≤ V_{DD} ≤ 1.95 V; I_{OH} = 10 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	1.65 V ≤ V_{DD} ≤ 1.95 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$ − 0.4 V; 1.65 V ≤ V_{DD} ≤ 1.95 V		10	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 1.65 V ≤ V_{DD} ≤ 1.95 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[10]	-	-	50	mA
I_{pd}	pull-down current	V_I = 1.8 V		10	29	90	μA
I_{pu}	pull-up current	V_I = 0 V; 1.65 V ≤ V_{DD} ≤ 1.95 V		−3	−13	−85	μA
		$V_{DD} < V_I < 3.0$ V		0	0	0	μA

Table 6. 8-bit ADC static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for HVQFN33 and WLCSP25 packages. T_{amb} = −10 °C to +85 °C for the HVQFN24 package. V_{DD} = 1.8 V ± 5 %; 8-bit resolution.

Symbol	Parameter		Min	Typ	Max	Unit
E_G	gain error	[5]	-	-	± 2	LSB
$f_{clk(ADC)}$	ADC clock frequency		-	-	110	kHz
f_s	sampling rate		-	-	10	kSamples/s
R_{vsi}	voltage source interface resistance		-	-	40	kΩ
R_i	input resistance	[6][7]	-	-	2.5	MΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 7.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 7.

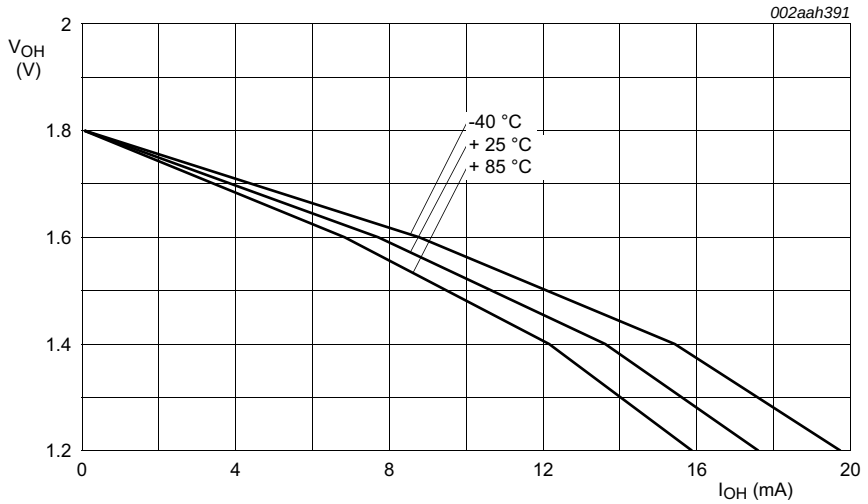
[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 7.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 7.

[6] T_{amb} = 25 °C; maximum sampling frequency f_s = 10 kSamples/s and analog input capacitance C_{ia} = 1 pF.

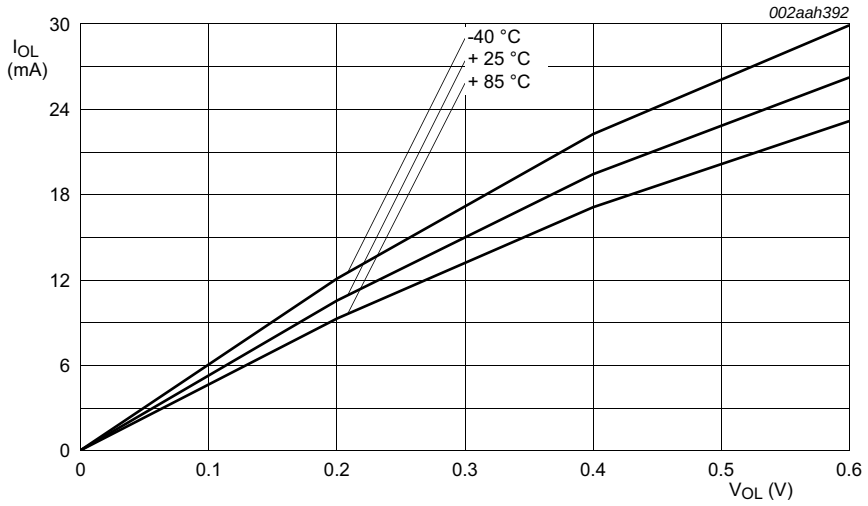
[7] Input resistance R_i depends on the sampling frequency fs: $R_i = 1 / (f_s \times C_{ia})$.

9.2 Electrical pin characteristics



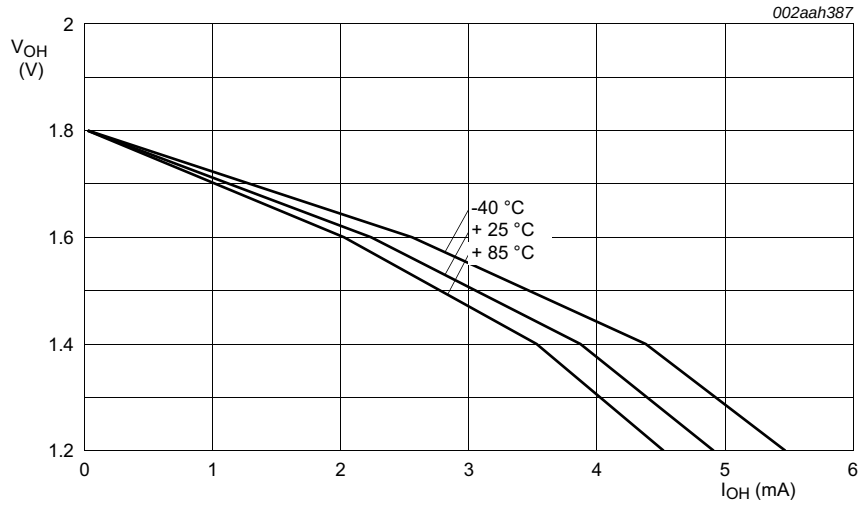
Conditions: high-drive pin PIO0_7; V_{DD} = 1.8 V.

Fig 8. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}.



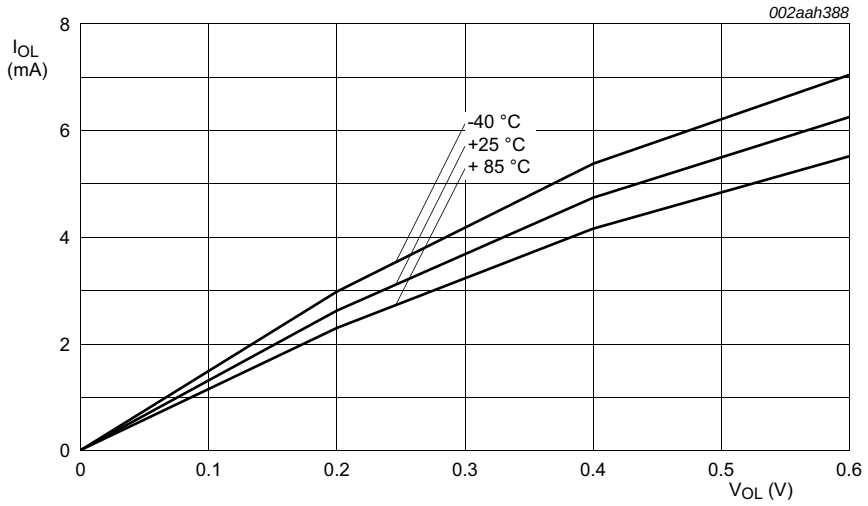
Conditions: I^2C-bus pins PIO0_4 and PIO0_5; V_{DD} = 1.8 V; configured for Fast mode plus in the IOCON PIO0_4 and PIO0_5 registers.

Fig 9. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



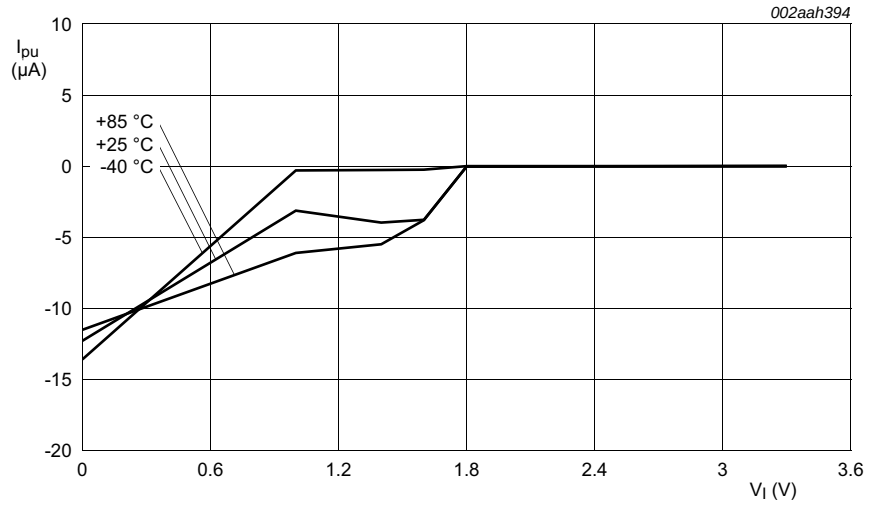
Conditions: standard port pins; V_{DD} = 1.8 V.

Fig 10. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



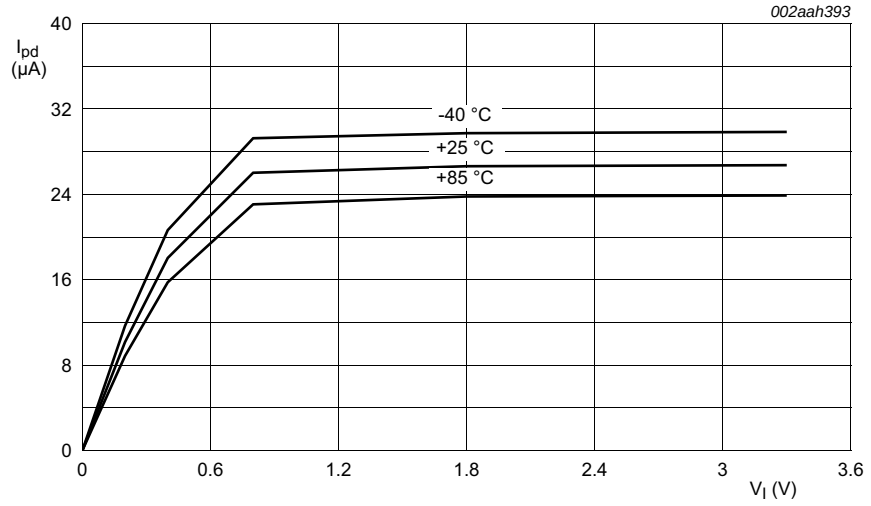
Conditions: standard port pins; V_{DD} = 1.8 V.

Fig 11. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: standard port pins; V_{DD} = 1.8 V.

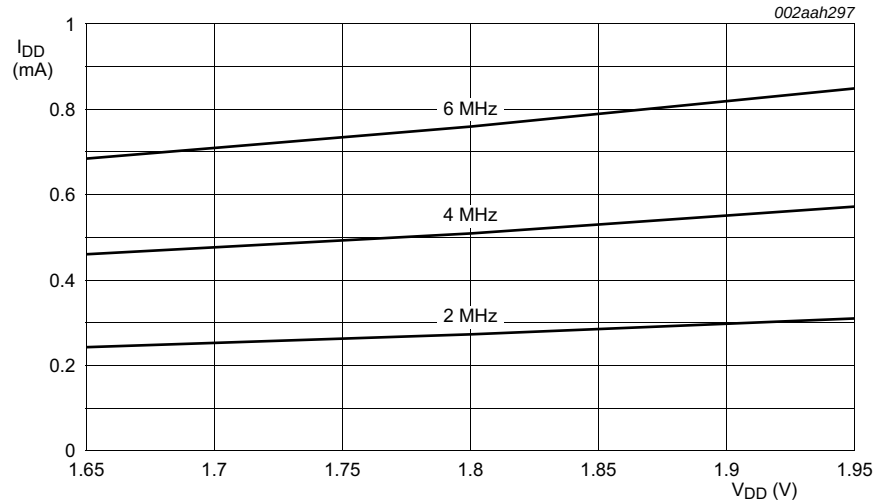
Fig 12. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: standard port pins; V_{DD} = 1.8 V.

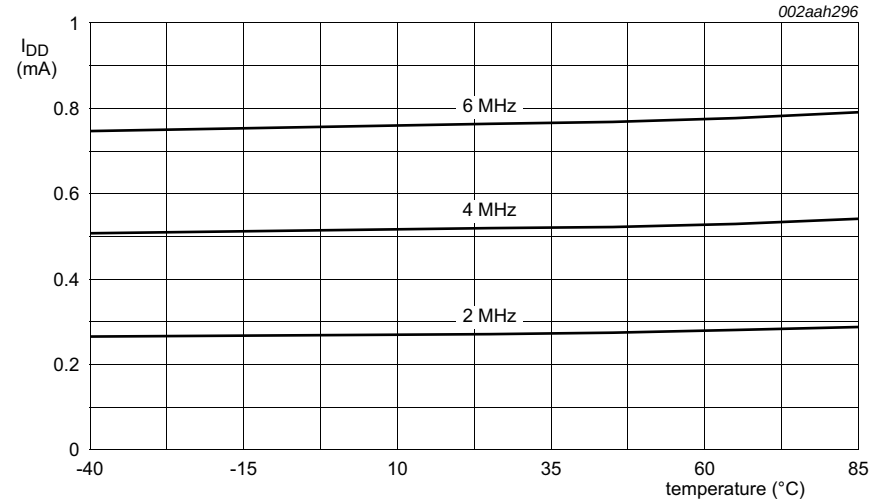
Fig 13. Typical pull-down current I_{pd} versus input voltage V_I

9.3 Power consumption



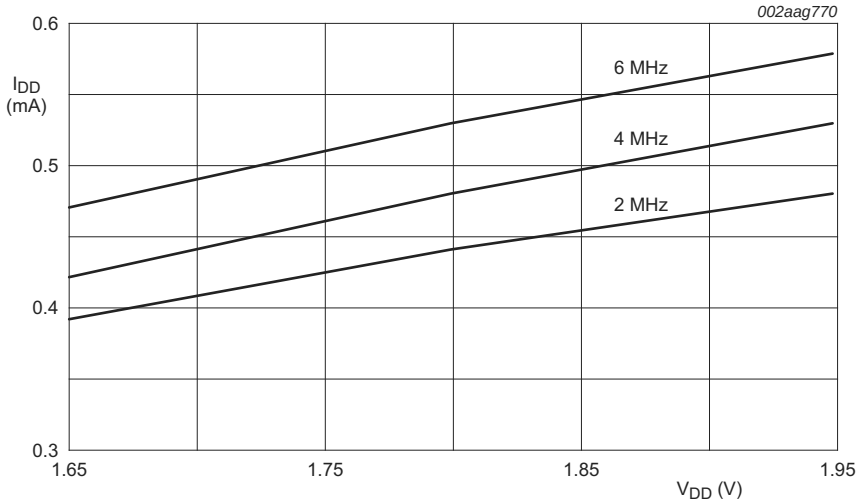
Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; System oscillator, system PLL, IRC, BOD disabled; system clock provided by external clock.

Fig 14. Active mode (2 MHz to 6 MHz): Typical supply current I_{DD} versus supply voltage V_{DD} for different clock frequencies



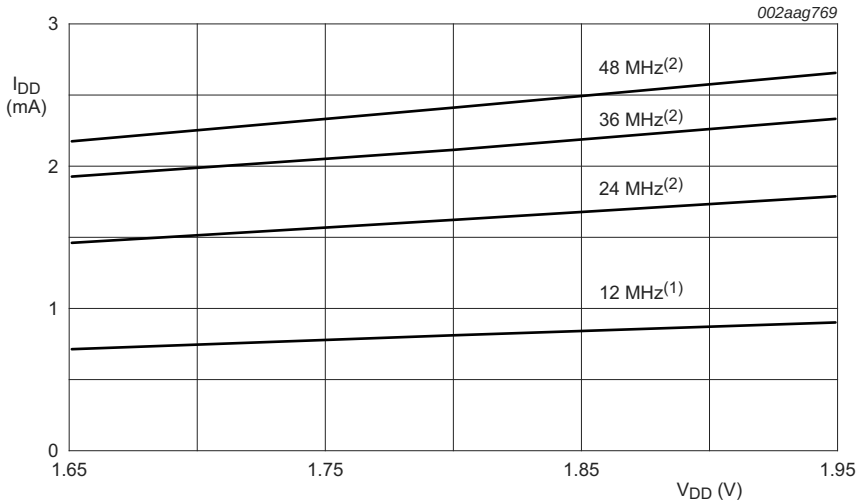
Conditions: V_{DD} = 1.8 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; System oscillator, system PLL, IRC, BOD disabled; system clock provided by external clock.

Fig 15. Active mode (2 MHz to 6 MHz): Typical supply current I_{DD} versus temperature for different clock frequencies



Conditions: T_{amb} = 25 °C; Sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; System oscillator and system PLL disabled; IRC disabled; system clock provided by external clock.

Fig 18. Sleep mode (2 MHz to 6 MHz): Typical supply current I_{DD} versus supply voltage V_{DD} for different clock frequencies



Conditions: T_{amb} = 25 °C; Sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 19. Sleep mode (12 MHz to 48 MHz): Typical supply current I_{DD} versus supply voltage V_{DD} for different clock frequencies

10.3 Internal oscillators

Table 11. Dynamic characteristic: internal oscillators
V_{DD} = 1.65V to 1.95 V.

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	*-20 °C ≤ T_{amb} ≤ +85 °C*	12 - 2.5 %	12	12 + 2.5 %	MHz
		-40 °C ≤ T_{amb} < -20 °C	12 - 5 %	12	12 + 5 %	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

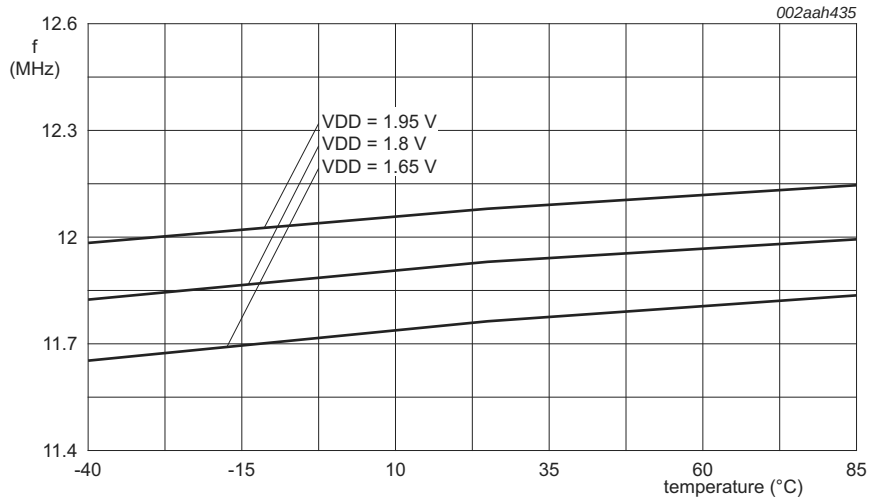


Fig 23. Typical internal RC oscillator frequency for different supply voltages V_{DD}

Table 12. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +85 °C) is ±40 %.

[3] See the *LPC111xLV user manual*.

10.4 I²C-bus

Table 13. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus	0	1	MHz

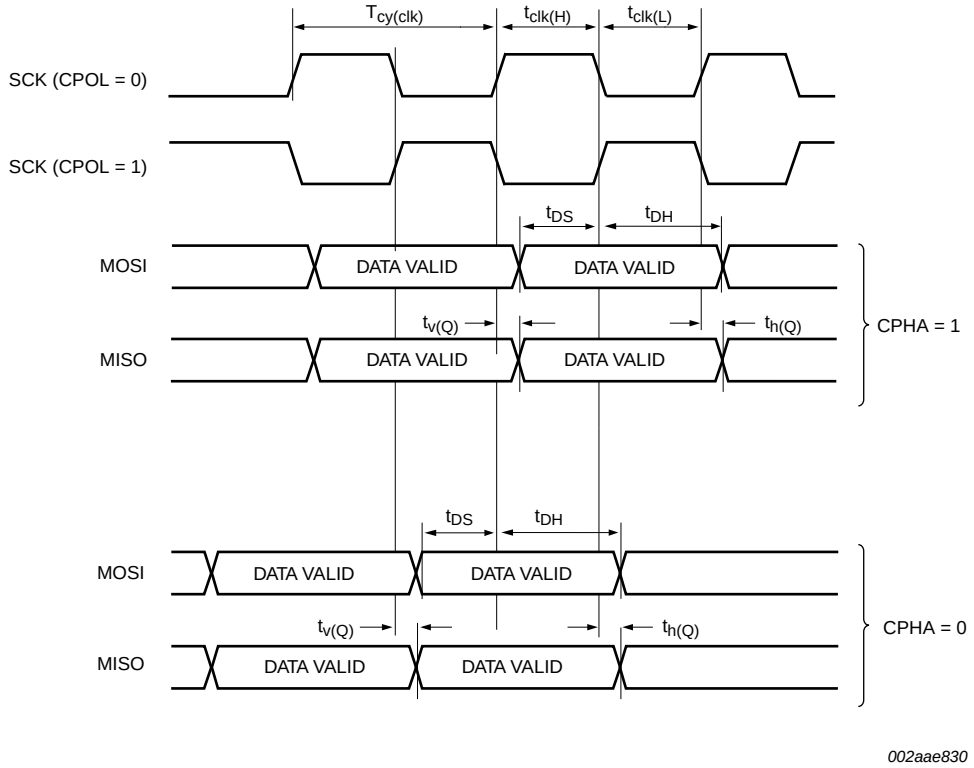


Fig 26. SPI slave timing in SPI mode

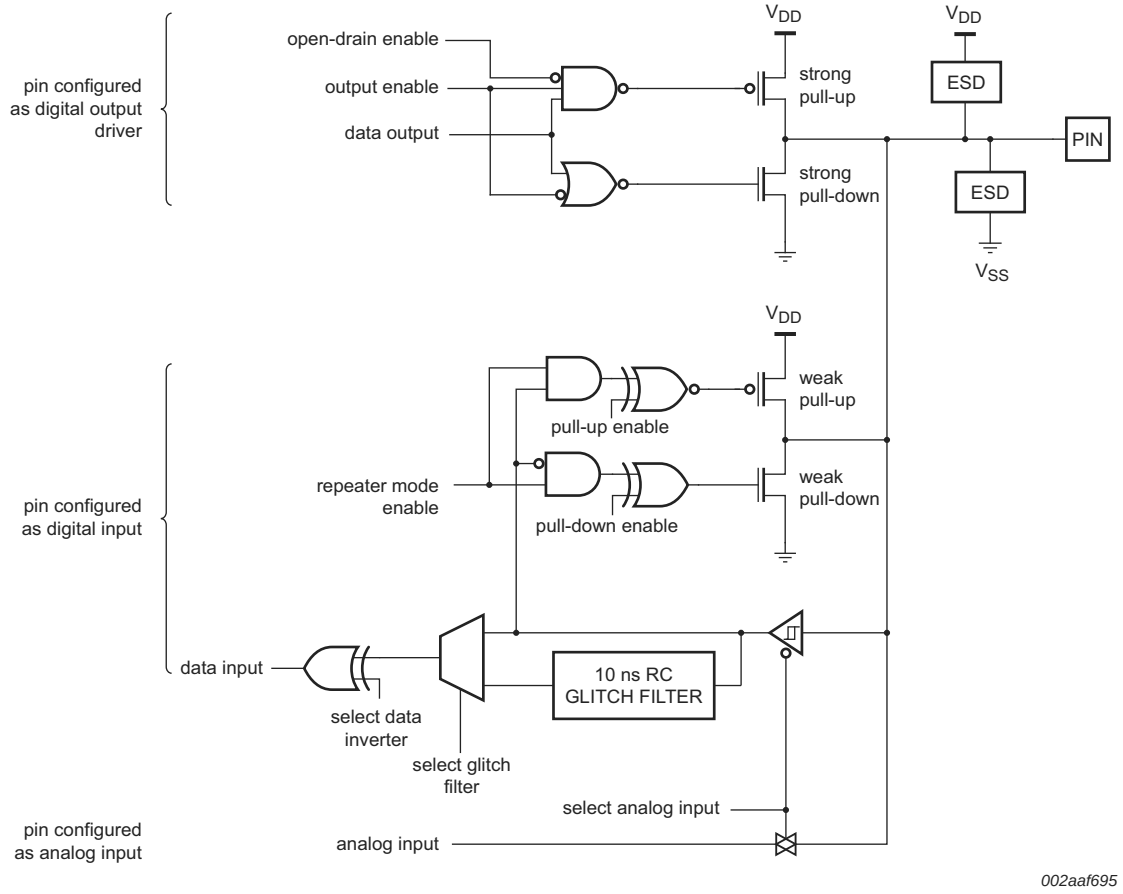


Fig 27. Standard I/O pad configuration

11.3 Reset pad configuration

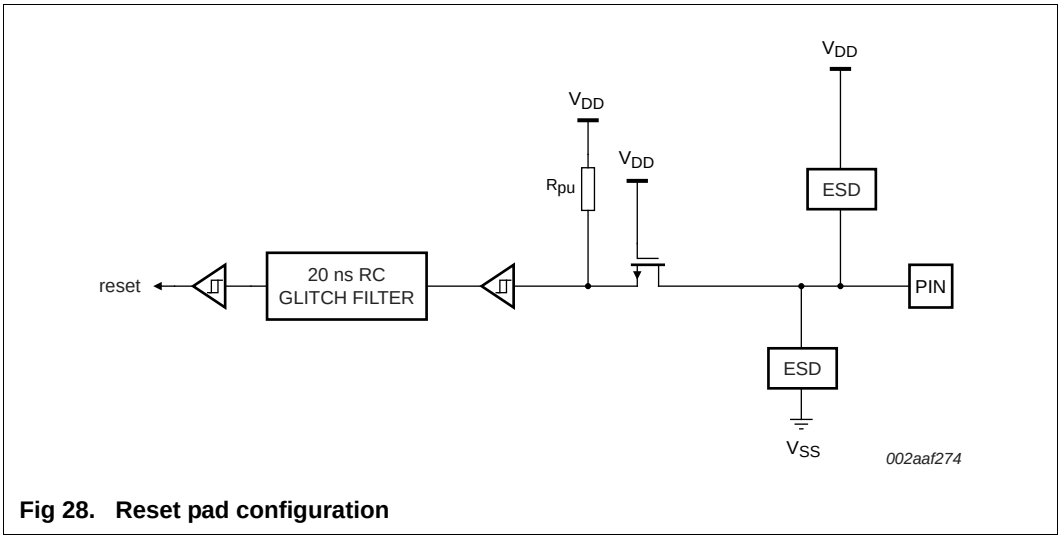
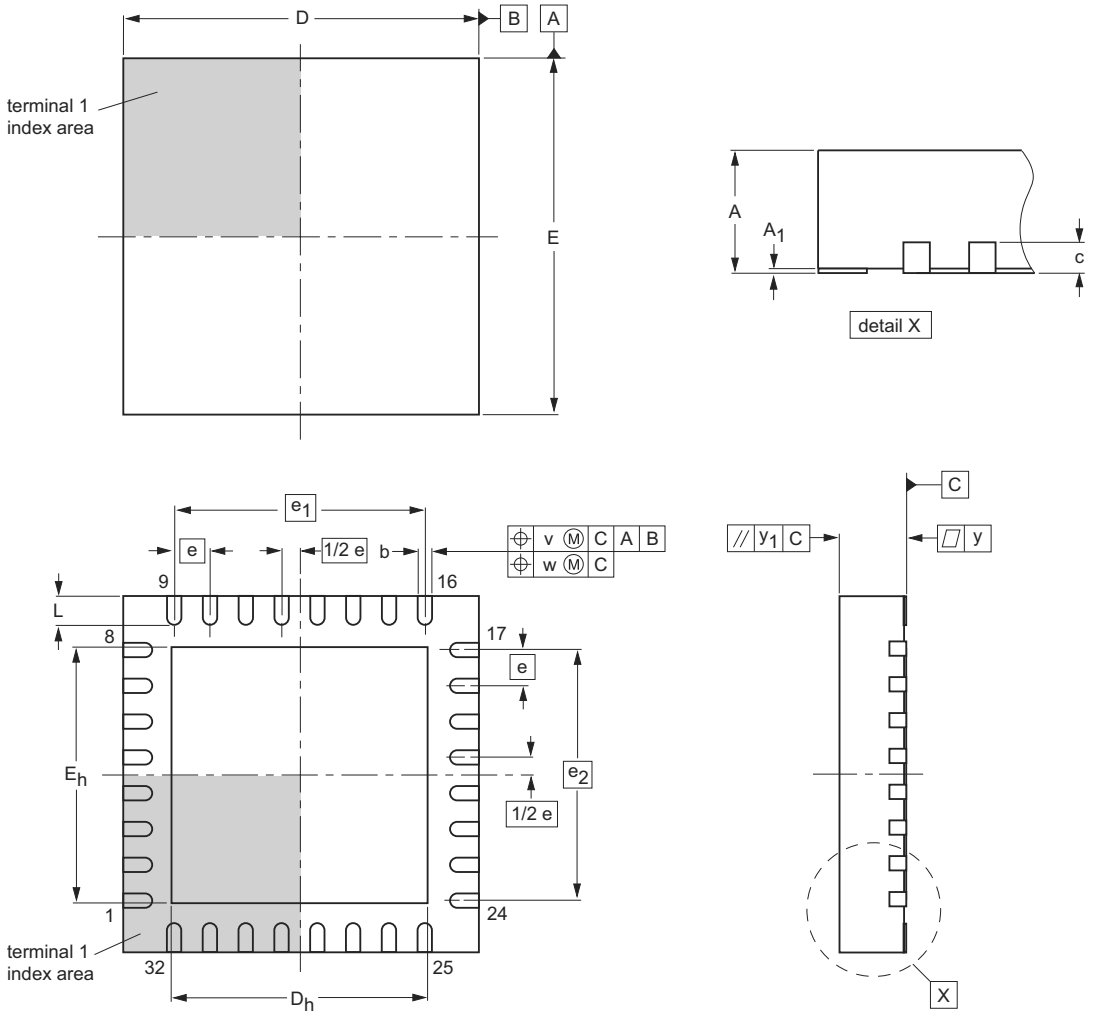


Fig 28. Reset pad configuration

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm



Dimensions (mm are the original dimensions)

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

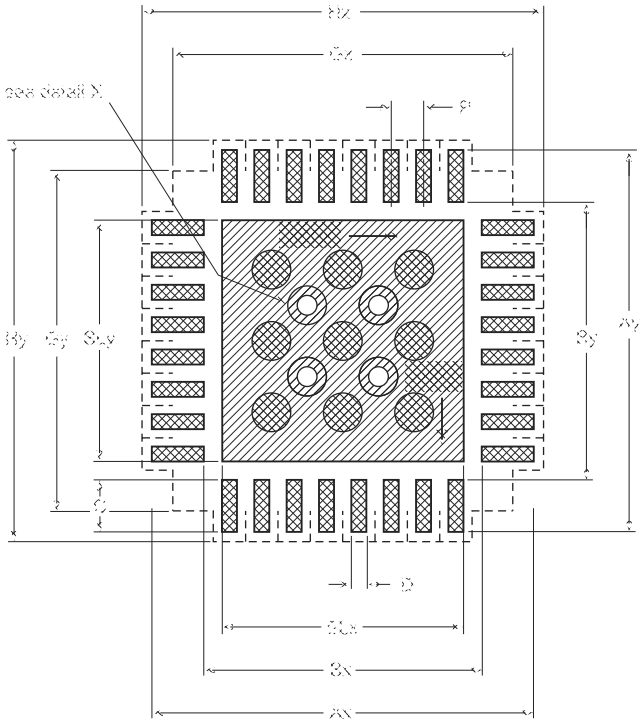
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

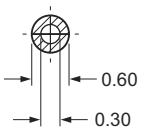
hvqfn33f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		MO-220				~~11-10-11~~ 11-10-17

Fig 31. Package outline (HVQFN33)

Footprint information for reflow soldering of HVQFN33 package





detail X

solder land

solder paste

occupied area

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

002aag766

Fig 33. Reflow soldering for the HVQFN33 (5x5) package

14. Abbreviations

Table 15. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	Brown-Out Detect
GPIO	General-Purpose Input/Output
JEDEC	Joint Electron Devices Engineering Council
NVM	Non-Volatile Memory
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
TTL	Transistor-Transistor Logic
USART	Universal Synchronous Asynchronous Receiver/Transmitter

15. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC111XLV_LPC11XXLVUK v.2	20121010	Product data sheet	-	LPC111XLV_LPC11XXLVUK v.1
Modifications:	• Functions CT16B0_CAP1/RXD added to pin PIO3_4. • Functions CT16B1_CAP1/TXD added to pin PIO3_5. • Function CT32B1_CAP1 added to pin PIO1_11. • Capture/clear functionality added to counter/timers. See Section 7.12. • Figure 21 “Deep-sleep mode: Typical supply current I_{DD} versus temperature” updated. • Electrical pin characteristics data combined in Section 9.2 for dual and single power supplies. • SSP timing characteristics in slave mode removed for single power supply parts in Table 14. • Table 11 “Dynamic characteristic: internal oscillators” and Figure 23 updated. • Figure 33 corrected. • Removed dual-power supply option. All parts use a single 1.8 V +/- 10 % power supply. • Removed 10-bit ADC. Only the 8-bit ADC is available. • Temperature range for ADC characteristics on the HVQFN24 package restricted to T_{amb} = -10 °C to +85 °C. • BOD interrupt level 0 removed in Table 8. • IRC accuracy updated to 2.5 % accuracy for T_{amb} = -20 °C to +85 °C and to 5 % accuracy for T_{amb} = -40 °C to -20 °C. • Data sheet status changed to Product data sheet.			
LPC111XLV_LPC11XXLVUK v.1	20120621	Objective data sheet	-	-

19. Contents

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