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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 6x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	25-UFBGA, WLCSP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1102lvukz

Table 1. Ordering information *…continued*

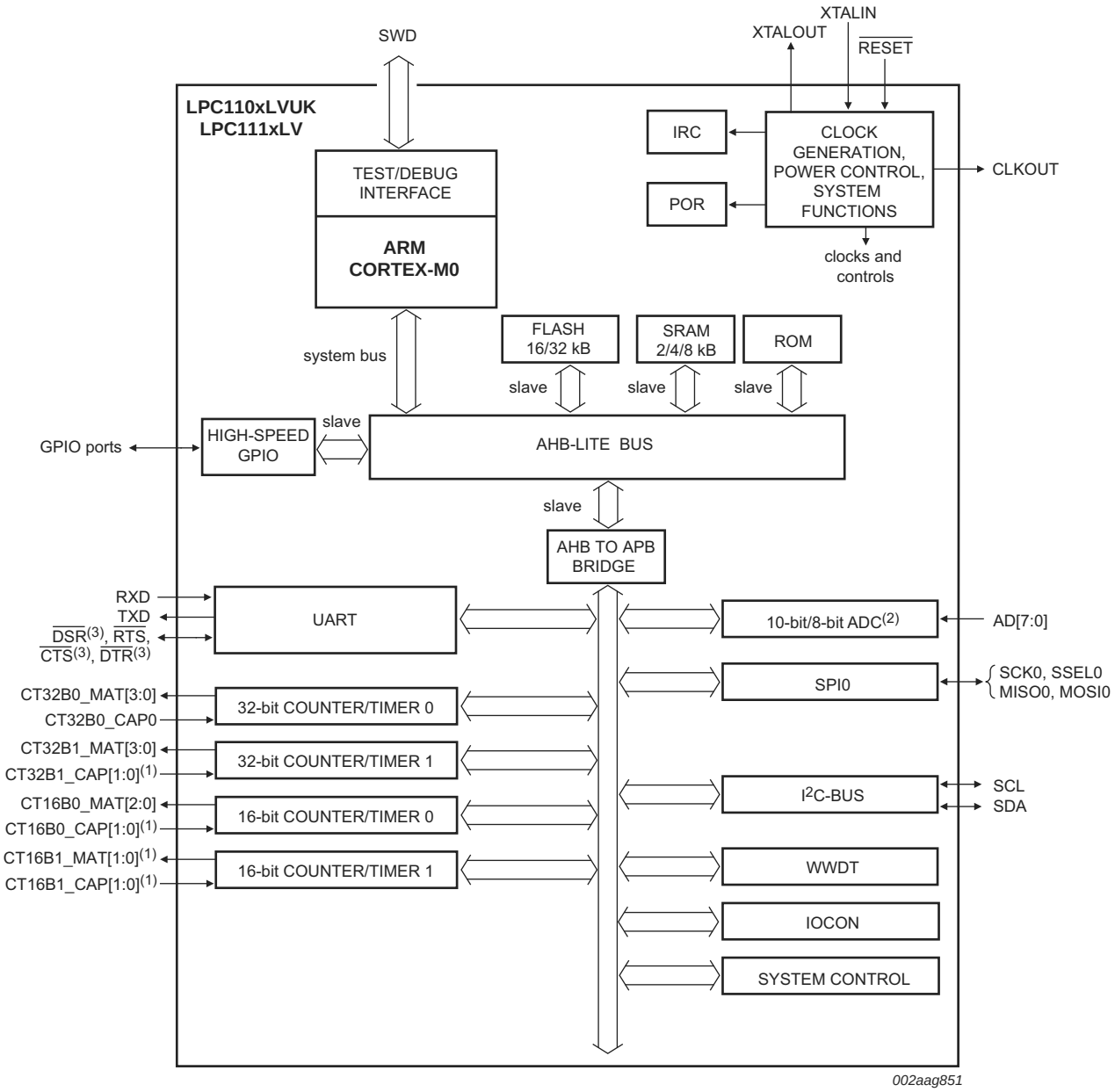
Type number	Package		
	Name	Description	Version
LPC1114LVFHN24/303	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm	SOT616-3
LPC1112LVFHI33/103	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1114LVFHI33/303	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a

4.1 Ordering options

Table 2. Ordering options

Type number	Flash in kB	Total SRAM in kB	SPI/ SSP	I2C	UART	ADC	GPIO pins	Package
LPC1101LVUK	32	2	1	1	1	6-channel	21	WLCSP25
LPC1102LVUK	32	8	1	1	1	6-channel	21	WLCSP25
LPC1112LVFHN24/003	16	2	1	1	1	6-channel	20	HVQFN24
LPC1114LVFHN24/103	32	4	1	1	1	6-channel	20	HVQFN24
LPC1114LVFHN24/303	32	8	1	1	1	6-channel	20	HVQFN24
LPC1112LVFHI33/103	16	4	1	1	1	8-channel	27	HVQFN33
LPC1114LVFHI33/303	32	8	1	1	1	8-channel	27	HVQFN33

5. Block diagram



(1) CT16B1_MAT1, CT32B1_CAP1, CT1B0_CAP1, CT16B1_CAP1 available on HVQFN33 only. CT16B1_MAT0 available on HVQFN33 and WLCSP25 packages only.

(2) 6 channels on WLCSP25 and HVQFN24 packages. 8 channels on HVQFN33 packages.

(3) $\overline{\text{DSR}}$ on WLCSP25 package only. $\overline{\text{DTR}}$ on HVQFN33 package only. $\overline{\text{CTS}}$ on HVQFN24 and HVQFN33 packages only.

Fig 1. LPC111xLV/LPC11xxLVUK block diagram

6. Pinning information

6.1 Pinning

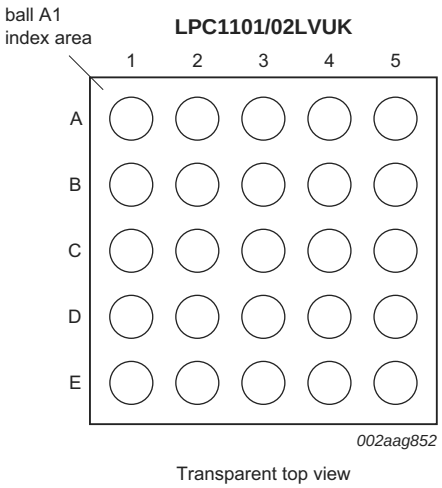


Fig 2. Pin configuration WLCSP25 package

6.2 Pin description

Table 3. LPC110xLVUK/LPC111xLV pin description table

Symbol	WLCSP25	HVQFN24	HVQFN33		Start logic input	Type	Reset state [1]	Description
$\overline{\text{RESET}}$/PIO0_0	D1	2	2	[2]	yes	I	I; PU	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
						I/O	-	**PIO0_0 —** General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	C3	3	3	[3]	yes	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
						O	-	**CLKOUT —** Clockout pin.
						O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	B2	7	8	[3]	yes	I/O	I; PU	**PIO0_2 —** General purpose digital input/output pin.
						I/O	-	**SSEL0 —** Slave Select for SPI0.
						I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	-	-	9	[3]	yes	I/O	I;PU	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/SCL	A2	8	10	[4]	yes	I/O	I; IA	**PIO0_4 —** General purpose digital input/output pin (open-drain).
						I/O	-	**SCL —** I^2C-bus, open-drain clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	A3	9	11	[4]	yes	I/O	I; IA	**PIO0_5 —** General purpose digital input/output pin (open-drain).
						I/O	-	**SDA —** I^2C-bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	A4	10	15	[3]	yes	I/O	I; PU	**PIO0_6 —** General purpose digital input/output pin.
						I/O	-	**SCK0 —** Serial clock for SPI0.
PIO0_7/$\overline{\text{CTS}}$	-	11	16	[3]	yes	I/O	I; PU	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
						I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	A5	12	17	[3]	yes	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
						I/O	-	**MISO0 —** Master In Slave Out for SPI0.
						O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	B5	13	18	[3]	yes	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
						I/O	-	**MOSI0 —** Master Out Slave In for SPI0.
						O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.

Table 3. LPC110xLVUK/LPC111xLV pin description table

Symbol	WLCSP25	HVQFN24	HVQFN33		Start logic input	Type	Reset state [1]	Description
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	B4	14	19	[3]	yes	I	I; PU	**SWCLK —** Serial wire clock.
						I/O	-	**PIO0_10 —** General purpose digital input/output pin.
						I/O	-	**SCK0 —** Serial clock for SPI0.
						O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	C5	15	21	[5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCON block.
						I/O	-	**PIO0_11 —** General purpose digital input/output pin.
						I	-	**AD0 —** A/D converter, input 0.
						O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
R/PIO1_0/ AD1/CT32B1_CAP0	C4	16	22	[5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCON block.
						I/O	-	**PIO1_0 —** General purpose digital input/output pin.
						I	-	**AD1 —** A/D converter, input 1.
						I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	D5	17	23	[5]	no	O	I; PU	**R —** Reserved. Configure for an alternate function in the IOCON block.
						I/O	-	**PIO1_1 —** General purpose digital input/output pin.
						I	-	**AD2 —** A/D converter, input 2.
						O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	D4	18	24	[5]	no	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCON block.
						I/O	-	**PIO1_2 —** General purpose digital input/output pin.
						I	-	**AD3 —** A/D converter, input 3.
						O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	E5	19	25	[5]	no	I/O	I; PU	**SWDIO —** Serial wire debug input/output.
						I/O	-	**PIO1_3 —** General purpose digital input/output pin.
						I	-	**AD4 —** A/D converter, input 4.
						O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3	D3	20	26	[5]	no	I/O	I; PU	**PIO1_4 —** General purpose digital input/output pin with 10 ns glitch filter.
						I	-	**AD5 —** A/D converter, input 5.
						O	-	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0	E2	23	30	[3]	no	I/O	I; PU	**PIO1_5 —** General purpose digital input/output pin.
						O	-	**$\overline{\text{RTS}}$ —** Request To Send output for UART.
						I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	D2	24	31	[3]	no	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
						I	-	**RXD —** Receiver input for UART.
						O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.

Table 3. LPC110xLVUK/LPC111xLV pin description table

Symbol	WLCSP25	HVQFN24	HVQFN33		Start logic input	Type	Reset state [1]	Description
PIO1_7/TXD/ CT32B0_MAT1	E1	1	32	[3]	no	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
						O	-	**TXD —** Transmitter output for UART.
						O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	B1	6	7	[3]	no	I/O	I; PU	**PIO1_8 —** General purpose digital input/output pin.
						I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0	B3	-	12	[3]	no	I/O	I; PU	**PIO1_9 —** General purpose digital input/output pin.
						O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	-	-	20	[5]	no	I/O	I;PU	**PIO1_10 —** General purpose digital input/output pin.
						I	-	**AD6 —** A/D converter, input 6.
						O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_11/AD7/ CT32B0_MAT3	-	-	27	[5]	no	I/O	I;PU	**PIO1_11 —** General purpose digital input/output pin.
						I	-	**AD7 —** A/D converter, input 7.
						O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
PIO2_0/$\overline{\text{DTR}}$	-	-	1	[3]	no	I/O	I;PU	**PIO2_0 —** General purpose digital input/output pin.
						O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
PIO2_1/$\overline{\text{DSR}}$	A1	-	-	[3]	no	I/O	I; PU	**PIO2_1 —** General purpose digital input/output pin.
						I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for UART.
PIO3_4/ CT16B0_CAP1/RXD	-	-	13	[3]	no	I/O	I;PU	**PIO3_4 —** General purpose digital input/output pin.
						I	-	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0.
						I	-	**RXD —** Receiver input for UART.
PIO3_5/ CT16B1_CAP1/TXD	-	-	14	[3]	no	I/O	I;PU	**PIO3_5 —** General purpose digital input/output pin.
						I	-	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
						O	-	**TXD —** Transmitter output for UART.
V_{DD}	E3	22	29; 6; 28		-	-	-	1.8 V supply voltage to the core, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	C1	4	4	[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	C2	5	5	[6]	-	O	-	Output from the oscillator amplifier.
V_{SS}	E4	21	33		-	-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level 0; IA = inactive, no pull-up/down enabled.

[2] See Figure 28 for the reset pad configuration.

[3] Pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 27).

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus.

[5] Pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as an ADC input, digital section of the pad is disabled (see Figure 27).

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.2 On-chip flash program memory

The LPC111xLV/LPC11xxLVUK contains up to 32 kB of on-chip flash memory.

The flash memory is divided into 4 kB sectors with each sector consisting of 16 pages. Individual pages of 256 byte each can be erased using the IAP erase page command.

7.3 On-chip SRAM

The LPC111xLV/LPC11xxLVUK contains up to 8 kB on-chip static RAM memory.

7.4 Memory map

The LPC111xLV/LPC11xxLVUK incorporates several distinct memory regions, shown in the following figures. Figure 5 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 megabyte in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kilobytes of space. This allows simplifying the address decoding for each peripheral.

7.8 UART

The LPC111xLV/LPC11xxLVUK contains one UART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The UART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.8.1 Features

- Maximum UART data bit rate of 3.125 MBit/s.
- 16 Byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.

7.9 SPI serial I/O controller

The LPC111xLV/LPC11xxLVUK contains one SPI controller.

The SPI controller is capable of operation on an SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SPI supports full-duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.9.1 Features

- Maximum SPI speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.10 I^2C-bus serial I/O controller

The LPC111xLV/LPC11xxLVUK contains one I^2C-bus controller.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock Line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the

7.15.5.2 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down. As an exception, the user has the option to keep the IRC, the BOD, and the watchdog timer/watchdog oscillator running for self-timed wake-up. Deep-sleep mode allows for additional power savings.

Up to 13 pins can serve as external wake-up pins to the start logic to wake up the chip from Deep-sleep mode.

Unless the watchdog oscillator or the IRC are selected to run in Deep-sleep mode, the clock source should be switched to IRC before entering Deep-sleep mode, because the IRC can be switched on and off glitch-free.

7.16 System control

7.16.1 Start logic

The start logic connects external pins to corresponding interrupts in the NVIC. Each pin shown in Table 3 as input to the start logic is connected to an individual interrupt in the NVIC interrupt vector table. The start logic pins can serve as external interrupt pins when the chip is in Active mode. In addition, an input signal on the start logic pins can wake up the chip from Deep-sleep mode when all clocks are shut down.

The start logic must be configured in the system configuration block and in the NVIC before being used.

7.16.2 Reset

Reset has four sources on the LPC111xLV/LPC11xxLVUK: the $\overline{\text{RESET}}$ pin, the Watchdog reset, the BrownOut Detection (BOD) circuit, and Power-On Reset (POR). The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

7.16.3 BrownOut Detection (BOD)

The LPC111xLV/LPC11xxLVUK includes a BOD circuit which monitors the voltage level on the V_{DD} pin. If this voltage falls below a fixed level (see Table 8), the BOD asserts a chip reset.

7.16.4 Code security (Code Read Protection - CRP)

This feature of the LPC111xLV/LPC11xxLVUK allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details see the *LPC111xLV user manual*.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.65	1.95	V
V_I	input voltage	only valid when the V_{DD} supply voltage is present $1.65\ V \leq V_{DD} < 1.8\ V$	[2]	−0.5	+3.0	V
		$V_{DD} \geq 1.8\ V$		−0.5	+5.0	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125\ °C$		-	100	mA
T_{stg}	storage temperature	non-operating	[3]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[4]	−6500	+6500	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

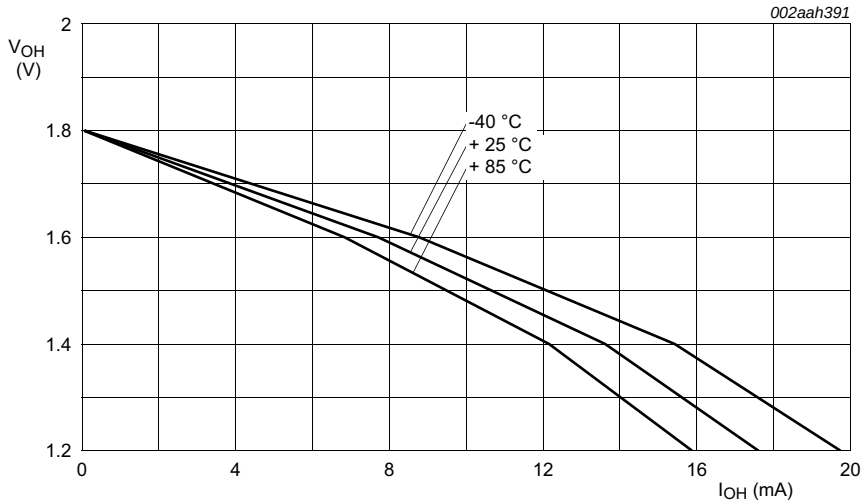
[3] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Refer to the JEDEC spec (J-STD-033B.1) for further details.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

Table 5. Static characteristics (single power supply *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

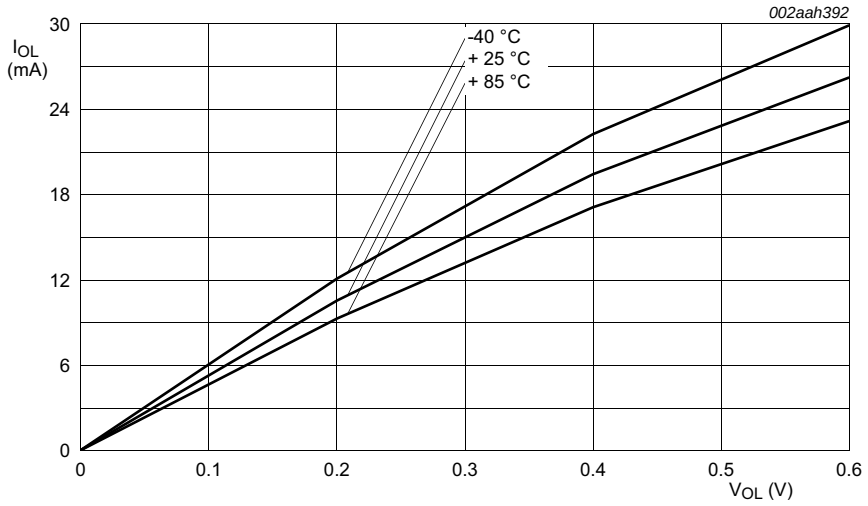
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[10]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[10]	-	-	50	mA
I_{pd}	pull-down current	V_I = 1.8 V (V_{DD} = 1.8 V)		10	29	90	μA
I_{pu}	pull-up current	V_I = 0 V; 1.65 V ≤ V_{DD} ≤ 1.95 V		−3	−13	−85	μA
		$V_{DD} < V_I < 3.0$ V		0	0	0	μA
High-drive output pin (PIO0_7)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function;	[8][9]				
		V_{DD} = 1.8 V		0	-	3.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	1.65 V ≤ V_{DD} ≤ 1.95 V; I_{OH} = 10 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	1.65 V ≤ V_{DD} ≤ 1.95 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$ − 0.4 V; 1.65 V ≤ V_{DD} ≤ 1.95 V		10	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 1.65 V ≤ V_{DD} ≤ 1.95 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[10]	-	-	50	mA
I_{pd}	pull-down current	V_I = 1.8 V		10	29	90	μA
I_{pu}	pull-up current	V_I = 0 V; 1.65 V ≤ V_{DD} ≤ 1.95 V		−3	−13	−85	μA
		$V_{DD} < V_I < 3.0$ V		0	0	0	μA

9.2 Electrical pin characteristics



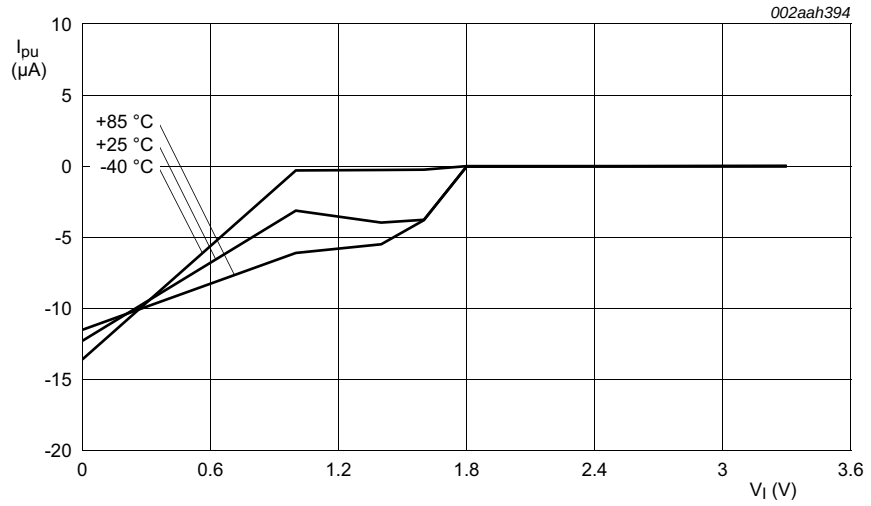
Conditions: high-drive pin PIO0_7; V_{DD} = 1.8 V.

Fig 8. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}.



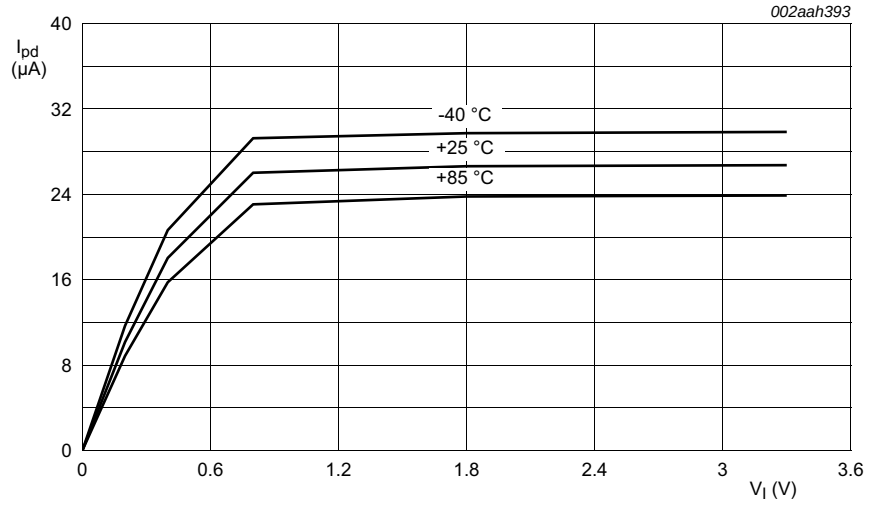
Conditions: I^2C-bus pins PIO0_4 and PIO0_5; V_{DD} = 1.8 V; configured for Fast mode plus in the IOCON PIO0_4 and PIO0_5 registers.

Fig 9. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: standard port pins; V_{DD} = 1.8 V.

Fig 12. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: standard port pins; V_{DD} = 1.8 V.

Fig 13. Typical pull-down current I_{pd} versus input voltage V_I

9.4 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

Table 7. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.26	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.18	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.004	-	-	System oscillator running; PLL off; independent of main clock frequency.
Main PLL	-	0.061	-	
ADC	-	0.08	0.29	
CLKOUT	-	0.18	0.45	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	0.02	0.06	
CT16B1	-	0.02	0.06	
CT32B0	-	0.02	0.07	
CT32B1	-	0.02	0.06	
GPIO	-	0.23	0.88	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCON	-	0.03	0.10	
I2C	-	0.04	0.13	
ROM	-	0.04	0.15	
SPI0	-	0.12	0.45	
UART	-	0.22	0.82	
WWDT	-	0.02	0.06	Main clock selected as clock source for the WWDT.

9.5 BOD static characteristics

Table 8. BOD static characteristics

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V

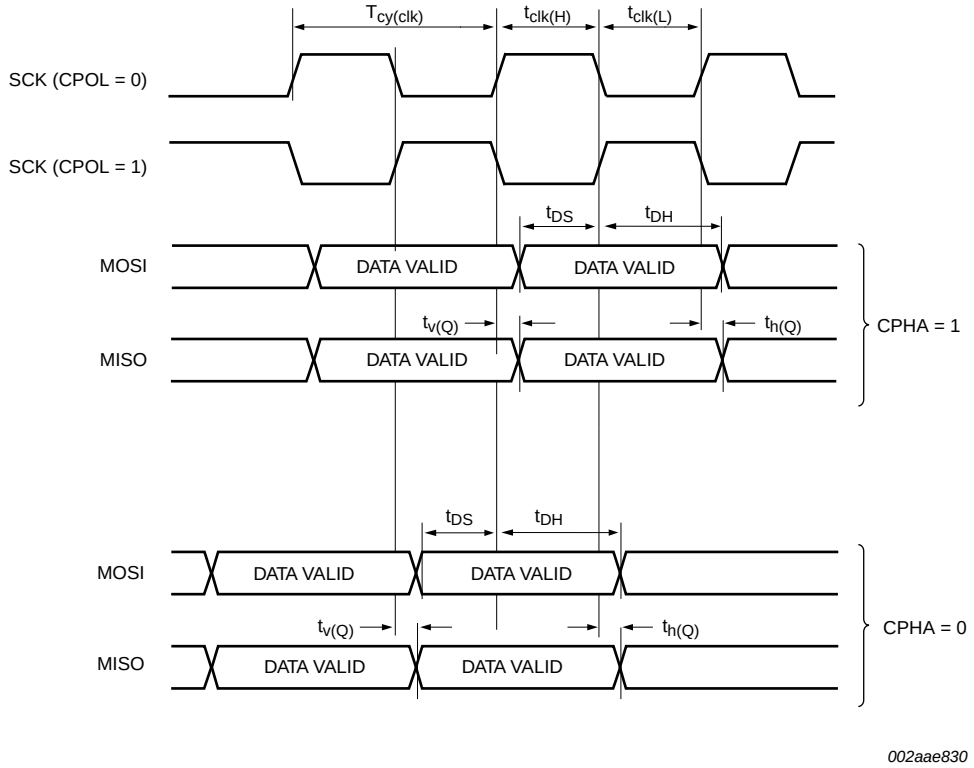


Fig 26. SPI slave timing in SPI mode

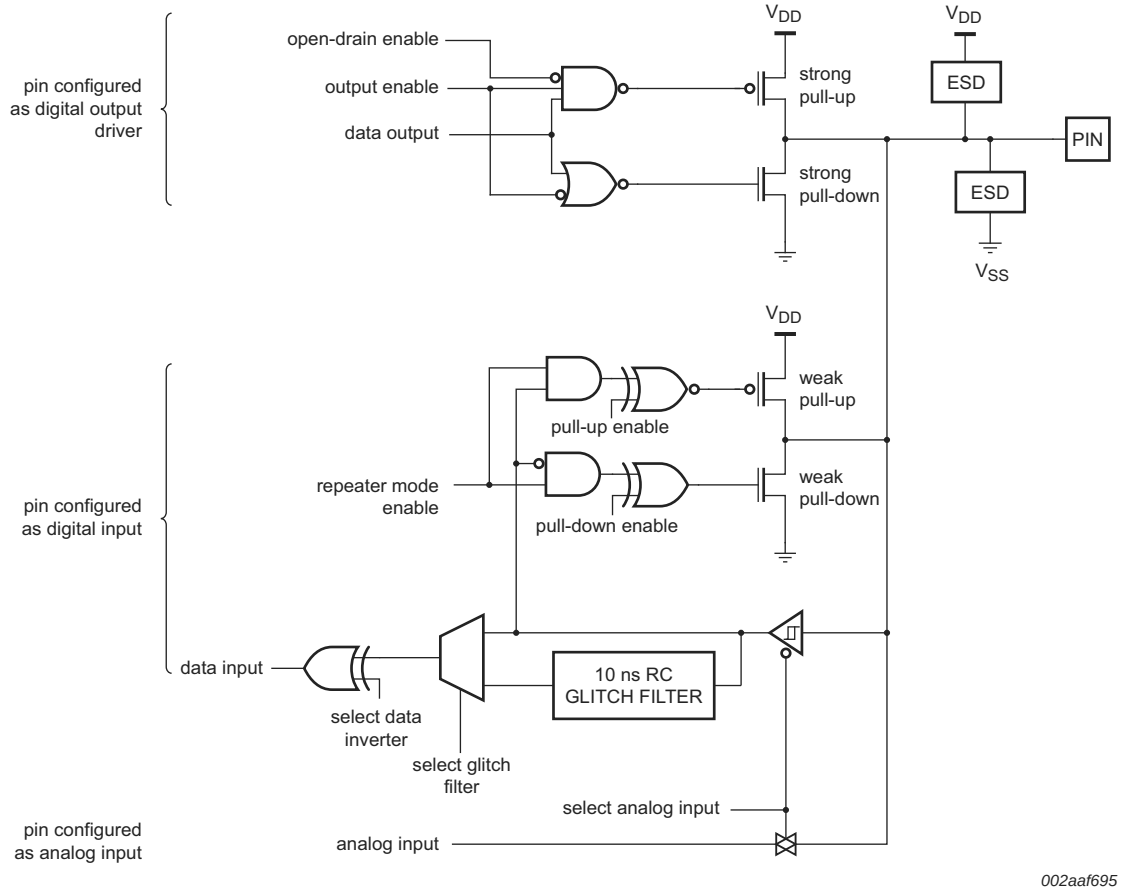


Fig 27. Standard I/O pad configuration

11.3 Reset pad configuration

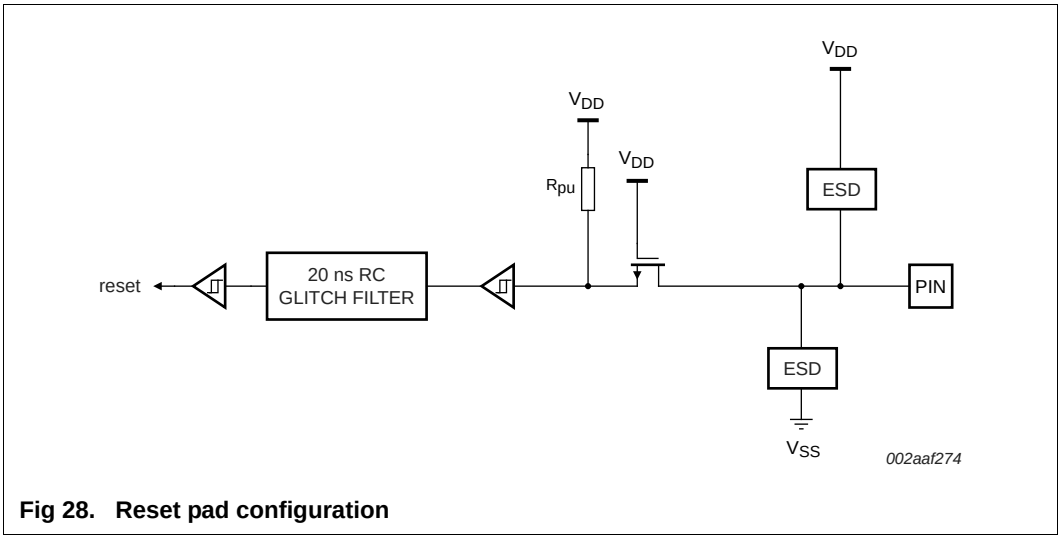
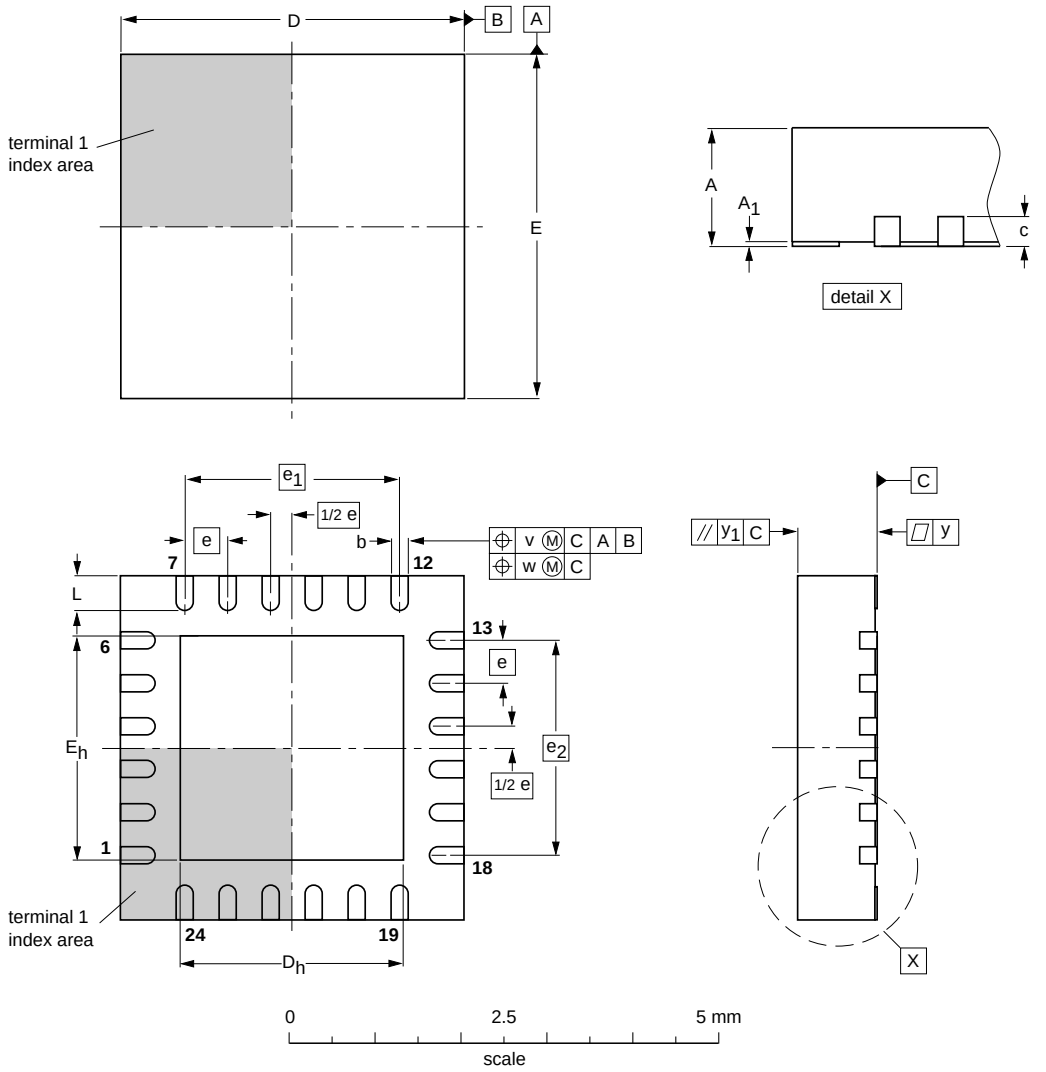


Fig 28. Reset pad configuration

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-3**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.75 2.45	4.1 3.9	2.75 2.45	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

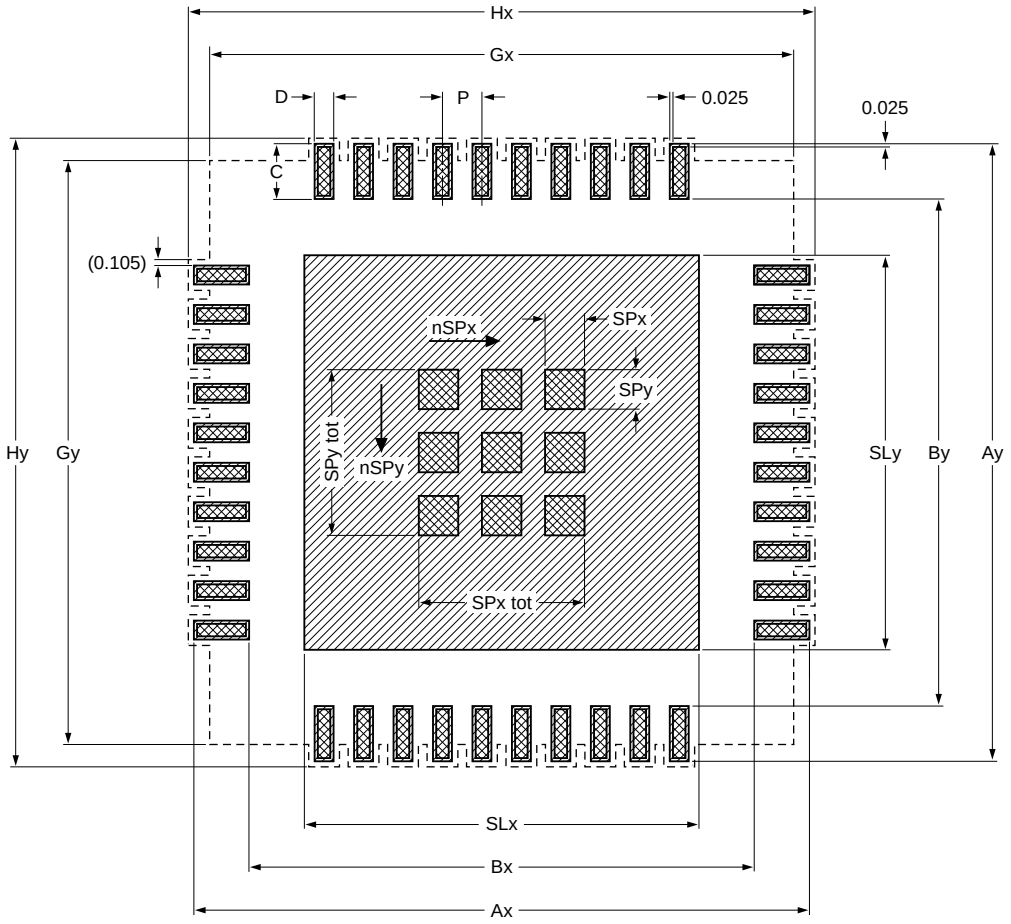
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-3	- - -	MO-220	- - -			~~04-11-19~~ 05-03-10

Fig 30. Package outline (HVQFN24)

13. Soldering

Footprint information for reflow soldering of HVQFN24 package **SOT616-3**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

nSPx	nSPy
2	2

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.500	5.000	5.000	3.200	3.200	0.900	0.240	2.500	2.500	1.500	1.500	0.550	0.550	4.300	4.300	5.250	5.250

Issue date ~~07-05-07~~ 09-06-15 *sot616-3_fr*

Fig 32. Reflow soldering for the HVQFN24 package

16. Legal information

17. Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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19. Contents

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Date of release: 10 October 2012
Document identifier: LPC111XLV_LPC11XXLVUK