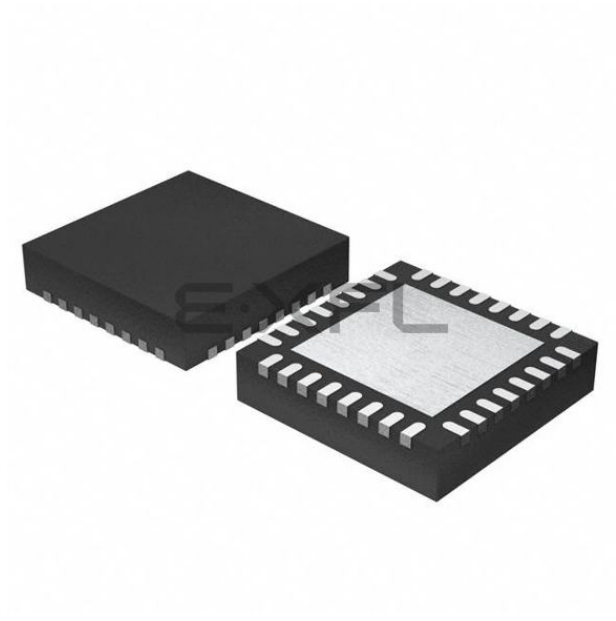

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	27
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 6x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1112lvfhi33-103

- UART with fractional baud rate generation and internal FIFO.
- One SPI controller with SSP features and with FIFO and multi-protocol capabilities.
- I^2C-bus interface supporting full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.

- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 2.5 % accuracy for T_{amb} = -20 °C to +85 °C and to 5 % accuracy for T_{amb} = -40 °C to -20 °C. The IRC can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
  - Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, and the Watchdog clock.
- Power control:
  - Two reduced power modes: Sleep and Deep-sleep mode.
  - Ultra-low power consumption in Deep-sleep mode ($\leq$ 1.6 μA).
  - 5 μs wake-up time from Deep-sleep mode.
  - Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 13 of the functional pins.
  - Power-On Reset (POR).
  - Brown-Out Detection (BOD) causing a forced reset.
- Unique device serial number for identification.
- Single power supply (1.65 V to 1.95 V)
- Available as WLCSP25, HVQFN24, and HVQFN33 package. Other package options are available for high-volume customers.

3. Applications

- Mobile phones
- Mobile accessories
- Cameras
- Tablets/Ultra books
- Active cables
- Portable medical electronics

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1101LVUK	WLCSP25	wafer level chip-size package; 25 bumps; 2.17 × 2.32 × 0.56 mm	-
LPC1102LVUK	WLCSP25	wafer level chip-size package; 25 bumps; 2.17 × 2.32 × 0.56 mm	-
LPC1112LVFHN24/003	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm	SOT616-3
LPC1114LVFHN24/103	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm	SOT616-3

Table 1. Ordering information *…continued*

Type number	Package		
	Name	Description	Version
LPC1114LVFHN24/303	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm	SOT616-3
LPC1112LVFHI33/103	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1114LVFHI33/303	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a

4.1 Ordering options

Table 2. Ordering options

Type number	Flash in kB	Total SRAM in kB	SPI/ SSP	I2C	UART	ADC	GPIO pins	Package
LPC1101LVUK	32	2	1	1	1	6-channel	21	WLCSP25
LPC1102LVUK	32	8	1	1	1	6-channel	21	WLCSP25
LPC1112LVFHN24/003	16	2	1	1	1	6-channel	20	HVQFN24
LPC1114LVFHN24/103	32	4	1	1	1	6-channel	20	HVQFN24
LPC1114LVFHN24/303	32	8	1	1	1	6-channel	20	HVQFN24
LPC1112LVFHI33/103	16	4	1	1	1	8-channel	27	HVQFN33
LPC1114LVFHI33/303	32	8	1	1	1	8-channel	27	HVQFN33

6. Pinning information

6.1 Pinning

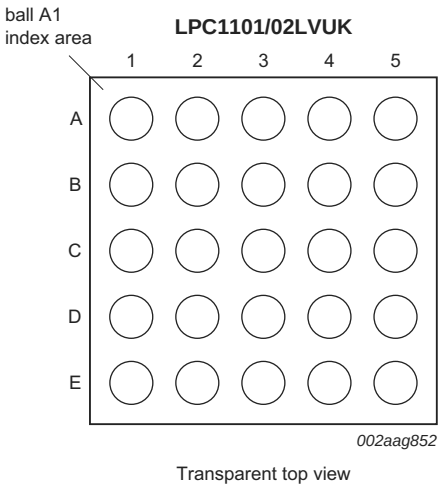
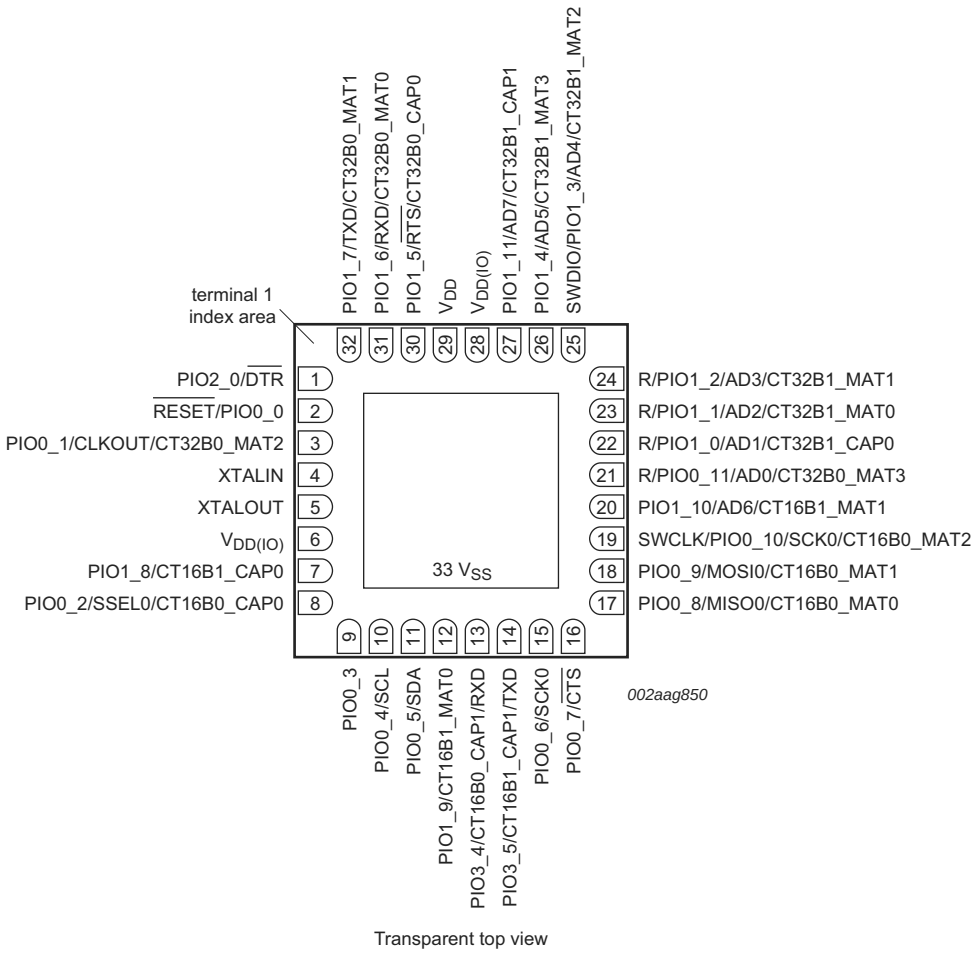


Fig 2. Pin configuration WLCSP25 package



For parts LPC1112LVFHI33/103 and LPC1114LVFHI33/303.

Fig 4. Pin configuration HVQFN33 package

capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.10.1 Features

- The I^2C-interface is a standard I^2C-bus compliant interface with open-drain pins. The I^2C-bus interface also supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- The I^2C-bus controller supports multiple address recognition and a bus monitor mode.

7.11 ADC

The LPC111xLV/LPC11xxLVUK contains one ADC. It is a single 8-bit successive approximation ADC with up to eight channels.

Remark: ADC specifications are valid for T_{amb} = -40 °C to +85 °C on HVQFN33 and WLCSP25 packages. ADC specifications are valid for T_{amb} = -10 °C to 85 °C on the HVQFN24 package.

7.11.1 Features

- 8-bit successive approximation ADC.
- Input multiplexing among 6 pins (WLCSP25 and HVQFN24 packages).
- Input multiplexing among 8 pins (HVQFN33 packages).
- Power-down mode.
- Measurement range 0 V to V_{DD}.
- 8-bit sampling rate of up to 10 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.12 General purpose external event counter/timers

The LPC111xLV/LPC11xxLVUK includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.12.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Up to two capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.13 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.14 Windowed WatchDog Timer

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.14.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via the UART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled (NO_ISP mode). For details see the *LPC111xLV user manual*.

7.16.5 APB interface

The APB peripherals are located on one APB bus.

7.16.6 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

7.16.7 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs. In addition, start logic inputs serve as external interrupts (see Section 7.16.1).

7.17 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug with four breakpoints and two watchpoints is supported.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.65	1.95	V
V_I	input voltage	only valid when the V_{DD} supply voltage is present $1.65\ V \leq V_{DD} < 1.8\ V$	[2]	−0.5	+3.0	V
		$V_{DD} \geq 1.8\ V$		−0.5	+5.0	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125\ °C$		-	100	mA
T_{stg}	storage temperature	non-operating	[3]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[4]	−6500	+6500	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Refer to the JEDEC spec (J-STD-033B.1) for further details.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

Table 6. 8-bit ADC static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for HVQFN33 and WLCSP25 packages. T_{amb} = −10 °C to +85 °C for the HVQFN24 package. V_{DD} = 1.8 V ± 5 %; 8-bit resolution.

Symbol	Parameter		Min	Typ	Max	Unit
E_G	gain error	[5]	-	-	± 2	LSB
$f_{clk(ADC)}$	ADC clock frequency		-	-	110	kHz
f_s	sampling rate		-	-	10	kSamples/s
R_{vsi}	voltage source interface resistance		-	-	40	kΩ
R_i	input resistance	[6][7]	-	-	2.5	MΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 7.

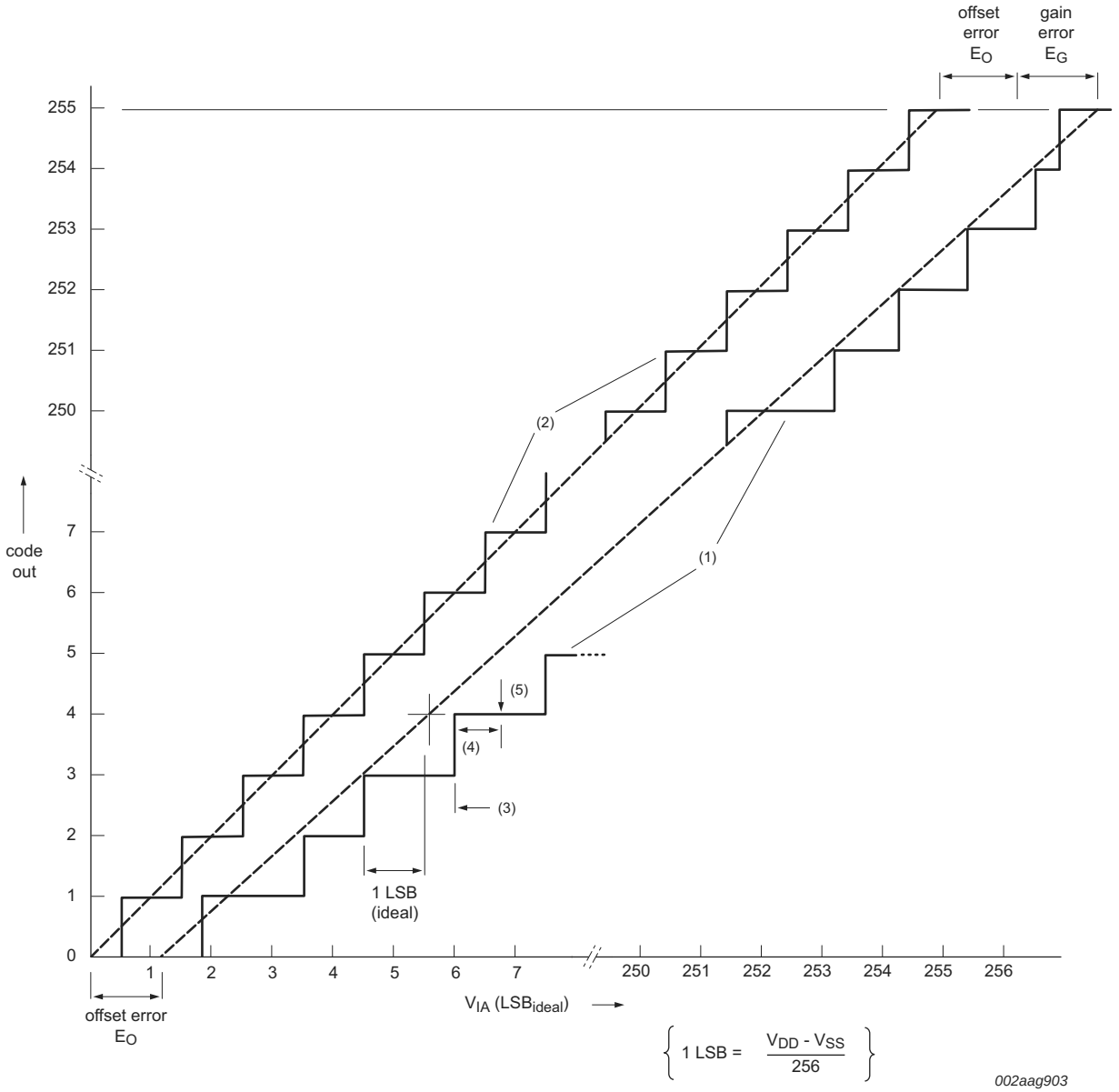
[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 7.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 7.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 7.

[6] T_{amb} = 25 °C; maximum sampling frequency f_s = 10 kSamples/s and analog input capacitance C_{ia} = 1 pF.

[7] Input resistance R_i depends on the sampling frequency fs: $R_i = 1 / (f_s \times C_{ia})$.



(1) Example of an actual transfer curve.

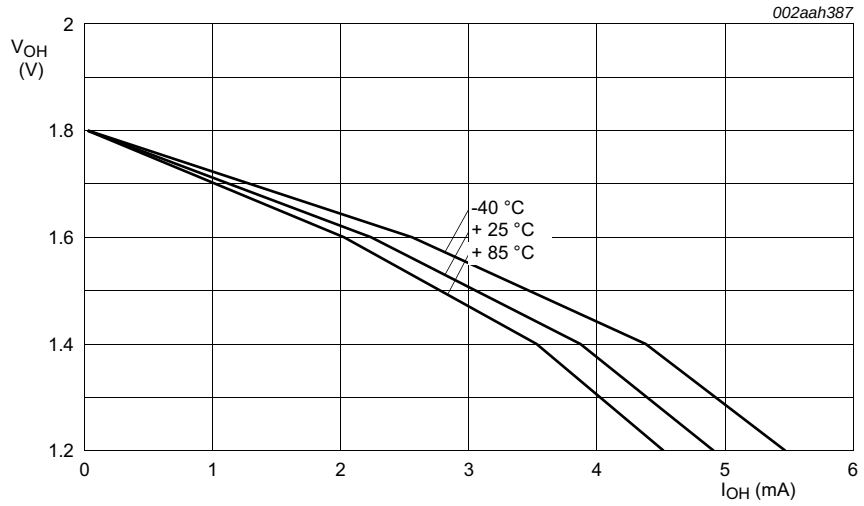
(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

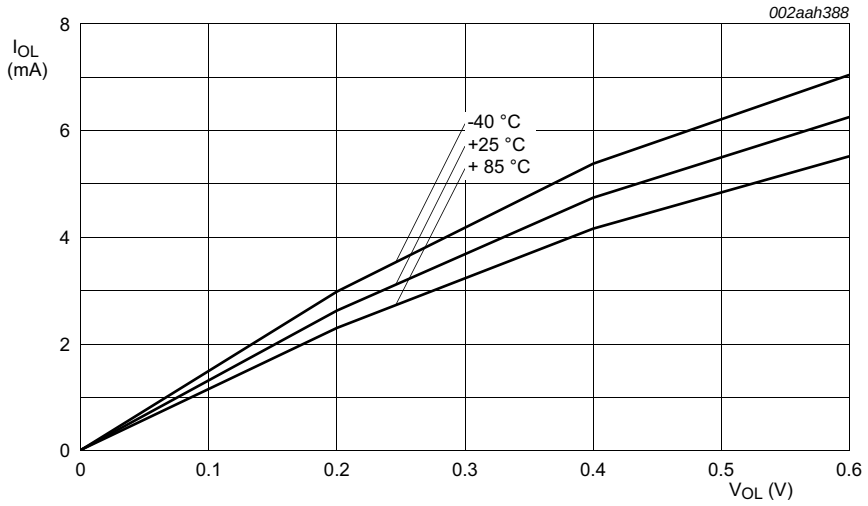
(5) Center of a step of the actual transfer curve.

Fig 7. ADC characteristics



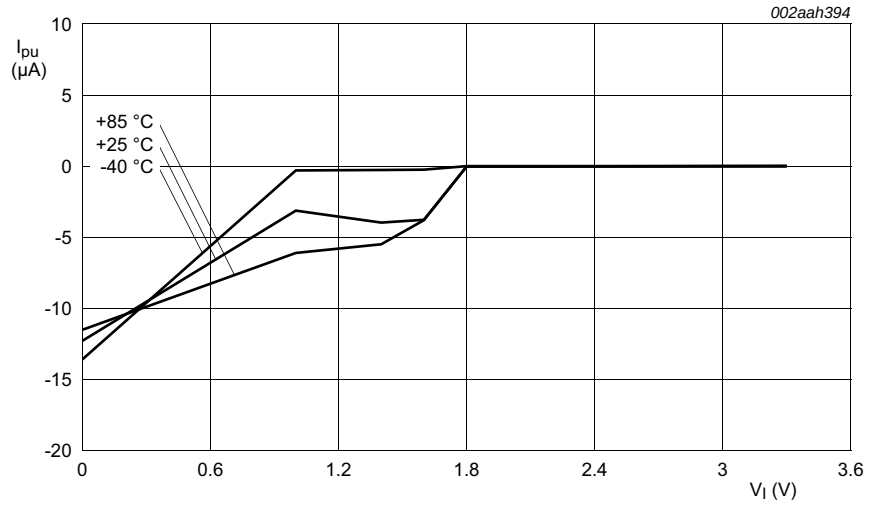
Conditions: standard port pins; V_{DD} = 1.8 V.

Fig 10. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



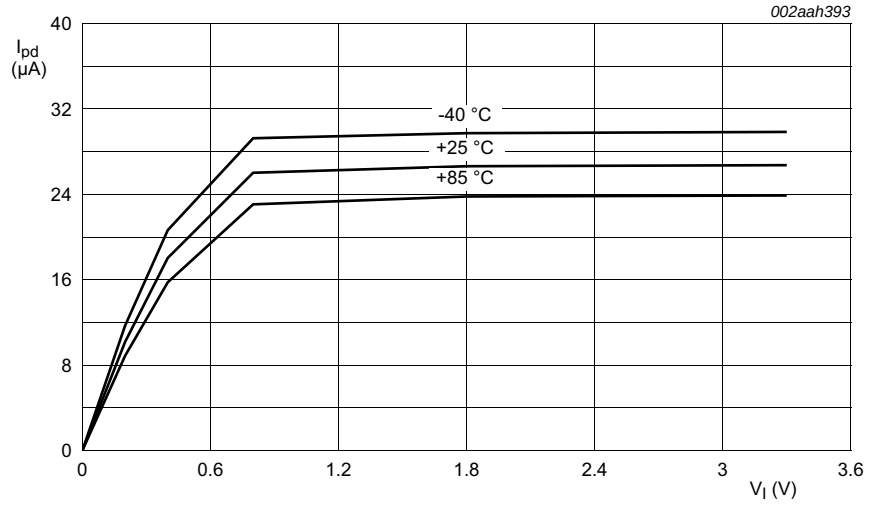
Conditions: standard port pins; V_{DD} = 1.8 V.

Fig 11. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



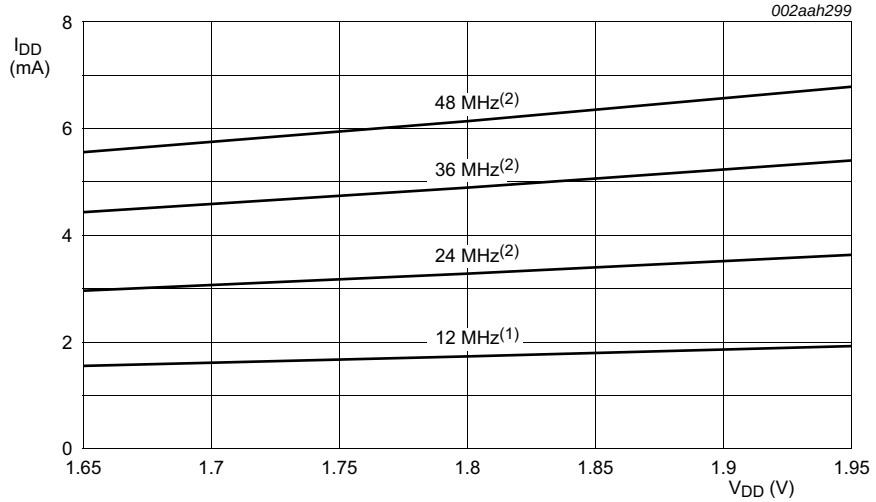
Conditions: standard port pins; V_{DD} = 1.8 V.

Fig 12. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: standard port pins; V_{DD} = 1.8 V.

Fig 13. Typical pull-down current I_{pd} versus input voltage V_I

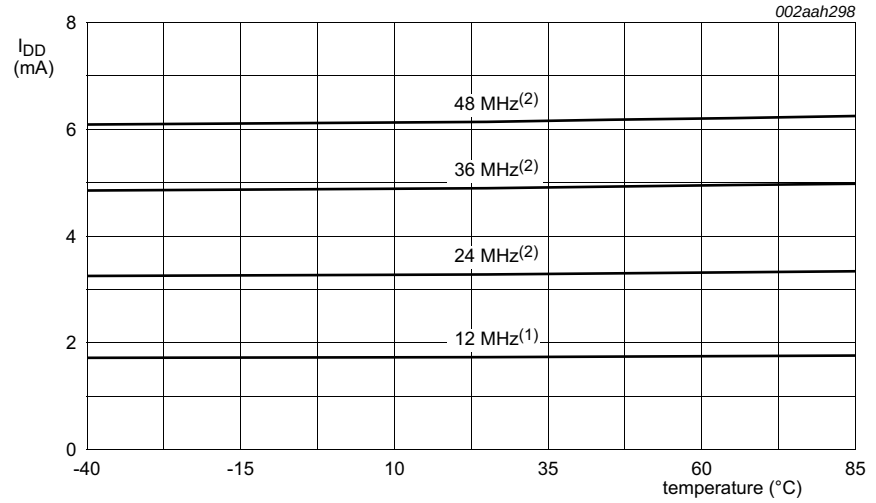


Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 16. Active mode: Typical supply current I_{DD} versus supply voltage for different system clock frequencies

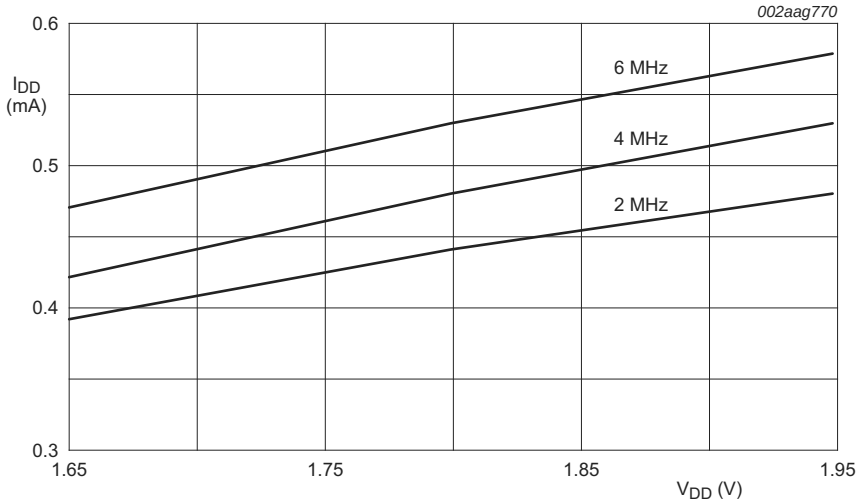


Conditions: V_{DD} = 1.8 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

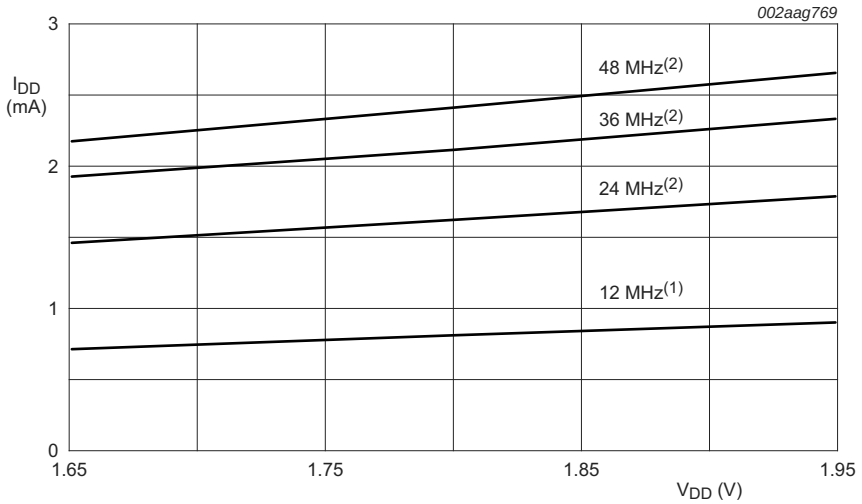
(2) System oscillator and system PLL enabled; IRC disabled.

Fig 17. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies



Conditions: T_{amb} = 25 °C; Sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; System oscillator and system PLL disabled; IRC disabled; system clock provided by external clock.

Fig 18. Sleep mode (2 MHz to 6 MHz): Typical supply current I_{DD} versus supply voltage V_{DD} for different clock frequencies



Conditions: T_{amb} = 25 °C; Sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 19. Sleep mode (12 MHz to 48 MHz): Typical supply current I_{DD} versus supply voltage V_{DD} for different clock frequencies

10. Dynamic characteristics

10.1 Flash memory

Table 9. Flash characteristics

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

10.2 External clock

Table 10. Dynamic characteristic: external clock

T_{amb} = –40 °C to +85 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

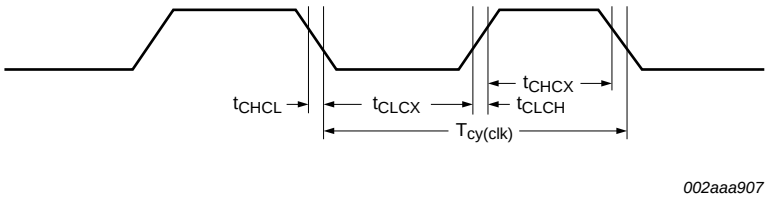


Fig 22. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

Table 13. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	$20 + 0.1 \times C_b$	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

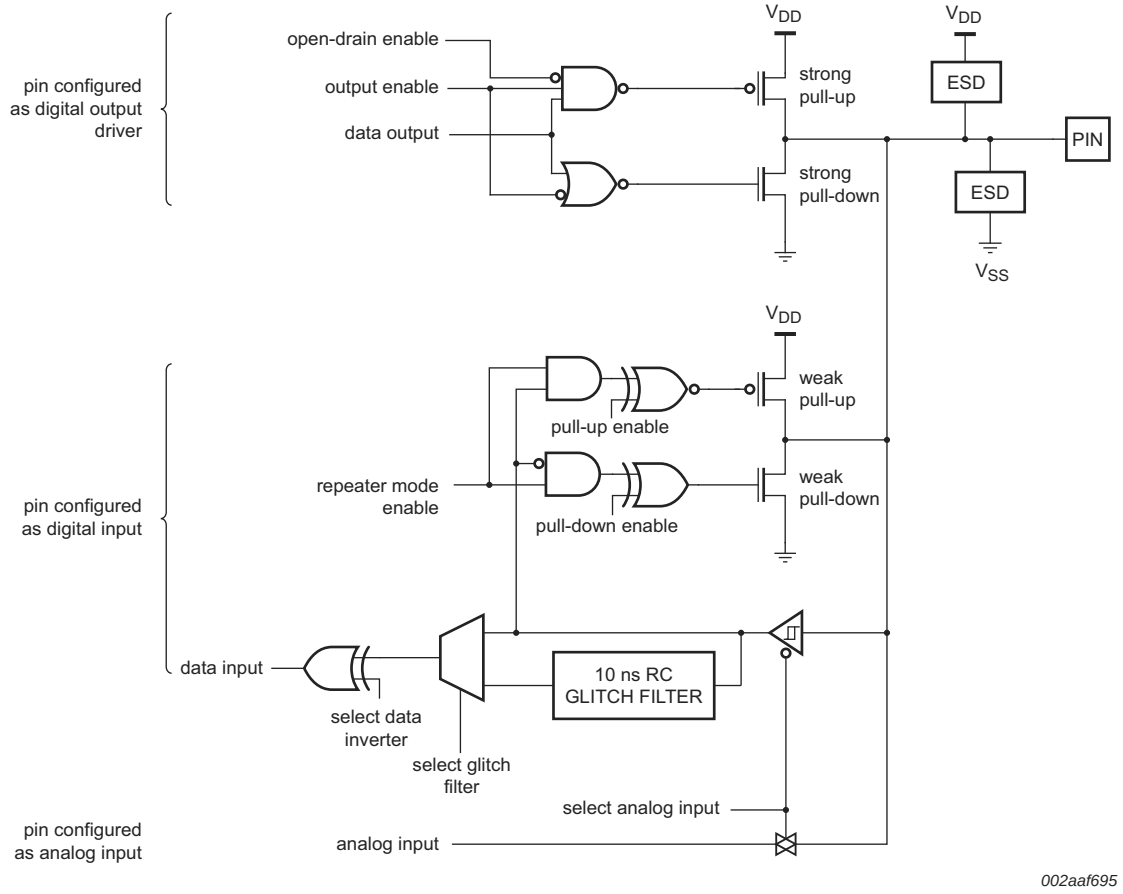


Fig 27. Standard I/O pad configuration

11.3 Reset pad configuration

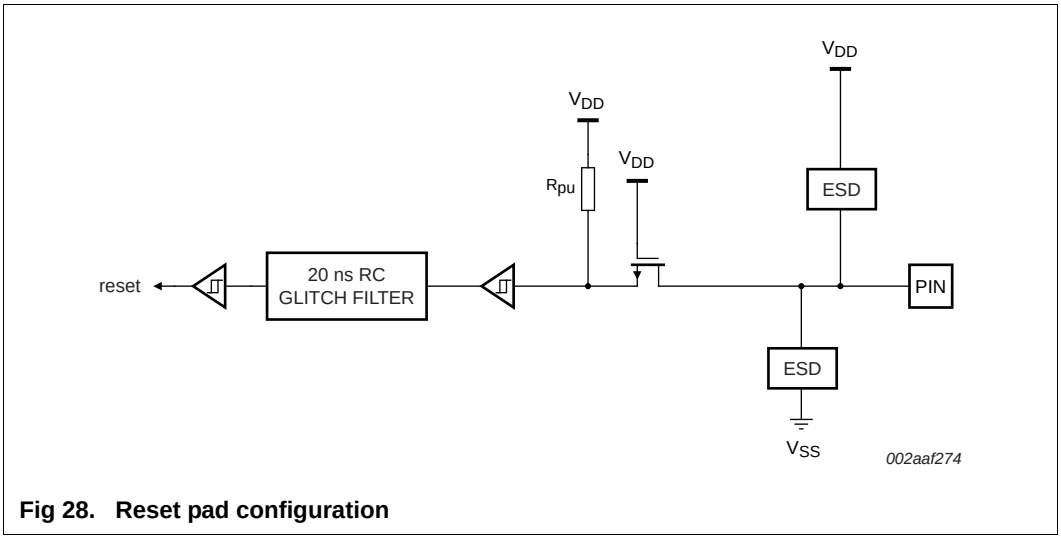
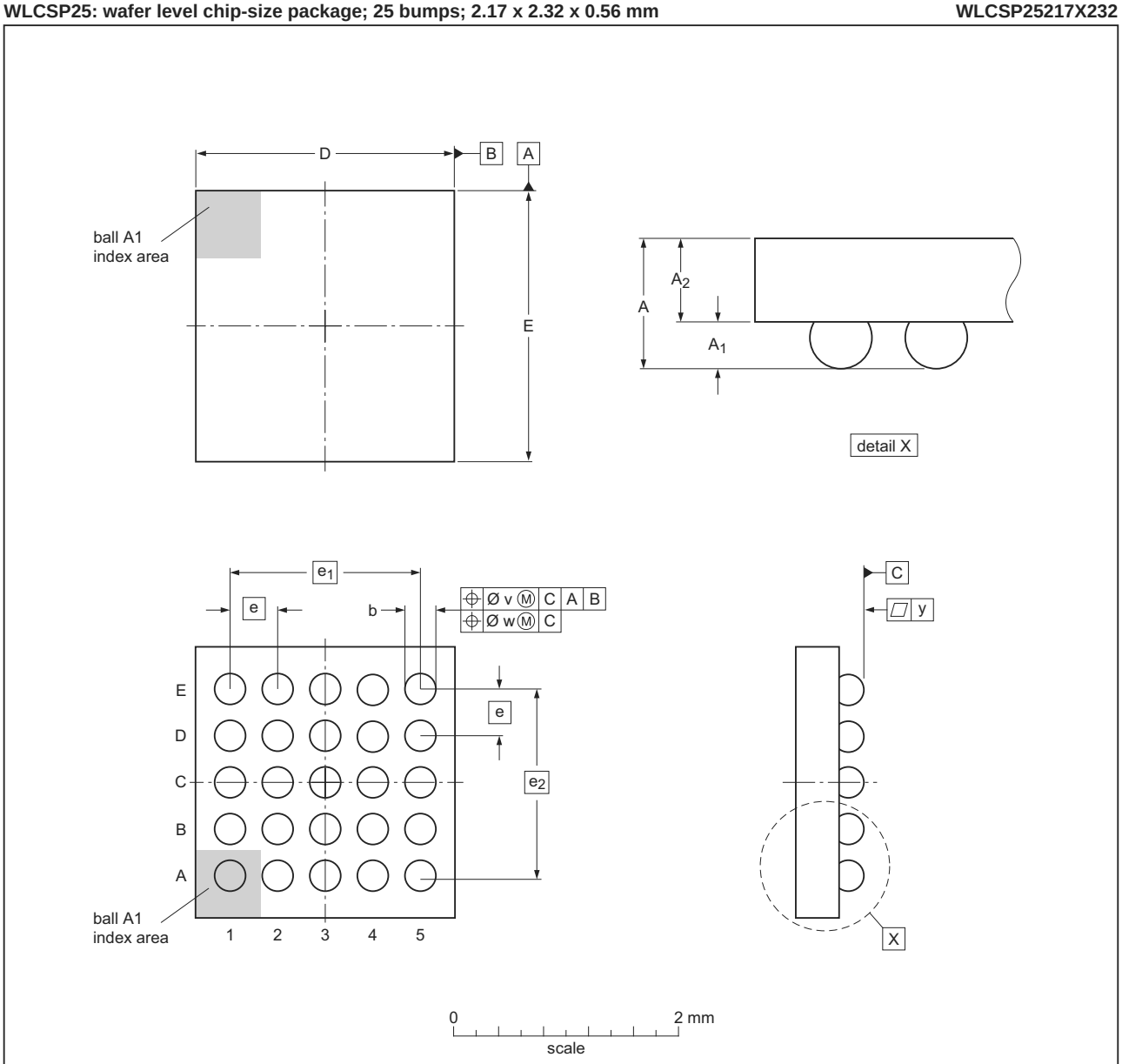


Fig 28. Reset pad configuration

12. Package outline

WLCSP25: wafer level chip-size package; 25 bumps; 2.17 x 2.32 x 0.56 mm **WLCSP25217X232**



Dimensions (mm are the original dimensions)

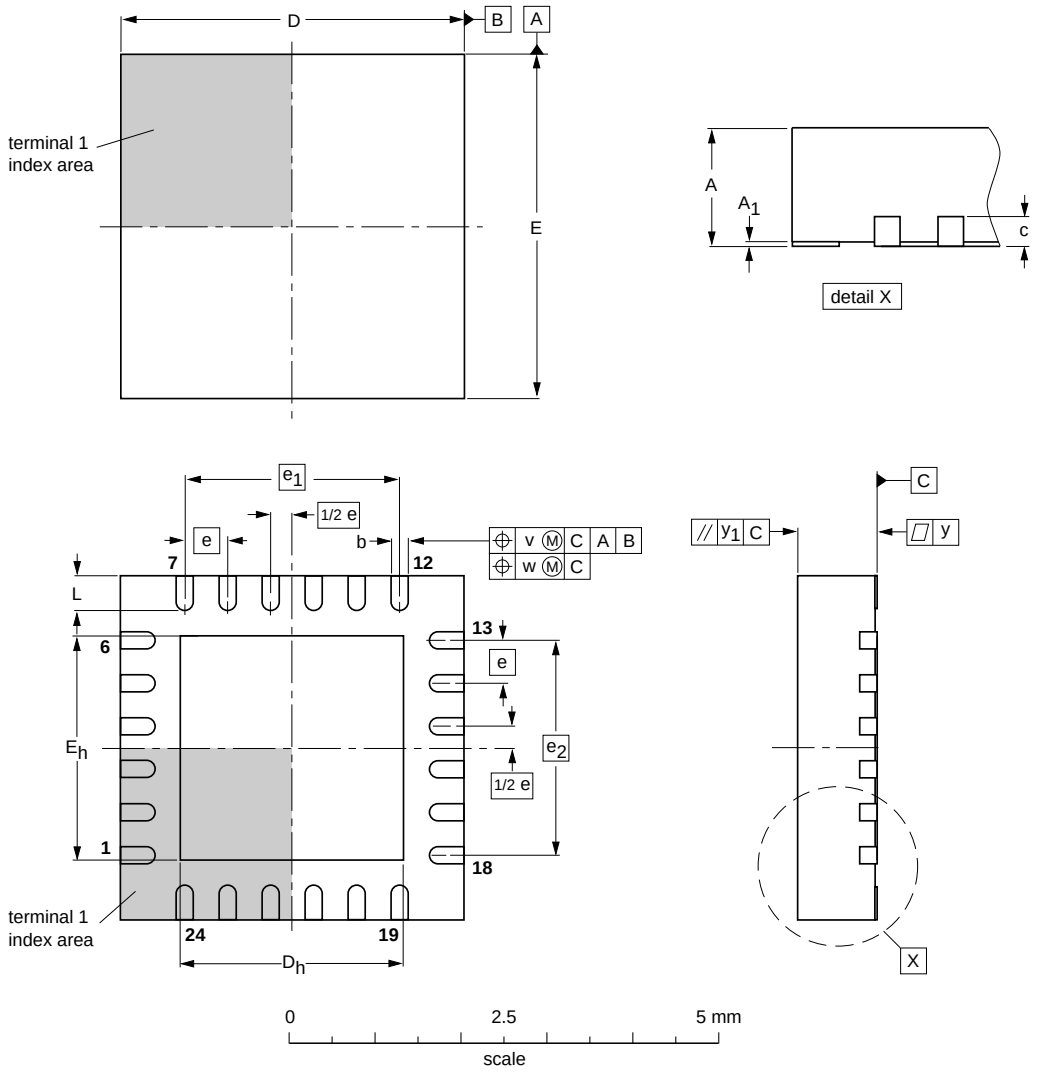
Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
	max	0.615	0.23	0.385	0.29	2.21	2.36						
mm	nom	0.560	0.20	0.360	0.26	2.17	2.32	0.4	1.6	1.6	0.15	0.05	0.05
	min	0.505	0.17	0.335	0.23	2.13	2.28						

wlcsp25_217x232_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
WLCSP25217X232						~~11-05-04~~ 12-02-13

Fig 29. Package outline (WLCSP25)

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-3**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.75 2.45	4.1 3.9	2.75 2.45	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

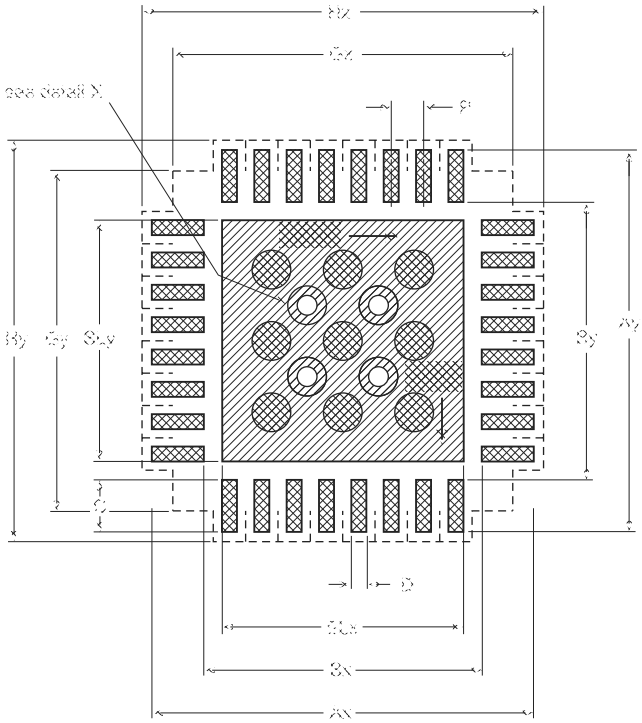
Note

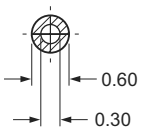
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-3	- - -	MO-220	- - -			~~04-11-19~~ 05-03-10

Fig 30. Package outline (HVQFN24)

Footprint information for reflow soldering of HVQFN33 package





detail X

solder land

solder paste

occupied area

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

002aag766

Fig 33. Reflow soldering for the HVQFN33 (5x5) package