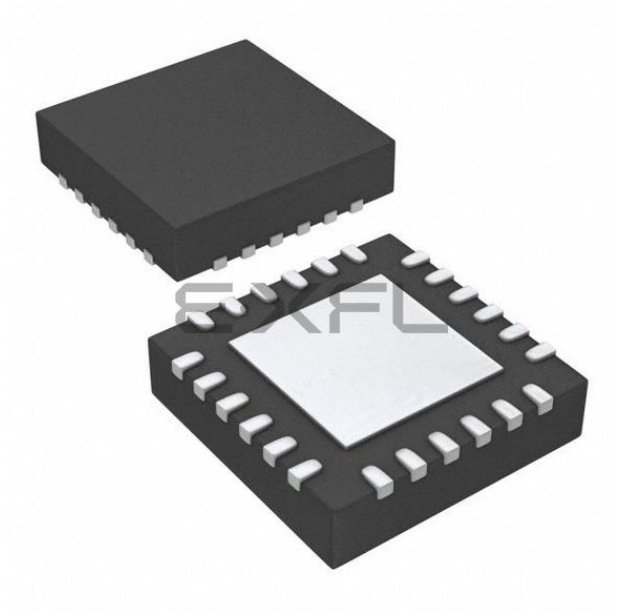


Welcome to E-XFL.COM

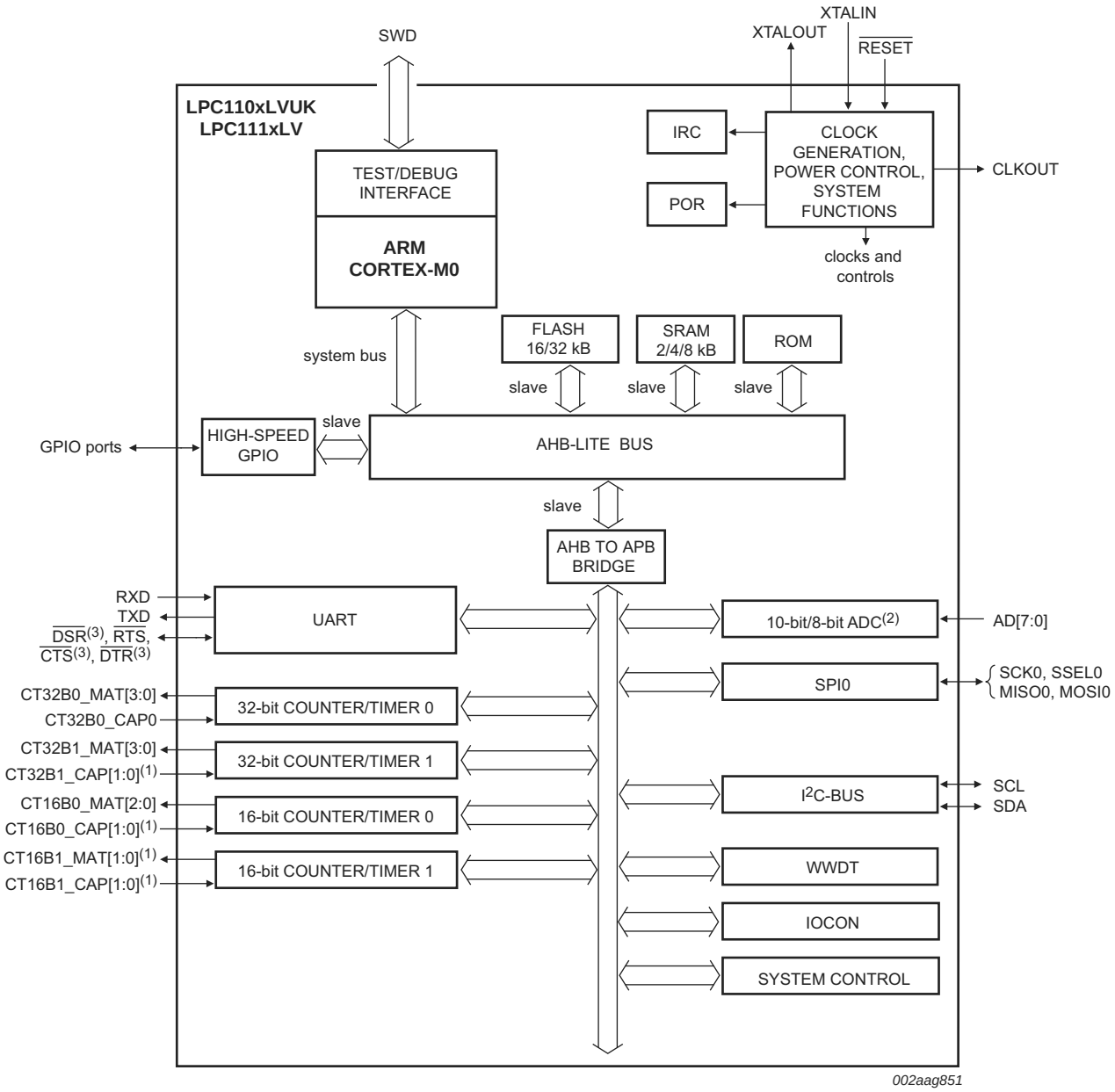
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	20
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 6x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-HVQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1112lvfhn24-003

5. Block diagram



(1) CT16B1_MAT1, CT32B1_CAP1, CT1B0_CAP1, CT16B1_CAP1 available on HVQFN33 only. CT16B1_MAT0 available on HVQFN33 and WLCSP25 packages only.

(2) 6 channels on WLCSP25 and HVQFN24 packages. 8 channels on HVQFN33 packages.

(3) $\overline{\text{DSR}}$ on WLCSP25 package only. $\overline{\text{DTR}}$ on HVQFN33 package only. $\overline{\text{CTS}}$ on HVQFN24 and HVQFN33 packages only.

Fig 1. LPC111xLV/LPC11xxLVUK block diagram

Table 3. LPC110xLVUK/LPC111xLV pin description table

Symbol	WLCSP25	HVQFN24	HVQFN33		Start logic input	Type	Reset state [1]	Description
PIO1_7/TXD/ CT32B0_MAT1	E1	1	32	[3]	no	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
						O	-	**TXD —** Transmitter output for UART.
						O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	B1	6	7	[3]	no	I/O	I; PU	**PIO1_8 —** General purpose digital input/output pin.
						I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0	B3	-	12	[3]	no	I/O	I; PU	**PIO1_9 —** General purpose digital input/output pin.
						O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	-	-	20	[5]	no	I/O	I;PU	**PIO1_10 —** General purpose digital input/output pin.
						I	-	**AD6 —** A/D converter, input 6.
						O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_11/AD7/ CT32B0_MAT3	-	-	27	[5]	no	I/O	I;PU	**PIO1_11 —** General purpose digital input/output pin.
						I	-	**AD7 —** A/D converter, input 7.
						O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
PIO2_0/$\overline{\text{DTR}}$	-	-	1	[3]	no	I/O	I;PU	**PIO2_0 —** General purpose digital input/output pin.
						O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
PIO2_1/$\overline{\text{DSR}}$	A1	-	-	[3]	no	I/O	I; PU	**PIO2_1 —** General purpose digital input/output pin.
						I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for UART.
PIO3_4/ CT16B0_CAP1/RXD	-	-	13	[3]	no	I/O	I;PU	**PIO3_4 —** General purpose digital input/output pin.
						I	-	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0.
						I	-	**RXD —** Receiver input for UART.
PIO3_5/ CT16B1_CAP1/TXD	-	-	14	[3]	no	I/O	I;PU	**PIO3_5 —** General purpose digital input/output pin.
						I	-	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
						O	-	**TXD —** Transmitter output for UART.
V_{DD}	E3	22	29; 6; 28		-	-	-	1.8 V supply voltage to the core, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	C1	4	4	[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	C2	5	5	[6]	-	O	-	Output from the oscillator amplifier.
V_{SS}	E4	21	33		-	-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level 0; IA = inactive, no pull-up/down enabled.

[2] See Figure 28 for the reset pad configuration.

[3] Pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 27).

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus.

[5] Pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as an ADC input, digital section of the pad is disabled (see Figure 27).

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.2 On-chip flash program memory

The LPC111xLV/LPC11xxLVUK contains up to 32 kB of on-chip flash memory.

The flash memory is divided into 4 kB sectors with each sector consisting of 16 pages. Individual pages of 256 byte each can be erased using the IAP erase page command.

7.3 On-chip SRAM

The LPC111xLV/LPC11xxLVUK contains up to 8 kB on-chip static RAM memory.

7.4 Memory map

The LPC111xLV/LPC11xxLVUK incorporates several distinct memory regions, shown in the following figures. Figure 5 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 megabyte in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kilobytes of space. This allows simplifying the address decoding for each peripheral.

capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.10.1 Features

- The I^2C-interface is a standard I^2C-bus compliant interface with open-drain pins. The I^2C-bus interface also supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- The I^2C-bus controller supports multiple address recognition and a bus monitor mode.

7.11 ADC

The LPC111xLV/LPC11xxLVUK contains one ADC. It is a single 8-bit successive approximation ADC with up to eight channels.

Remark: ADC specifications are valid for T_{amb} = -40 °C to +85 °C on HVQFN33 and WLCSP25 packages. ADC specifications are valid for T_{amb} = -10 °C to 85 °C on the HVQFN24 package.

7.11.1 Features

- 8-bit successive approximation ADC.
- Input multiplexing among 6 pins (WLCSP25 and HVQFN24 packages).
- Input multiplexing among 8 pins (HVQFN33 packages).
- Power-down mode.
- Measurement range 0 V to V_{DD}.
- 8-bit sampling rate of up to 10 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

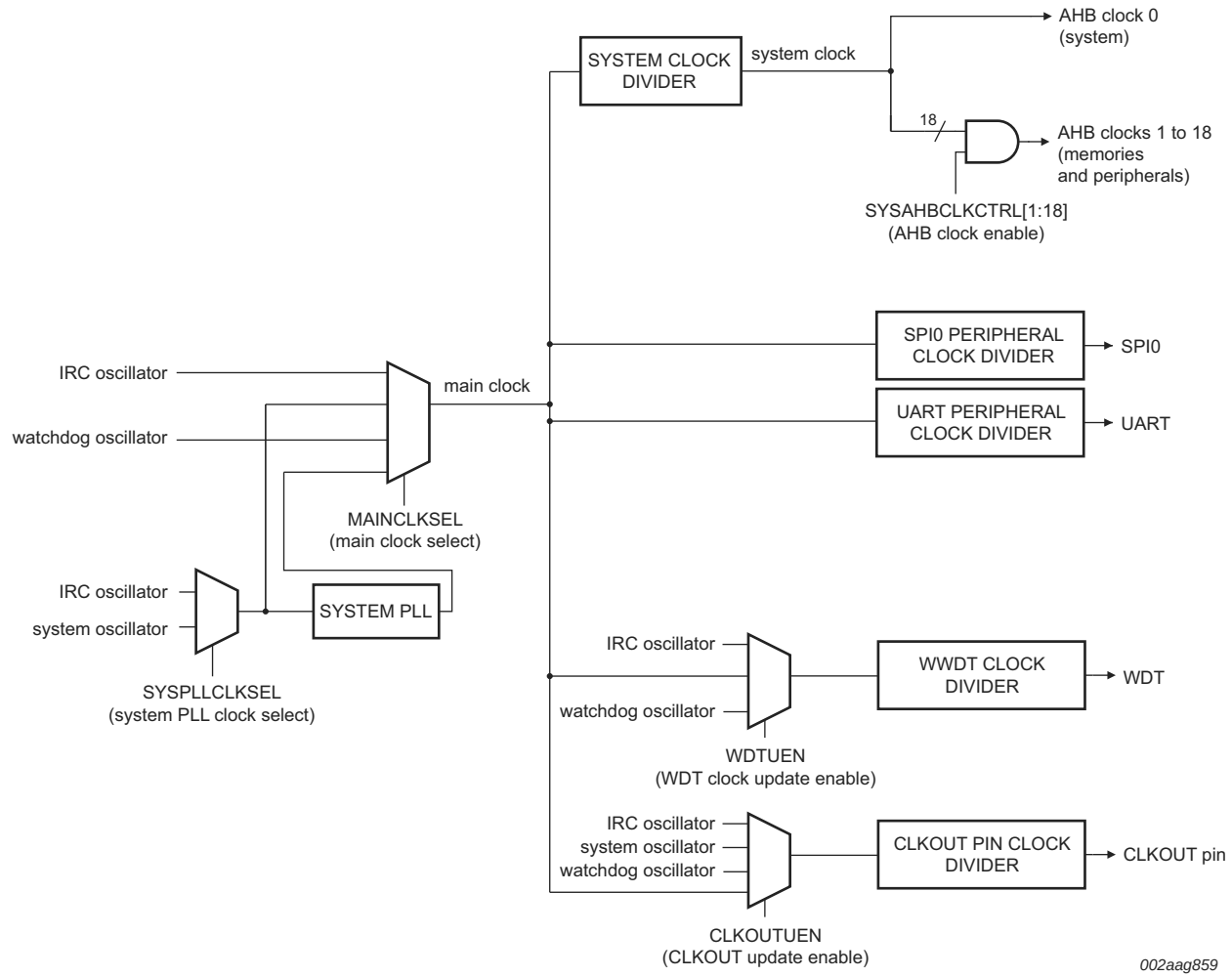


Fig 6. LPC111xLV/LPC11xxLVUK clock generation block diagram

7.15.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 2.5 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC111xLV/LPC11xxLVUK use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.15.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via the UART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled (NO_ISP mode). For details see the *LPC111xLV user manual*.

7.16.5 APB interface

The APB peripherals are located on one APB bus.

7.16.6 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

7.16.7 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs. In addition, start logic inputs serve as external interrupts (see Section 7.16.1).

7.17 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug with four breakpoints and two watchpoints is supported.

Table 5. Static characteristics (single power supply *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I²C-bus pins (PIO0_4 and PIO0_5)							
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD}$	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I²C-bus pins configured as standard mode pins 1.65 V ≤ V_{DD} ≤ 1.95 V		2.5	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I²C-bus pins configured as Fast-mode Plus pins 1.65 V ≤ V_{DD} ≤ 1.95 V;		15	-	-	mA
I_{LI}	input leakage current	$V_I = V_{DD}$	[11]	-	2	4	μA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled. BOD disabled for all measurements.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to UART and SPI0 disabled in system configuration block.

[6] IRC disabled; system oscillator enabled; system PLL enabled.

[7] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 18FF.

[8] Including voltage on outputs in 3-state mode.

[9] V_{DD} supply voltage must be present.

[10] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[11] To V_{SS}.

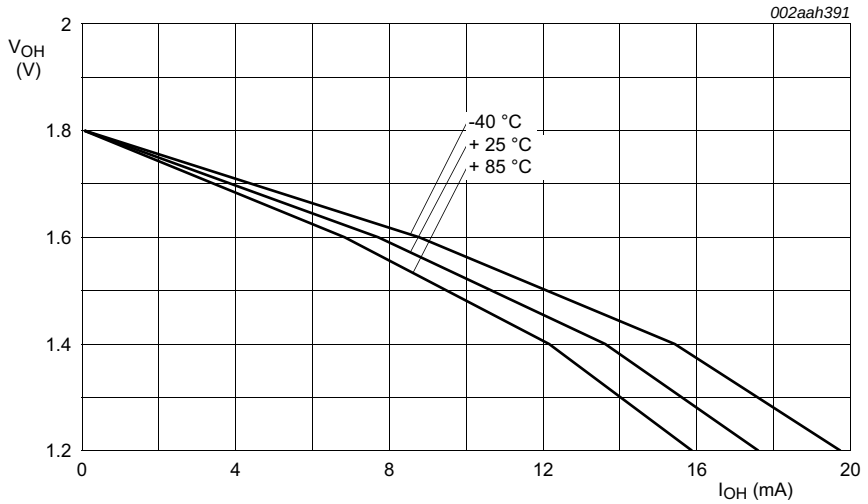
9.1.1 Analog characteristics

Remark: ADC specifications are valid for T_{amb} = -40 °C to +85 °C on HVQFN33 and WLCSP25 packages. ADC specifications are valid for T_{amb} = -10 °C to +85 °C on the HVQFN24 package.

Table 6. 8-bit ADC static characteristics
T_{amb} = −40 °C to +85 °C for HVQFN33 and WLCSP25 packages. T_{amb} = −10 °C to +85 °C for the HVQFN24 package. V_{DD} = 1.8 V ± 5 %; 8-bit resolution.

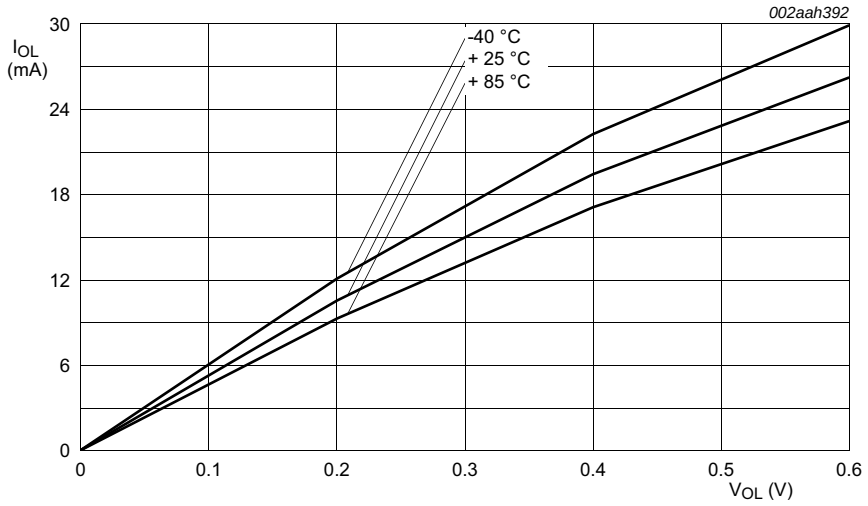
Symbol	Parameter		Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DD}	V
C_{ia}	analog input capacitance		-	-	1	pF
DNL	differential non-linearity	[1][2]	-	-	± 1	LSB
INL	integral non-linearity	[3]	-	-	± 1.5	LSB
E_O	offset error	[4]	-	-	± 1	LSB

9.2 Electrical pin characteristics



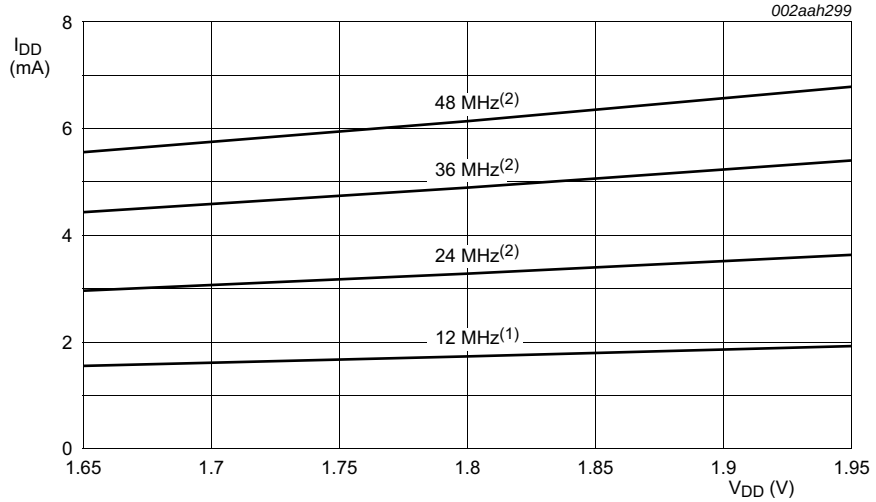
Conditions: high-drive pin PIO0_7; V_{DD} = 1.8 V.

Fig 8. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}.



Conditions: I^2C-bus pins PIO0_4 and PIO0_5; V_{DD} = 1.8 V; configured for Fast mode plus in the IOCON PIO0_4 and PIO0_5 registers.

Fig 9. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

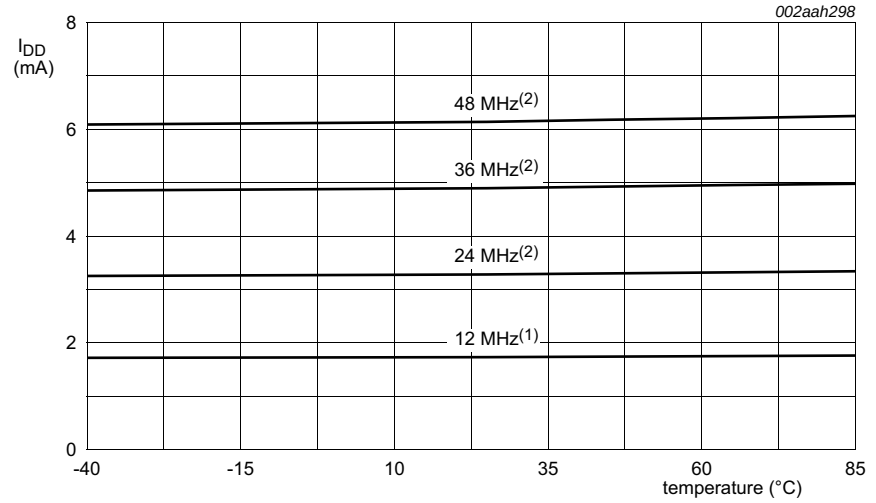


Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 16. Active mode: Typical supply current I_{DD} versus supply voltage for different system clock frequencies

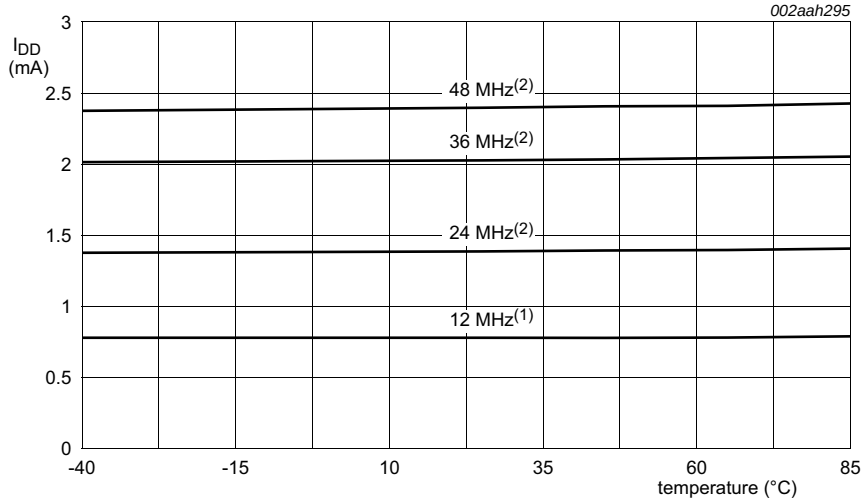


Conditions: V_{DD} = 1.8 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 17. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies

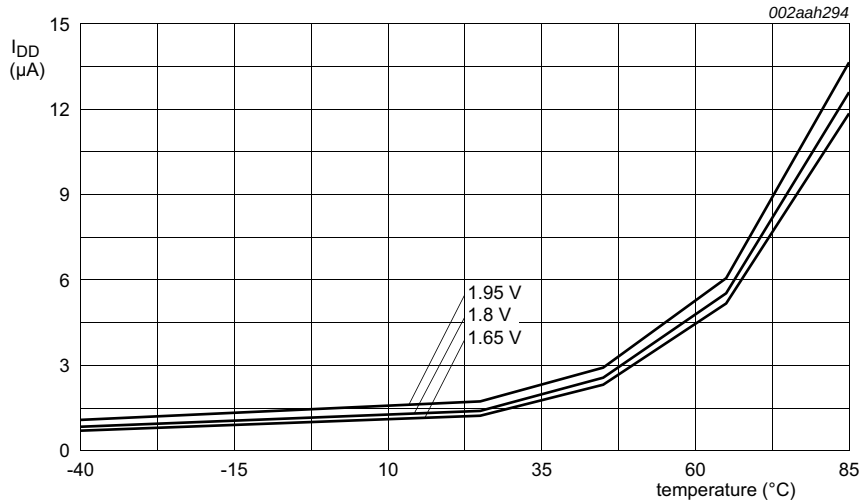


Conditions: T_{amb} = 25 °C; V_{DD} = 1.8 V; Sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 20. Sleep mode (12 MHz to 48 MHz): Typical supply current I_{DD} versus temperature for different clock frequencies



Conditions: all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 21. Deep-sleep mode: Typical supply current I_{DD} versus temperature

10.3 Internal oscillators

Table 11. Dynamic characteristic: internal oscillators
V_{DD} = 1.65V to 1.95 V.

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	*-20 °C ≤ T_{amb} ≤ +85 °C*	12 - 2.5 %	12	12 + 2.5 %	MHz
		-40 °C ≤ T_{amb} < -20 °C	12 - 5 %	12	12 + 5 %	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

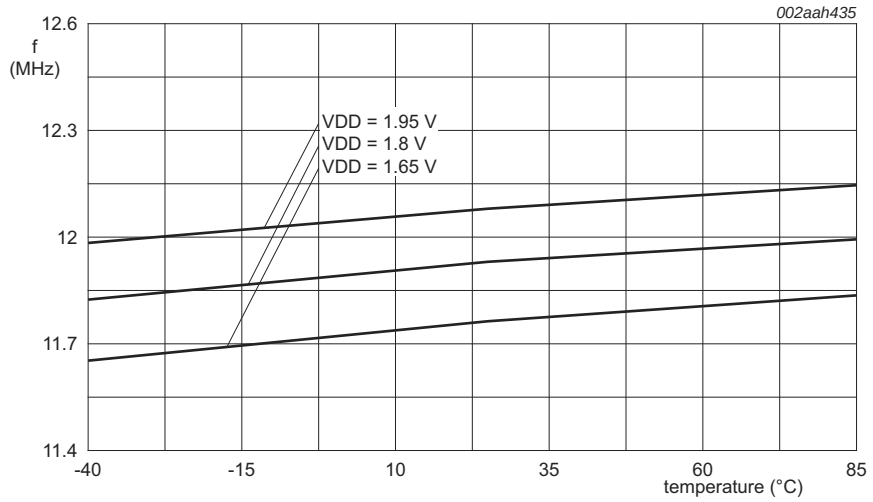


Fig 23. Typical internal RC oscillator frequency for different supply voltages V_{DD}

Table 12. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +85 °C) is ±40 %.

[3] See the *LPC111xLV user manual*.

10.4 I²C-bus

Table 13. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus	0	1	MHz

Table 13. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	$20 + 0.1 \times C_b$	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

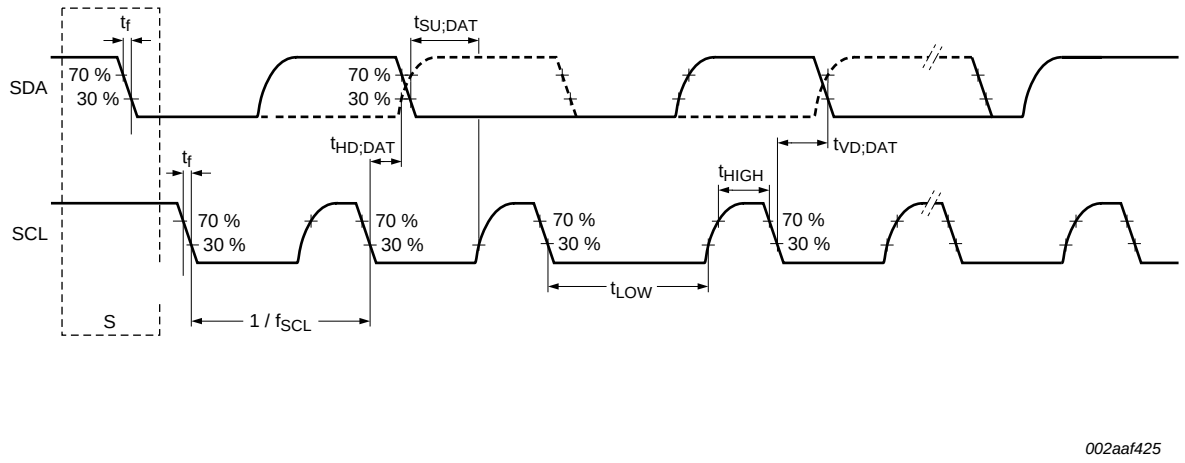


Fig 24. I²C-bus pins clock timing

10.5 SPI interface

Table 14. Dynamic characteristics of SPI pins in SPI mode

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master (in SPI mode)							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	50	-	-	ns
		when only transmitting	[1]	40	-	-	ns
t_{DS}	data set-up time	in SPI mode 1.8 V < V_{DD} < 1.95 V	[2]	24	-	-	ns
t_{DH}	data hold time	in SPI mode	[2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	0	-	-	ns

[1] $T_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / f_{main}. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] T_{amb} = −40 °C to 85 °C.

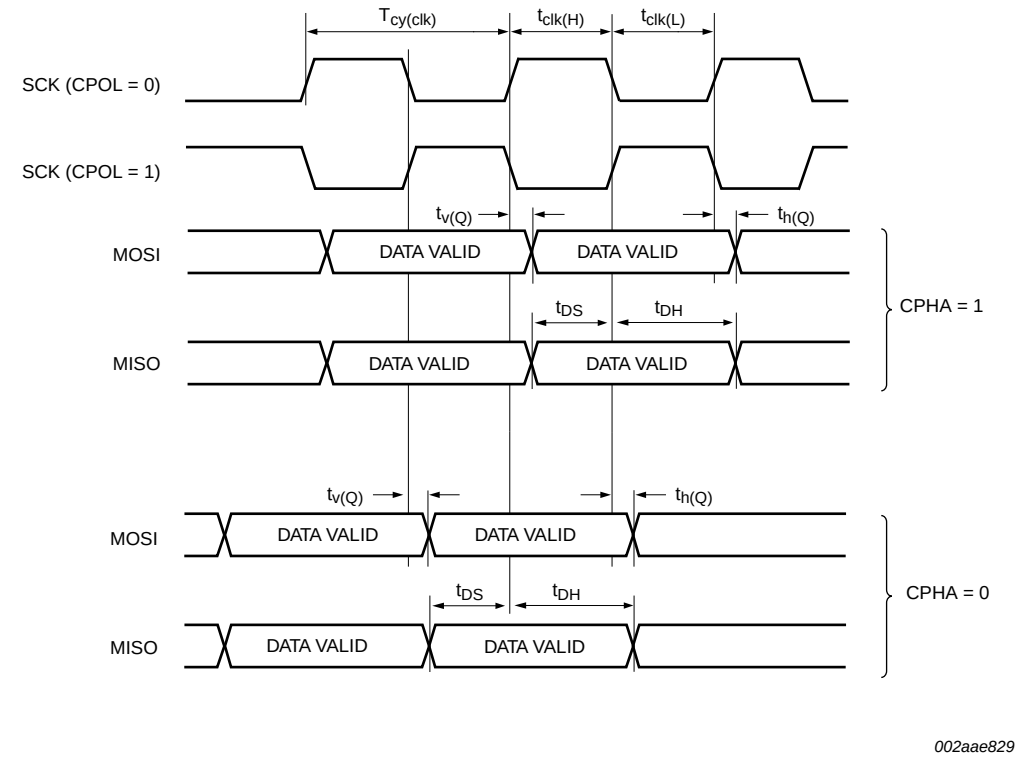


Fig 25. SPI master timing in SPI mode

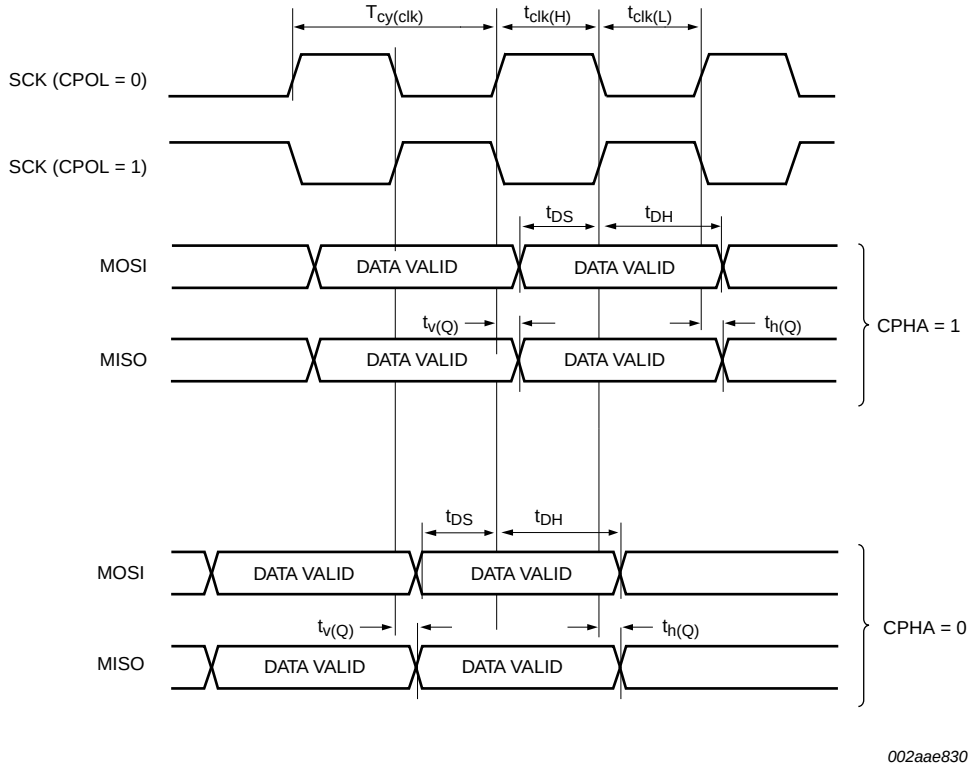


Fig 26. SPI slave timing in SPI mode

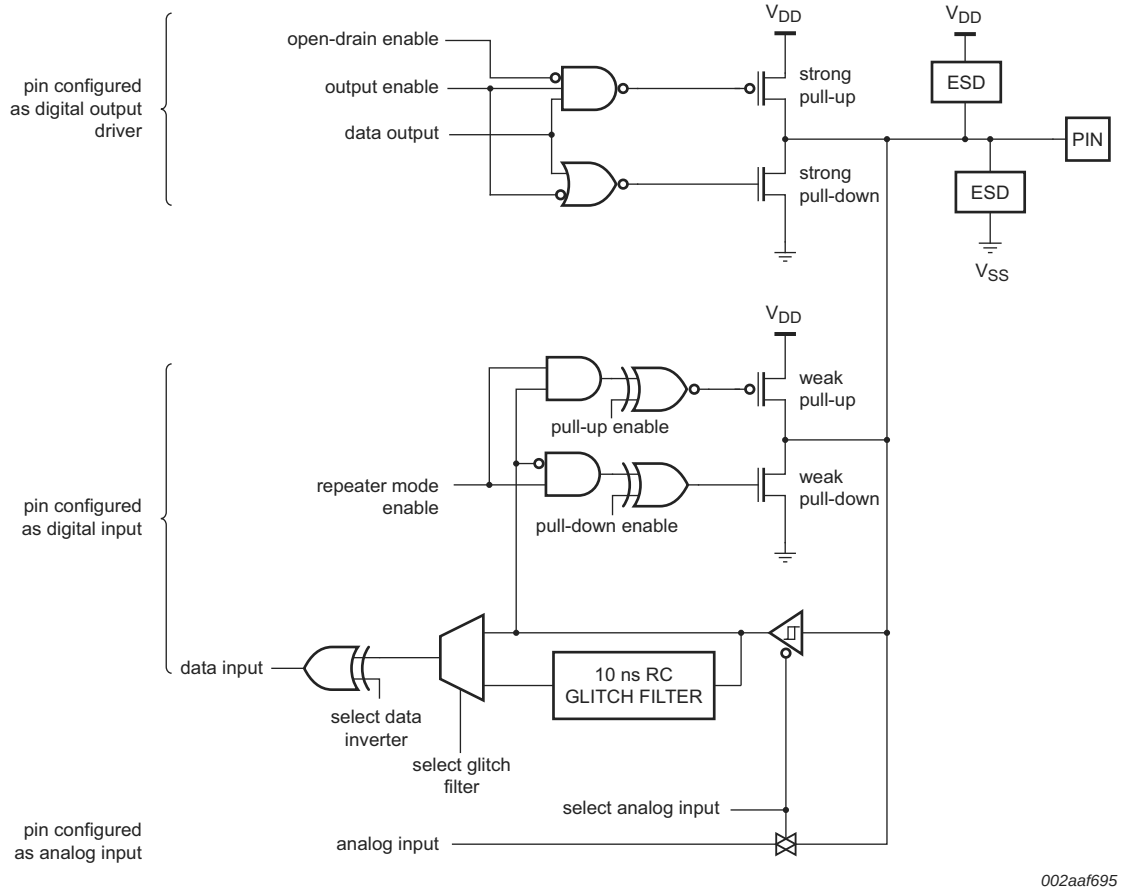


Fig 27. Standard I/O pad configuration

11.3 Reset pad configuration

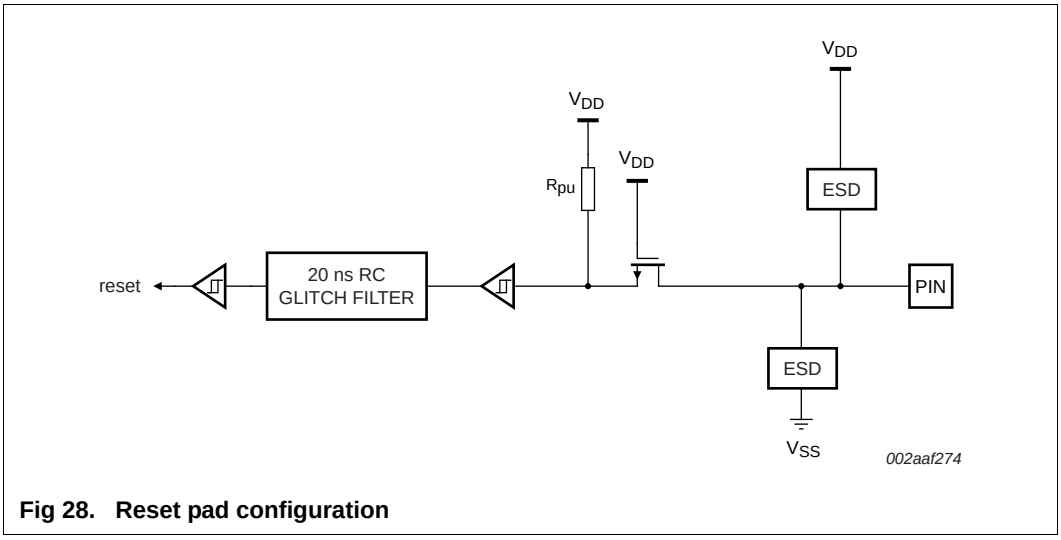
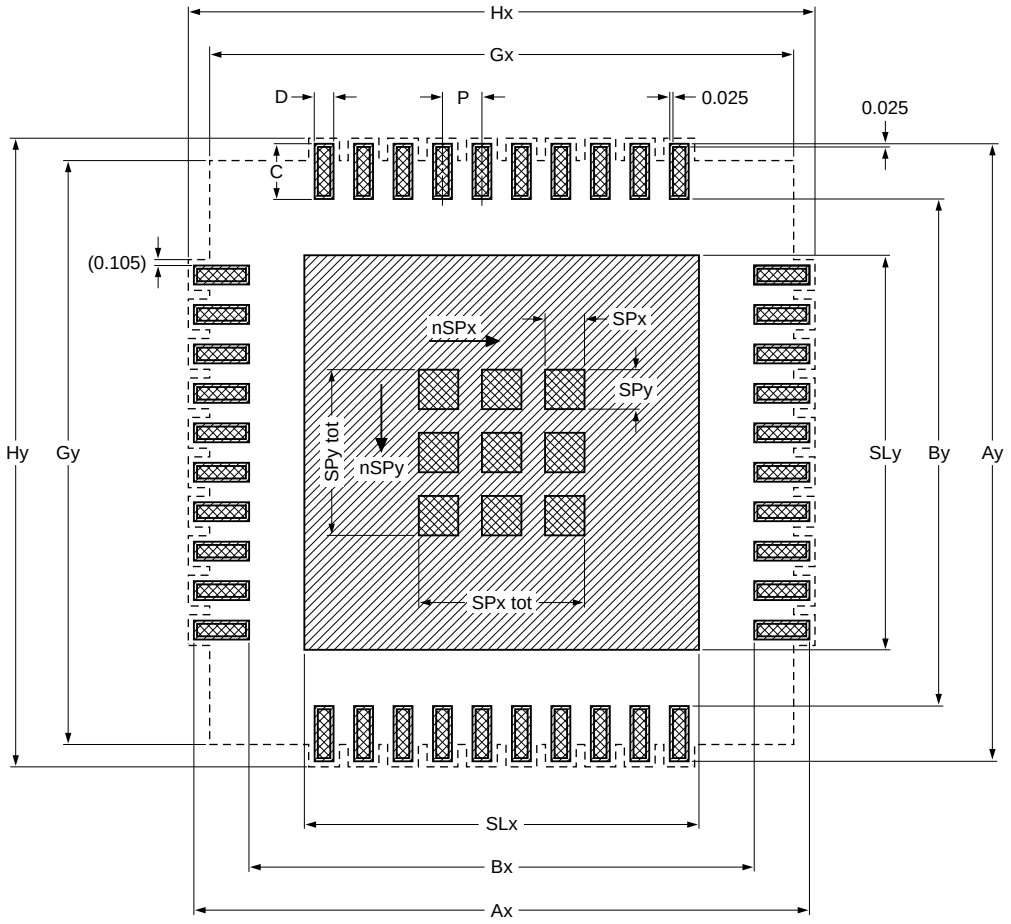


Fig 28. Reset pad configuration

13. Soldering

Footprint information for reflow soldering of HVQFN24 package **SOT616-3**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

nSPx	nSPy
2	2

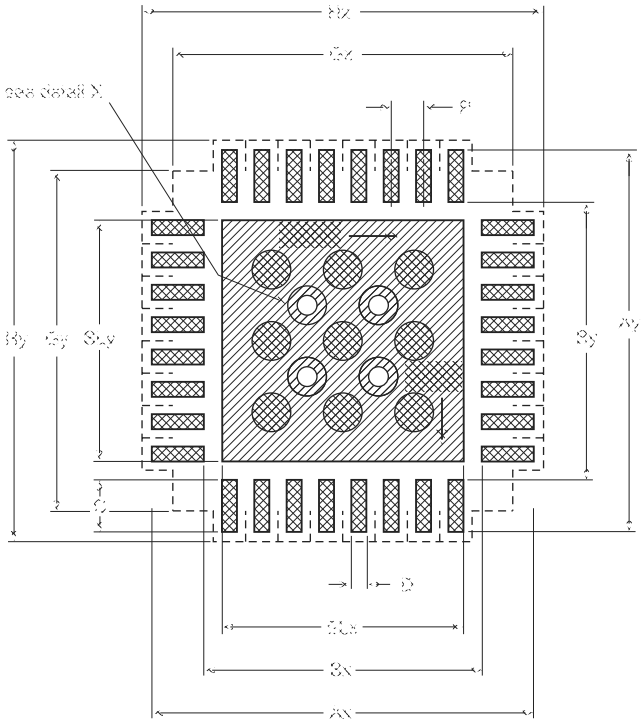
Dimensions in mm

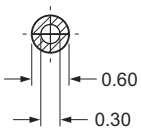
P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.500	5.000	5.000	3.200	3.200	0.900	0.240	2.500	2.500	1.500	1.500	0.550	0.550	4.300	4.300	5.250	5.250

Issue date ~~07-05-07~~ 09-06-15 *sot616-3_fr*

Fig 32. Reflow soldering for the HVQFN24 package

Footprint information for reflow soldering of HVQFN33 package





detail X

solder land

solder paste

occupied area

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

002aag766

Fig 33. Reflow soldering for the HVQFN33 (5x5) package

15. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC111XLV_LPC11XXLVUK v.2	20121010	Product data sheet	-	LPC111XLV_LPC11XXLVUK v.1
Modifications:	• Functions CT16B0_CAP1/RXD added to pin PIO3_4. • Functions CT16B1_CAP1/TXD added to pin PIO3_5. • Function CT32B1_CAP1 added to pin PIO1_11. • Capture/clear functionality added to counter/timers. See Section 7.12. • Figure 21 “Deep-sleep mode: Typical supply current I_{DD} versus temperature” updated. • Electrical pin characteristics data combined in Section 9.2 for dual and single power supplies. • SSP timing characteristics in slave mode removed for single power supply parts in Table 14. • Table 11 “Dynamic characteristic: internal oscillators” and Figure 23 updated. • Figure 33 corrected. • Removed dual-power supply option. All parts use a single 1.8 V +/- 10 % power supply. • Removed 10-bit ADC. Only the 8-bit ADC is available. • Temperature range for ADC characteristics on the HVQFN24 package restricted to T_{amb} = -10 °C to +85 °C. • BOD interrupt level 0 removed in Table 8. • IRC accuracy updated to 2.5 % accuracy for T_{amb} = -20 °C to +85 °C and to 5 % accuracy for T_{amb} = -40 °C to -20 °C. • Data sheet status changed to Product data sheet.			
LPC111XLV_LPC11XXLVUK v.1	20120621	Objective data sheet	-	-

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

17.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I^2C-bus — logo is a trademark of NXP B.V.

18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**