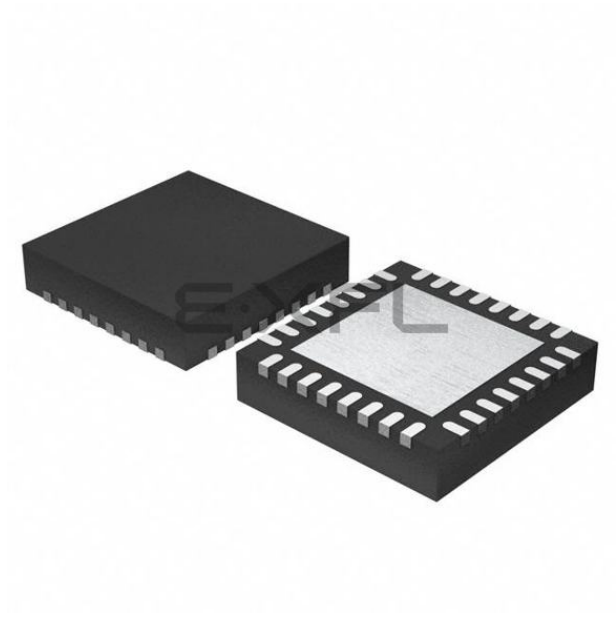

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 27 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 1.95V |
| Data Converters | A/D 8x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-VFQFN Exposed Pad |
| Supplier Device Package | 32-HVQFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1114lvfhi33-303 |

**Table 1. Ordering information** *…continued*

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| LPC1114LVFHN24/303 | HVQFN24 | plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm | SOT616-3 |
| LPC1112LVFHI33/103 | HVQFN33 | plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm | n/a |
| LPC1114LVFHI33/303 | HVQFN33 | plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm | n/a |

## 4.1 Ordering options

**Table 2. Ordering options**

| Type number | Flash in kB | Total SRAM in kB | SPI/ SSP | I2C | UART | ADC | GPIO pins | Package |
|---|---|---|---|---|---|---|---|---|
| LPC1101LVUK | 32 | 2 | 1 | 1 | 1 | 6-channel | 21 | WLCSP25 |
| LPC1102LVUK | 32 | 8 | 1 | 1 | 1 | 6-channel | 21 | WLCSP25 |
| LPC1112LVFHN24/003 | 16 | 2 | 1 | 1 | 1 | 6-channel | 20 | HVQFN24 |
| LPC1114LVFHN24/103 | 32 | 4 | 1 | 1 | 1 | 6-channel | 20 | HVQFN24 |
| LPC1114LVFHN24/303 | 32 | 8 | 1 | 1 | 1 | 6-channel | 20 | HVQFN24 |
| LPC1112LVFHI33/103 | 16 | 4 | 1 | 1 | 1 | 8-channel | 27 | HVQFN33 |
| LPC1114LVFHI33/303 | 32 | 8 | 1 | 1 | 1 | 8-channel | 27 | HVQFN33 |

- In the LPC111xLV/LPC11xxLVUK, the NVIC supports 32 vectored interrupts including up to 13 inputs to the start logic from individual GPIO pins.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.

### 7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any GPIO pin (total of up to 18 pins) regardless of the selected function, can be programmed to generate an interrupt on a level, or rising edge or falling edge, or both.

## 7.6 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

## 7.7 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC111xLV/LPC11xxLVUK use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Additionally, any GPIO pin (total of up to 18 pins) providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

### 7.7.1 Features

- Bit level port registers allow a single instruction to set or clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with pull-ups enabled after reset with the exception of the $I^2C$-bus pins PIO0_4 and PIO0_5.
- Pull-up/pull-down resistor configuration can be programmed through the IOCON block for each GPIO pin (except for pins PIO0_4 and PIO0_5).
- All GPIO pins (except PIO0_4 and PIO0_5) are pulled up to 1.8 V ($V_{DD}$ = 1.8 V) if their pull-up resistor is enabled in the IOCON block (single power supply).
- Programmable open-drain mode.

## 7.8 UART

The LPC111xLV/LPC11xxLVUK contains one UART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The UART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

### 7.8.1 Features

- Maximum UART data bit rate of 3.125 MBit/s.
- 16 Byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.

## 7.9 SPI serial I/O controller

The LPC111xLV/LPC11xxLVUK contains one SPI controller.

The SPI controller is capable of operation on an SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SPI supports full-duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

### 7.9.1 Features

- Maximum SPI speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

## 7.10 $I^2C$-bus serial I/O controller

The LPC111xLV/LPC11xxLVUK contains one $I^2C$-bus controller.

The $I^2C$-bus is bidirectional for inter-IC control using only two wires: a Serial Clock Line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the

capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The $I^2C$ is a multi-master bus and can be controlled by more than one bus master connected to it.

### 7.10.1 Features

- The $I^2C$-interface is a standard $I^2C$-bus compliant interface with open-drain pins. The $I^2C$-bus interface also supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The $I^2C$-bus can be used for test and diagnostic purposes.
- The $I^2C$-bus controller supports multiple address recognition and a bus monitor mode.

## 7.11 ADC

The LPC111xLV/LPC11xxLVUK contains one ADC. It is a single 8-bit successive approximation ADC with up to eight channels.

**Remark:** ADC specifications are valid for $T_{amb}$ = -40 °C to +85 °C on HVQFN33 and WLCSP25 packages. ADC specifications are valid for $T_{amb}$ = -10 °C to 85 °C on the HVQFN24 package.

### 7.11.1 Features

- 8-bit successive approximation ADC.
- Input multiplexing among 6 pins (WLCSP25 and HVQFN24 packages).
- Input multiplexing among 8 pins (HVQFN33 packages).
- Power-down mode.
- Measurement range 0 V to $V_{DD}$.
- 8-bit sampling rate of up to 10 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

**Table 6. 8-bit ADC static characteristics** *…continued*

*$T_{amb}$ = −40 °C to +85 °C for HVQFN33 and WLCSP25 packages. $T_{amb}$ = −10 °C to +85 °C for the HVQFN24 package. $V_{DD}$ = 1.8 V ± 5 %; 8-bit resolution.*

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $E_G$ | gain error | [5] | - | - | ± 2 | LSB |
| $f_{clk(ADC)}$ | ADC clock frequency | | - | - | 110 | kHz |
| $f_s$ | sampling rate | | - | - | 10 | kSamples/s |
| $R_{vsi}$ | voltage source interface resistance | | - | - | 40 | kΩ |
| $R_i$ | input resistance | [6][7] | - | - | 2.5 | MΩ |

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error ($E_D$) is the difference between the actual step width and the ideal step width. See Figure 7.

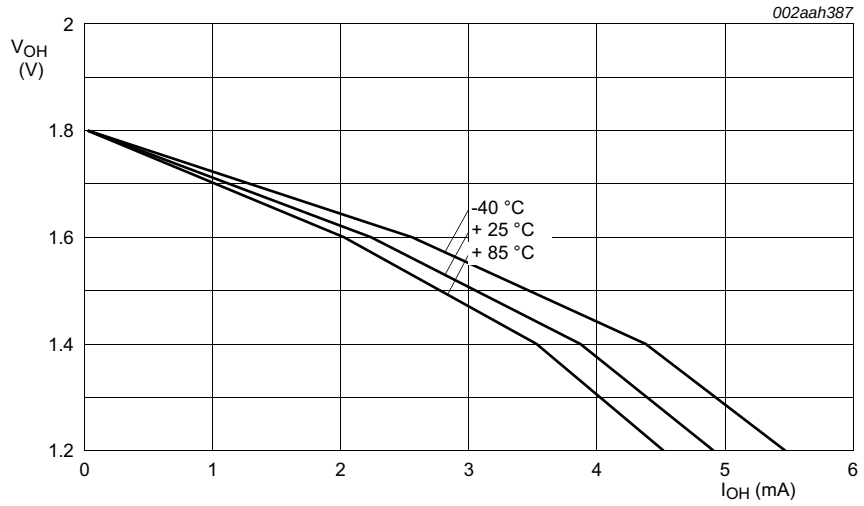
[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 7.

[4] The offset error ($E_O$) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 7.

[5] The gain error ($E_G$) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 7.

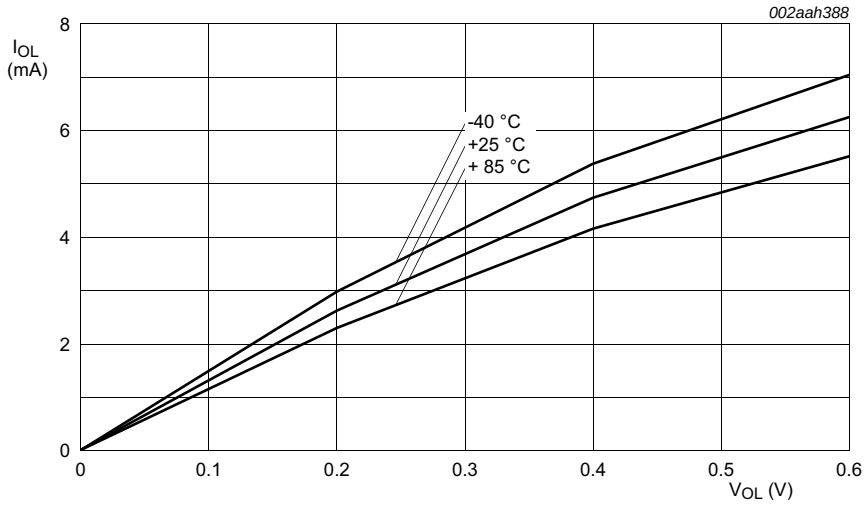
[6] $T_{amb}$ = 25 °C; maximum sampling frequency $f_s$ = 10 kSamples/s and analog input capacitance $C_{ia}$ = 1 pF.

[7] Input resistance $R_i$ depends on the sampling frequency fs: $R_i = 1 / (f_s \times C_{ia})$.




Conditions: standard port pins; $V_{DD}$ = 1.8 V.

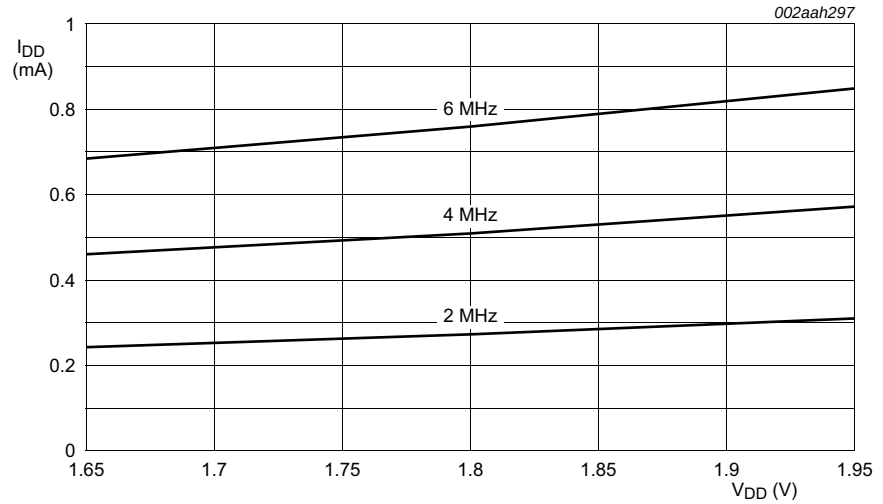
**Fig 10. Typical HIGH-level output voltage $V_{OH}$ versus HIGH-level output source current $I_{OH}$**




Conditions: standard port pins; $V_{DD}$ = 1.8 V.

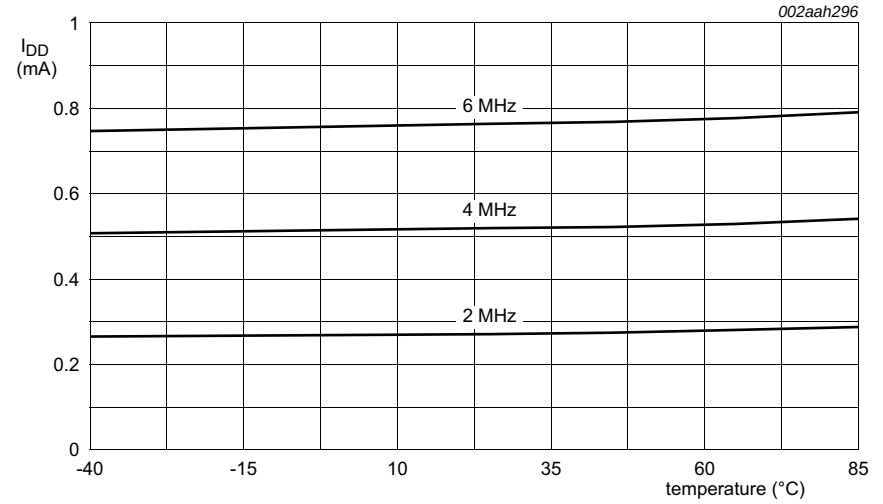
**Fig 11. Typical LOW-level output current $I_{OL}$ versus LOW-level output voltage $V_{OL}$**

## 9.3 Power consumption



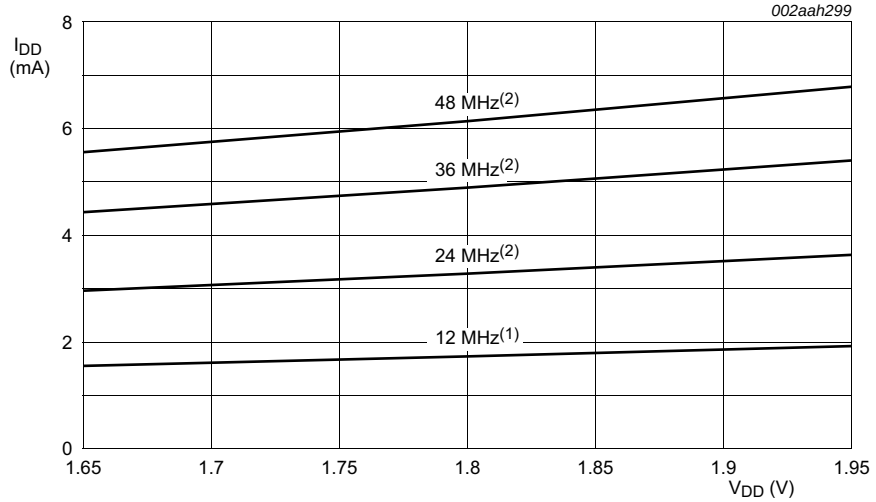

Conditions: $T_{amb}$ = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; System oscillator, system PLL, IRC, BOD disabled; system clock provided by external clock.

**Fig 14. Active mode (2 MHz to 6 MHz): Typical supply current $I_{DD}$ versus supply voltage $V_{DD}$ for different clock frequencies**




Conditions: $V_{DD}$ = 1.8 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; System oscillator, system PLL, IRC, BOD disabled; system clock provided by external clock.

**Fig 15. Active mode (2 MHz to 6 MHz): Typical supply current $I_{DD}$ versus temperature for different clock frequencies**

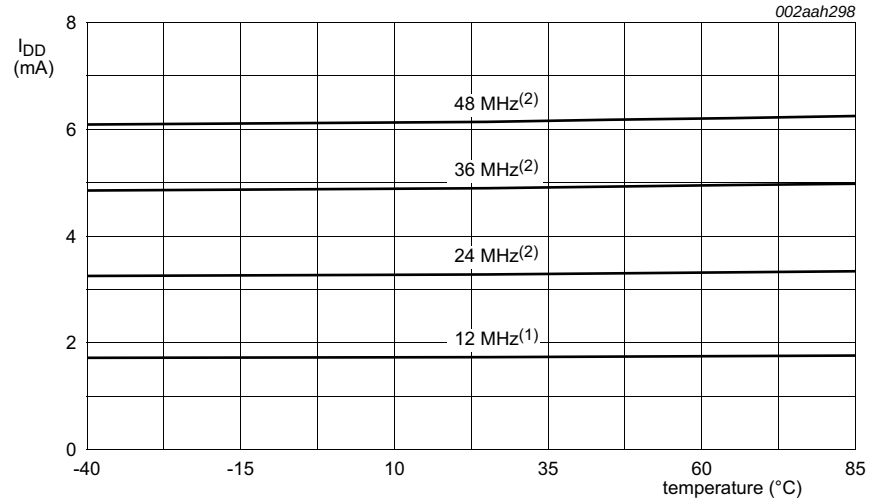



Conditions: $T_{amb}$ = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

**Fig 16. Active mode: Typical supply current $I_{DD}$ versus supply voltage for different system clock frequencies**

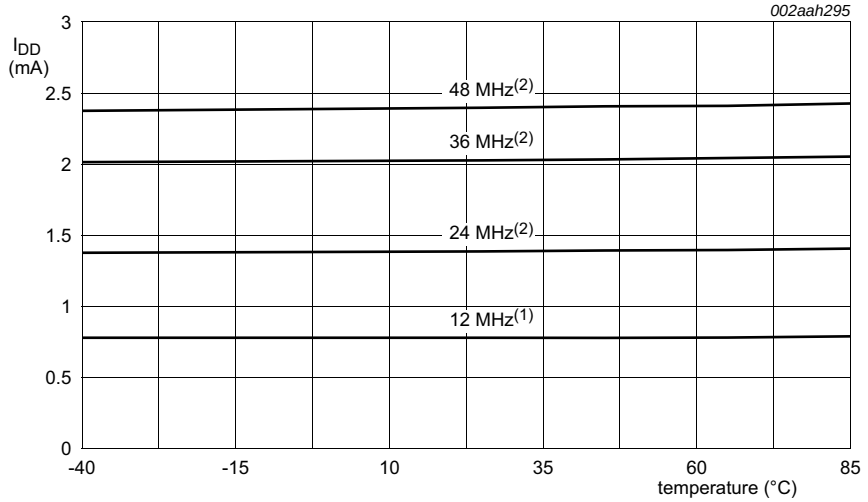



Conditions: $V_{DD}$ = 1.8 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

**Fig 17. Active mode: Typical supply current $I_{DD}$ versus temperature for different system clock frequencies**

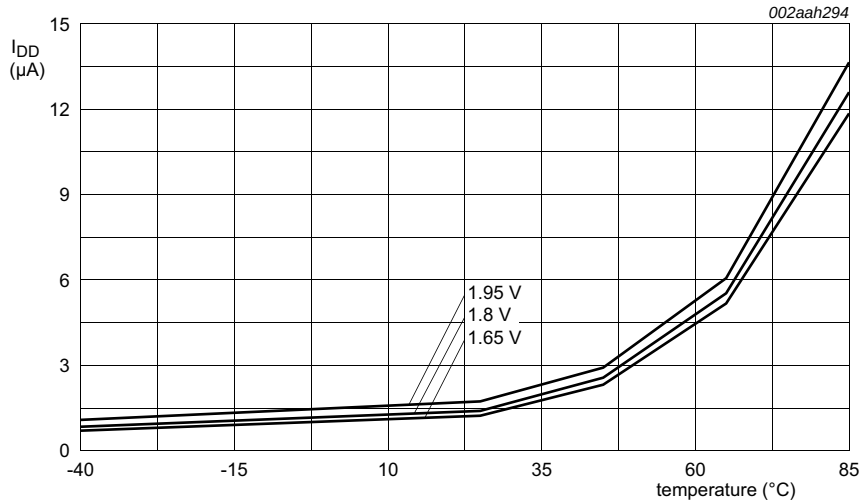



Conditions: $T_{amb}$ = 25 °C; $V_{DD}$ = 1.8 V; Sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

**Fig 20. Sleep mode (12 MHz to 48 MHz): Typical supply current $I_{DD}$ versus temperature for different clock frequencies**




Conditions: all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

**Fig 21. Deep-sleep mode: Typical supply current $I_{DD}$ versus temperature**

## 10.3 Internal oscillators

**Table 11. Dynamic characteristic: internal oscillators**
*$V_{DD}$ = 1.65V to 1.95 V.*

| Symbol | Parameter | Conditions | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{osc(RC)}$ | internal RC oscillator frequency | *-20 °C ≤ $T_{amb}$ ≤ +85 °C* | 12 - 2.5 % | 12 | 12 + 2.5 % | MHz |
| | | *-40 °C ≤ $T_{amb}$ < -20 °C* | 12 - 5 % | 12 | 12 + 5 % | MHz |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

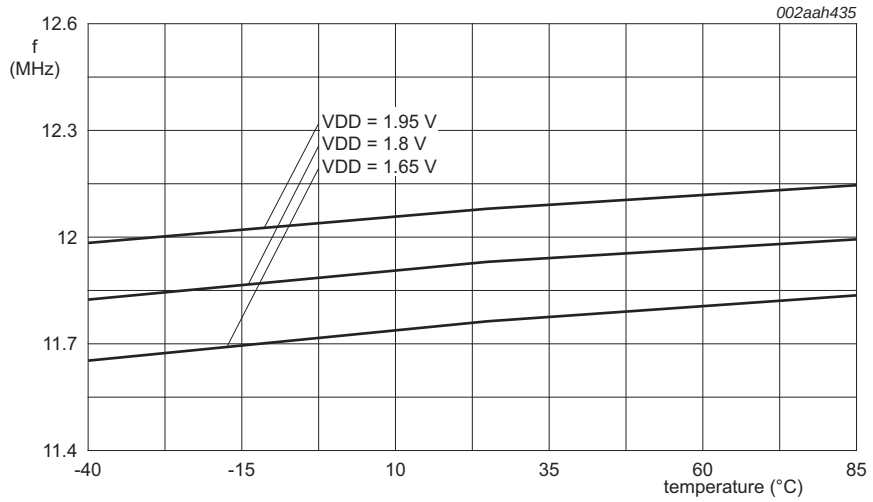



**Fig 23. Typical internal RC oscillator frequency for different supply voltages $V_{DD}$**

**Table 12. Dynamic characteristics: Watchdog oscillator**

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{osc(int)}$ | internal oscillator frequency | DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register; | [2][3] | - | 9.4 | - | kHz |
| | | DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register | [2][3] | - | 2300 | - | kHz |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature ($T_{amb}$ = −40 °C to +85 °C) is ±40 %.

[3] See the *LPC111xLV user manual*.

## 10.4 I²C-bus

**Table 13. Dynamic characteristic: I²C-bus pins[1]**
*$T_{amb}$ = −40 °C to +85 °C.[2]*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | Standard-mode | 0 | 100 | kHz |
| | | Fast-mode | 0 | 400 | kHz |
| | | Fast-mode Plus | 0 | 1 | MHz |

**Table 13. Dynamic characteristic: I²C-bus pins[1]**
*$T_{amb}$ = −40 °C to +85 °C.[2]*

| Symbol | Parameter | | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $t_f$ | fall time | [4][5][6][7] | of both SDA and SCL signals | - | 300 | ns |
| | | | Standard-mode | | | |
| | | | Fast-mode | $20 + 0.1 \times C_b$ | 300 | ns |
| | | | Fast-mode Plus | - | 120 | ns |
| $t_{LOW}$ | LOW period of the SCL clock | | Standard-mode | 4.7 | - | µs |
| | | | Fast-mode | 1.3 | - | µs |
| | | | Fast-mode Plus | 0.5 | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | Standard-mode | 4.0 | - | µs |
| | | | Fast-mode | 0.6 | - | µs |
| | | | Fast-mode Plus | 0.26 | - | µs |
| $t_{HD;DAT}$ | data hold time | [3][4][8] | Standard-mode | 0 | - | µs |
| | | | Fast-mode | 0 | - | µs |
| | | | Fast-mode Plus | 0 | - | µs |
| $t_{SU;DAT}$ | data set-up time | [9][10] | Standard-mode | 250 | - | ns |
| | | | Fast-mode | 100 | - | ns |
| | | | Fast-mode Plus | 50 | - | ns |

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH}$(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] $C_b$ = total capacitance of one bus line in pF.

[6] The maximum $t_f$ for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage $t_f$ is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified $t_f$.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period ($t_{LOW}$) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

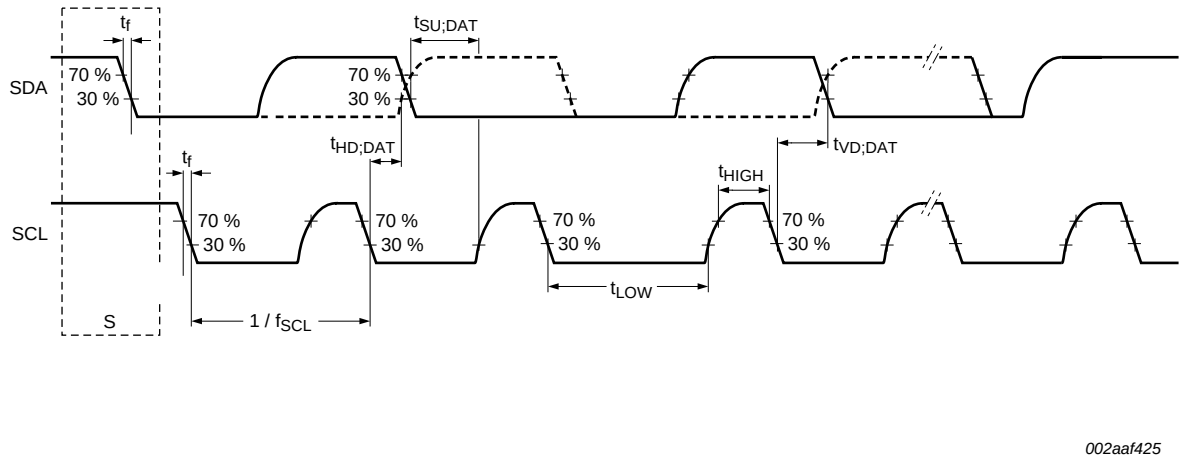



**Fig 24. I²C-bus pins clock timing**

## 10.5 SPI interface

**Table 14. Dynamic characteristics of SPI pins in SPI mode**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **SPI master (in SPI mode)** | | | | | | | |
| $T_{cy(clk)}$ | clock cycle time | full-duplex mode | [1] | 50 | - | - | ns |
| | | when only transmitting | [1] | 40 | - | - | ns |
| $t_{DS}$ | data set-up time | in SPI mode<br>1.8 V < $V_{DD}$ < 1.95 V | [2] | 24 | - | - | ns |
| $t_{DH}$ | data hold time | in SPI mode | [2] | 0 | - | - | ns |
| $t_{v(Q)}$ | data output valid time | in SPI mode | [2] | - | - | 10 | ns |
| $t_{h(Q)}$ | data output hold time | in SPI mode | [2] | 0 | - | - | ns |

[1] $T_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / $f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency $f_{main}$, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] $T_{amb}$ = −40 °C to 85 °C.

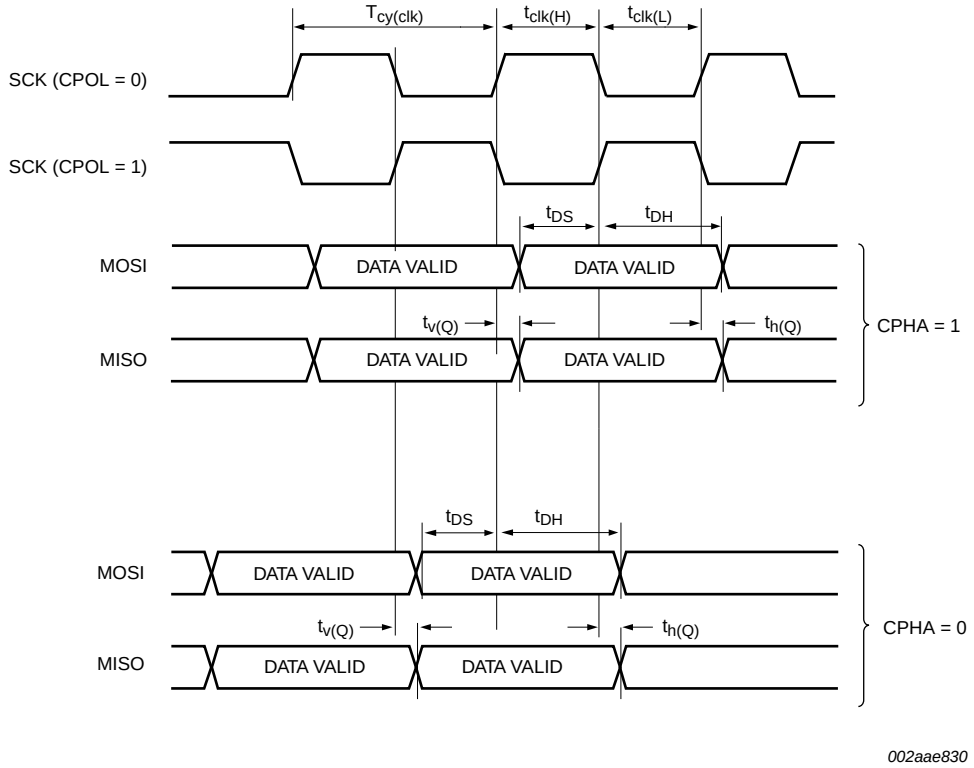



**Fig 26. SPI slave timing in SPI mode**

# 11. Application information

## 11.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 6:

- The ADC input trace must be short and as close as possible to the LPC111xLV/LPC11xxLVUK chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

## 11.2 Standard I/O pad configuration

Figure 27 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

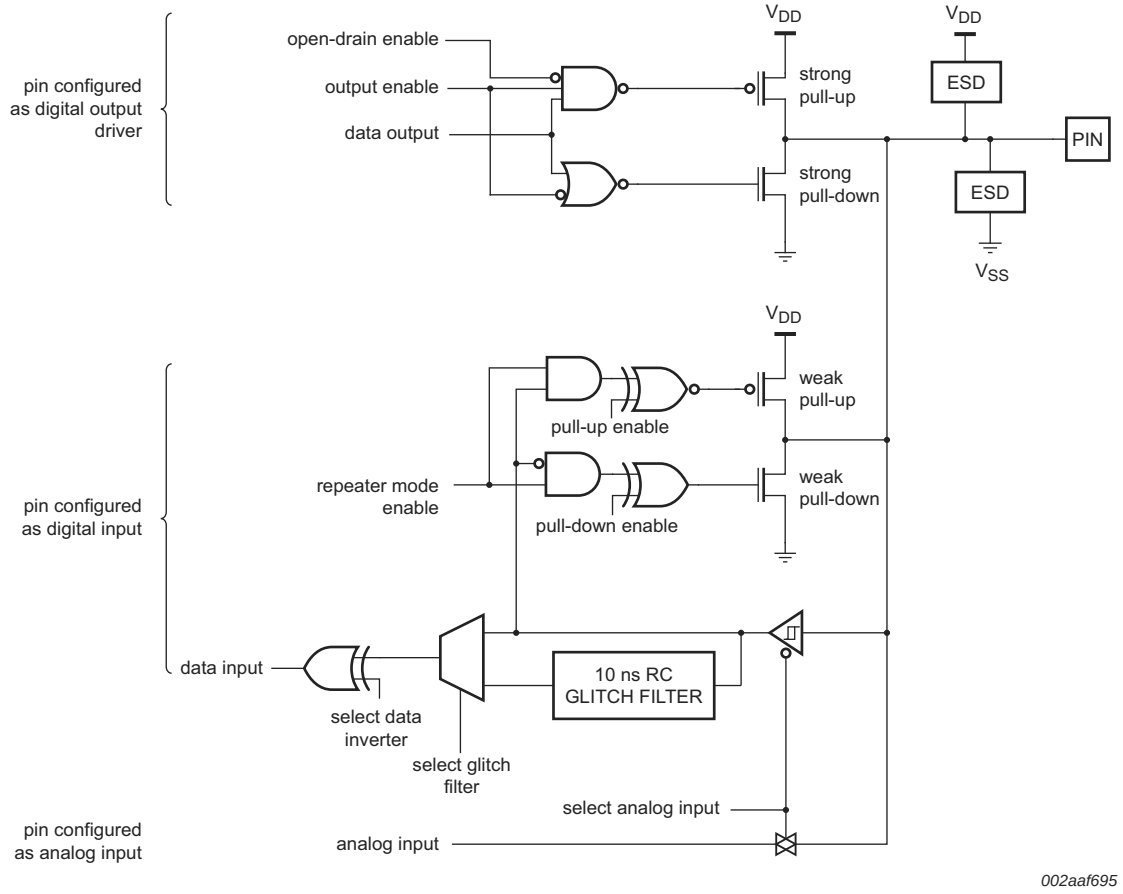



**Fig 27. Standard I/O pad configuration**

## 11.3 Reset pad configuration

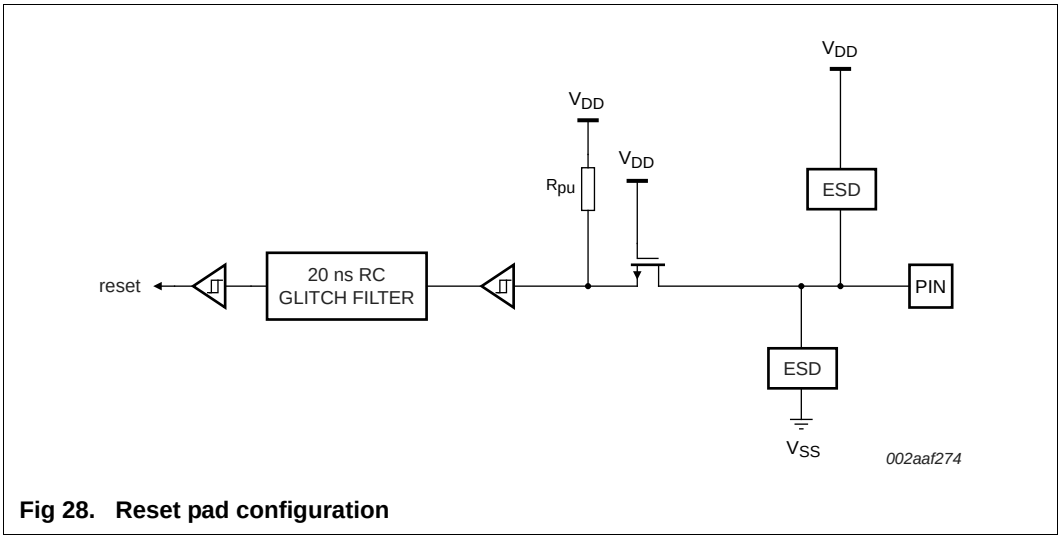
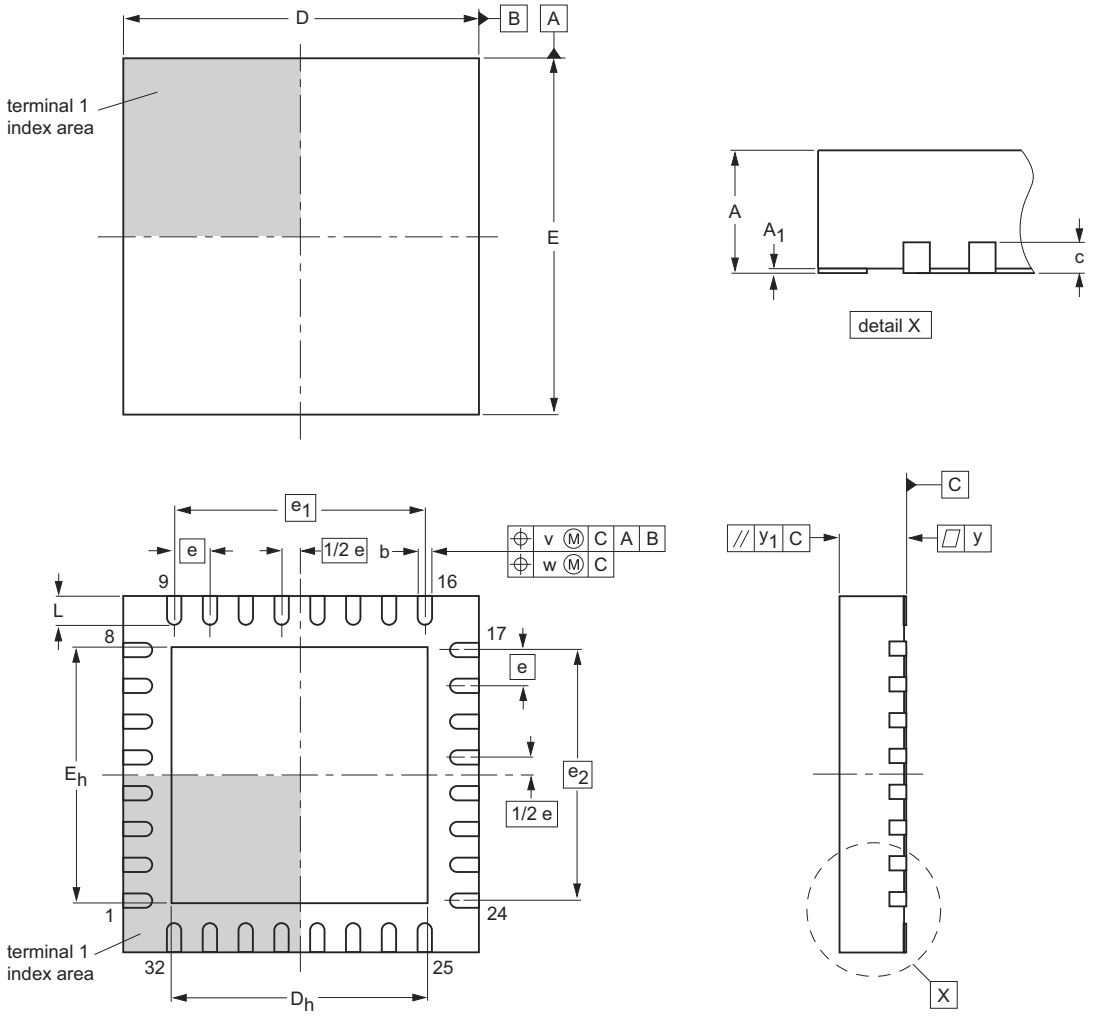



**Fig 28. Reset pad configuration**

**HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm**




Dimensions (mm are the original dimensions)

| Unit[1] | | A[1] | $A_1$ | b | c | D[1] | $D_h$ | E[1] | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.85 | 0.05 | 0.30 | 0.2 | 5.1 | 3.75 | 5.1 | 3.75 | 0.5 | 3.5 | 3.5 | 0.5 | 0.1 | 0.05 | 0.05 | 0.1 |
| | nom | | | | | | | | | | | | | | | | |
| | min | | 0.00 | 0.18 | | 4.9 | 3.45 | 4.9 | 3.45 | | | | 0.3 | | | | |

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

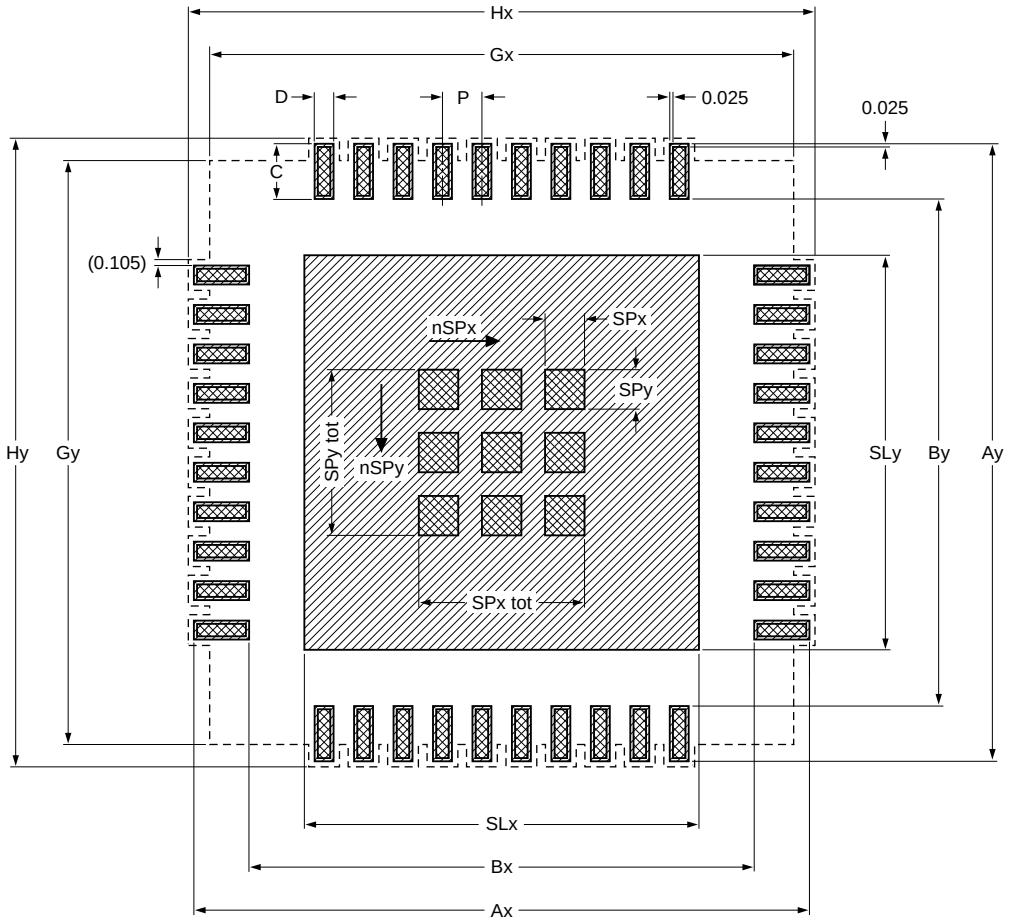
*hvqfn33f_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| | | MO-220 | | | | ~~11-10-11~~ 11-10-17 |

**Fig 31. Package outline (HVQFN33)**

# 13. Soldering

**Footprint information for reflow soldering of HVQFN24 package** **SOT616-3**




Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

| nSPx | nSPy |
|---|---|
| 2 | 2 |

Dimensions in mm

| P | Ax | Ay | Bx | By | C | D | SLx | SLy | SPx tot | SPy tot | SPx | SPy | Gx | Gy | Hx | Hy |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.500 | 5.000 | 5.000 | 3.200 | 3.200 | 0.900 | 0.240 | 2.500 | 2.500 | 1.500 | 1.500 | 0.550 | 0.550 | 4.300 | 4.300 | 5.250 | 5.250 |

Issue date ~~07-05-07~~ 09-06-15 *sot616-3_fr*

**Fig 32. Reflow soldering for the HVQFN24 package**

# 15. Revision history

**Table 16. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| LPC111XLV_LPC11XXLVUK v.2 | 20121010 | Product data sheet | - | LPC111XLV_LPC11XXLVUK v.1 |
| Modifications: | • Functions CT16B0_CAP1/RXD added to pin PIO3_4.<br>• Functions CT16B1_CAP1/TXD added to pin PIO3_5.<br>• Function CT32B1_CAP1 added to pin PIO1_11.<br>• Capture/clear functionality added to counter/timers. See Section 7.12.<br>• Figure 21 “Deep-sleep mode: Typical supply current $I_{DD}$ versus temperature” updated.<br>• Electrical pin characteristics data combined in Section 9.2 for dual and single power supplies.<br>• SSP timing characteristics in slave mode removed for single power supply parts in Table 14.<br>• Table 11 “Dynamic characteristic: internal oscillators” and Figure 23 updated.<br>• Figure 33 corrected.<br>• Removed dual-power supply option. All parts use a single 1.8 V +/- 10 % power supply.<br>• Removed 10-bit ADC. Only the 8-bit ADC is available.<br>• Temperature range for ADC characteristics on the HVQFN24 package restricted to $T_{amb}$ = -10 °C to +85 °C.<br>• BOD interrupt level 0 removed in Table 8.<br>• IRC accuracy updated to 2.5 % accuracy for $T_{amb}$ = -20 °C to +85 °C and to 5 % accuracy for $T_{amb}$ = -40 °C to -20 °C.<br>• Data sheet status changed to Product data sheet. | | | |
| LPC111XLV_LPC11XXLVUK v.1 | 20120621 | Objective data sheet | - | - |

# 16. Legal information

# 17. Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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